AN5441S

Deflection distortion correction IC

■ Overview

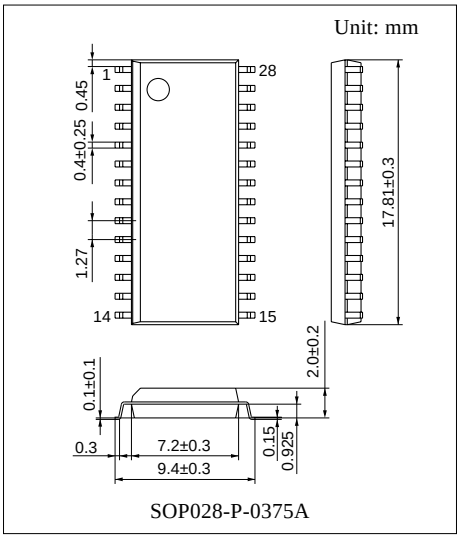
The AN5441S is a distortion correction processing IC for deflection system of color televisions and wide screen televisions.

■ Features

- Distortion correcting functions
  - Vertical amplitude
  - Vertical linearity
  - Vertical S-shape
  - Vertical position
  - Vertical EHT
  - Horizontal amplitude
  - EW parabola
  - Trapezoidal
  - Upper/lower EW corner
  - Horizontal EHT
- Built-in horizontal and vertical blanking pulse generation circuit
- Supports I^2C bus control

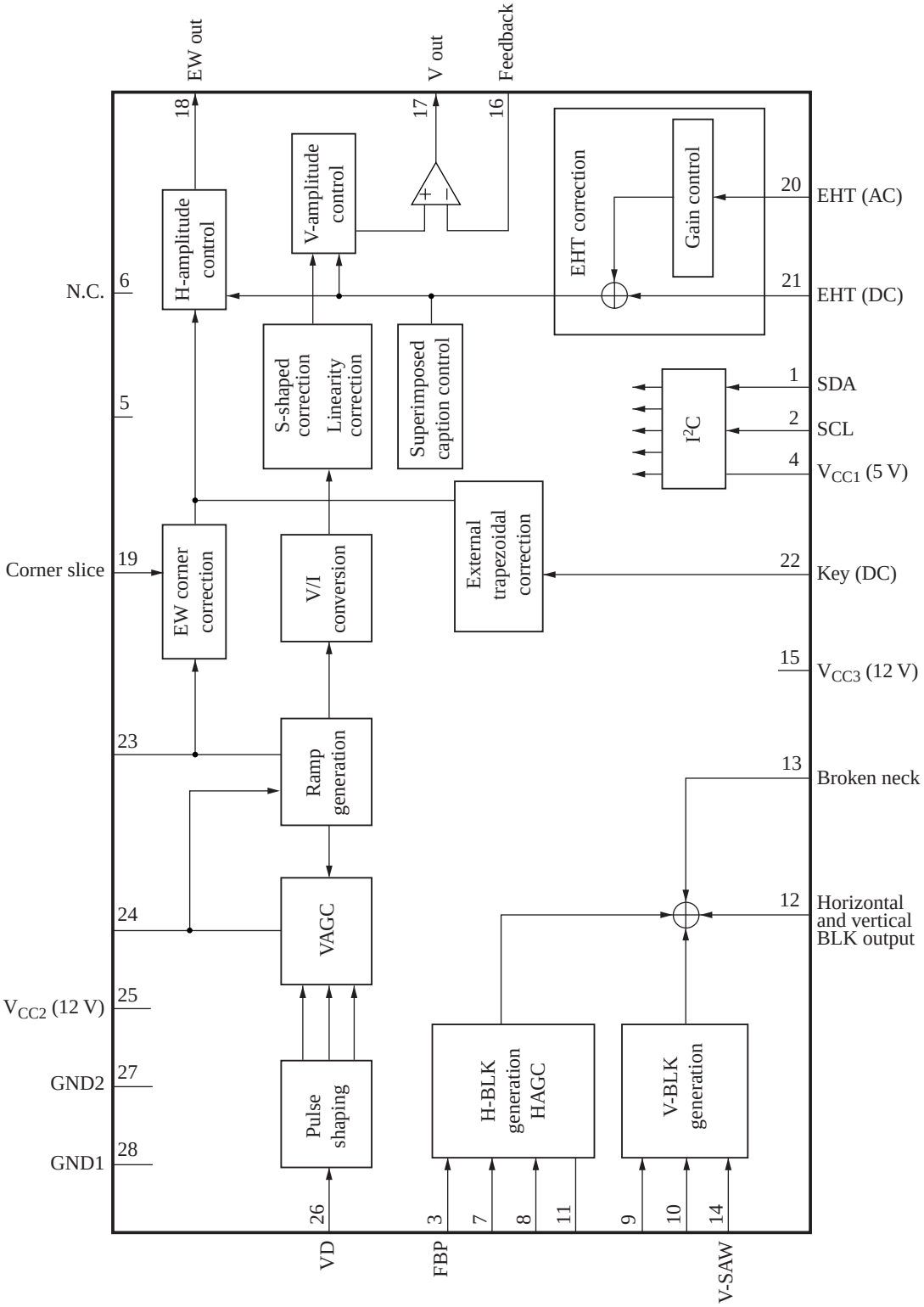
■ Applications

- Color televisions and wide screen televisions



SOP028-P-0375A

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	I^2C SDA input	15	V_{CC3} (12 V)
2	I^2C SCL input	16	Vertical feedback input
3	Horizontal FBP input	17	Vertical pre-drive output
4	V_{CC1} (5 V)	18	EW output
5	Test pin	19	Corner slice voltage
6	N.C.	20	EHT-AC input
7	H-BLK high-level slice voltage	21	EHT-DC input
8	H-BLK low-level slice voltage	22	Control for keystone correction
9	V-BLK high-level slice voltage	23	Capacitor for ramp generation
10	V-BLK low-level slice voltage	24	Capacitor for V-AGC
11	Capacitor for H-AGC	25	V_{CC2} (12 V)
12	Horizontal and vertical BLK output	26	VD pulse input
13	Broken neck detection	27	GND2
14	V-BLK sawtooth input	28	GND1

■ Absolute Maximum Ratings

Parameter	Symbol		Rating	Unit
Supply voltage	V_{CC}	V_{CC1}	5.6	V
		V_{CC2} , V_{CC3}	13.4	
Supply current	I_{CC}	I_{CC1}	24.5	mA
		I_{CC2}	24.0	
		I_{CC3}	3.2	
Power dissipation *2	P_D		449	mW
Operating ambient temperature *2	T_{opr}		−20 to +70	°C
Storage temperature *1	T_{stg}		−55 to +150	°C

Note) ∗1 : Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

∗2 : The power dissipation shown is the value for T_a = 70°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1}	4.5 to 5.5	V
	V_{CC2}	10.8 to 13.2	
	V_{CC3}	10.8 to 13.2	

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Circuit current I_{CC1}	I_4	V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 12 V	11.7	17.0	20.2	mA
Circuit current I_{CC2}	I_{25}	V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 12 V	13.1	16.6	20.2	mA
Circuit current I_{CC3}	I_{15}	V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 12 V	1.8	2.1	2.3	mA
EHT-AC input pin voltage	$V_{20\text{-}27,\ 28}$	V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 12 V	2.6	3.0	3.4	V
Vertical pull-in frequency 1	f_{V1}	f_V = 50 Hz input	45	50	55	Hz
Vertical pull-in frequency 2	f_{V2}	f_V = 60 Hz input	55	60	65	Hz
Typical vertical output amplitude	$e_{V(typ)}$	typ.	2.3	2.7	3.1	V[p-p]
Typical EW output amplitude	$e_{E(typ)}$	typ.	1.42	1.82	2.22	V[p-p]
Vertical BLK output pulse width	t_{VB}	Wide	3.3	4.8	6.2	ms
Horizontal BLK output pulse width 1	$t_{HB(1)}$	Normal	11.7	12.2	12.7	µs
Horizontal BLK output pulse width 2	$t_{HB(2)}$	Wide	37	39	41	µs
Vertical output amplitude change ratio (max.)	$\frac{e_{v(max)}}{e_{v(typ)}}$	V amplitude typ. → max. ratio	42	48	54	%
Vertical output amplitude change ratio (min.)	$\frac{e_{v(min)}}{e_{v(typ)}}$	V amplitude typ. → min. ratio	–54	–48	– 42	%
Vertical output S-shape change ratio 1	Δe_{VS1}	Vertical S-shape min. → max. ratio	–20	–13	–6	%
Vertical output S-shape change ratio 2	Δe_{VS2}	Vertical S-shape min. → max. ratio (change of V out 40% to 60% point)	—	1.5	6.0	%
Vertical output (upper side) linearity change ratio 1	Δe_{VC1}	Vertical linearity (upper side) typ. → max.	6	10	14	%
Vertical output (upper side) linearity change ratio 2	Δe_{VC2}	Vertical linearity (upper side) typ. → max.	–14	–10	–6	%
Vertical output position change amount (max.)	$\Delta e_{VP(max)}$	Vertical position typ. → max.	–1.0	– 0.8	– 0.6	V
Vertical output position change amount (min.)	$\Delta e_{VP(min)}$	Vertical position typ. → min.	0.5	0.7	0.9	V
Vertical output (lower side) linearity change ratio 1	—	Vertical linearity (lower side) typ. → max.	8	12	16	%
Vertical output (lower side) linearity change ratio 2	—	Vertical linearity (lower side) typ. → min.	–16	–12	– 8	%
Vertical output EHT-DC change	Δe_{VED}	EHT-DC = 6 V, vertical EHT, min. → max.	–24.8	–21.8	–18.8	%
Vertical output EHT-AC change 1	$\Delta e_{VEA(1)}$	EHT-AC = 2V, VEHT: max., EHT gain, min. → max.	–16	–12	–8	%
Vertical output EHT-AC change 2	$\Delta e_{VEA(2)}$	EHT-AC = 4 V, VEHT: max., EHT gain, min. → max.	9	13	17	%
Vertical output superimposed caption change 1	$\Delta e_{VJ(1)}$	Vertical superimposed caption min. → max.	–13	–10	–7	%
Vertical output superimposed caption change 2	$\Delta e_{VJ(2)}$	Vertical superimposed caption min. → max., V amplitude typ. → min.	–15	–11	–7	%

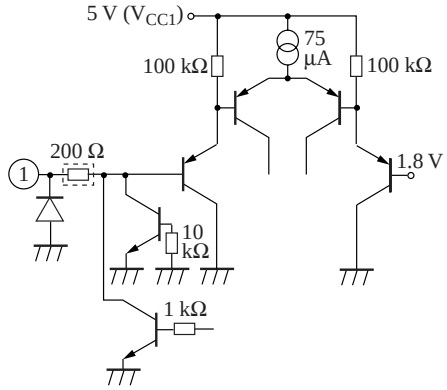
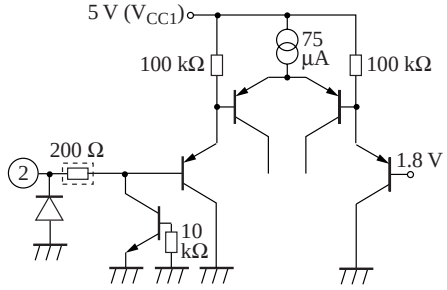
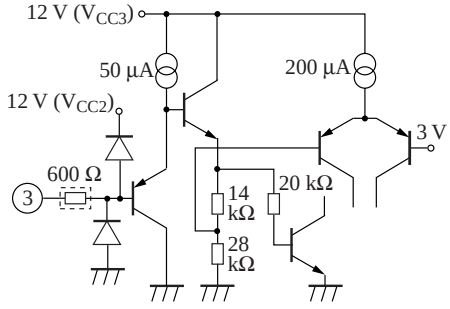
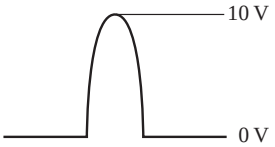
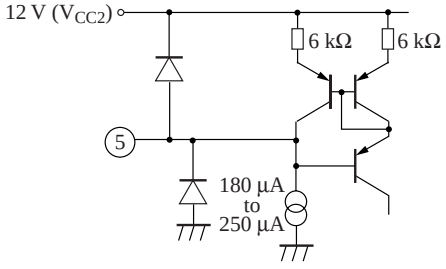
■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Vertical output amplitude (max.)	$\Delta e_{V(max)}$	V amplitude max.	3.5	3.9	4.3	V
Vertical output amplitude (min.)	$\Delta e_{V(min)}$	V amplitude min.	1.1	1.4	1.7	V
Vertical output center DC level	Δe_{VDC}	typ.	4.5	4.9	5.3	V
EW output parabolic amplitude change (min.)	$e_{E(min)}$	Parabolic amplitude min.	0	0.1	0.5	V[p-p]
EW output parabolic amplitude change (max.)	$e_{E(max)}$	Parabolic amplitude max.	2.5	3.5	4.5	V[p-p]
EW output horizontal amplitude change (min.)	$e_{ED(min)}$	Horizontal amplitude min.	5.45	6.0	6.93	V
EW output horizontal amplitude change (max.)	$e_{ED(max)}$	Horizontal amplitude max.	0.7	2.0	2.6	V
EW output trapezoidal change (min.)	$\Delta e_{ET(min)}$	Trapzoidal SW : On, trapezoidal typ. → min.	64	96	126	%
EW output trapezoidal change (max.)	$\Delta e_{ET(max)}$	Trapzoidal SW : On, trapezoidal typ. → max.	−130	−100	−68	%
EW output upper corner change (min.)	$\Delta e_{ECT(min)}$	Upper corner min.	−95	−65	−35	%
EW output upper corner change (max.)	$\Delta e_{ECT(max)}$	Upper corner max.	30	60	90	%
EW output lower corner change (min.)	$\Delta e_{ECB(min)}$	Lower corner min.	−95	−65	−35	%
EW output lower corner change (max.)	$\Delta e_{ECB(max)}$	Lower corner max.	25	55	85	%
EW output (bottom voltage) EHT-DC change	Δe_{EED}	EHT-DC: 6 V Horizontal EHT min. → max.	2.1	2.6	3.1	V
EW output (bottom voltage) EHT-AC change 1	$\Delta e_{EEA(1)}$	EHT-AC: 2 V, horizontal EHT: max., EHT gain min. → max.	1.2	1.4	1.6	V
EW output (bottom voltage) EHT-AC change 2	$\Delta e_{EEA(2)}$	EHT-AC: 4 V , horizontal EHT: max., EHT gain min. → max.	−1.8	−1.5	−1.2	V
EW output (EW amplitude) KEY change 1 (min.)	$\Delta e_{EK(min1)}$	KEY = 2 V, trapezoidal SW: On, trapezoidal max. → min.	95	120	145	%
EW output (EW amplitude) KEY change 1 (max.)	$\Delta e_{EK(max1)}$	KEY = 3.2 V, trapezoidal SW: On, trapezoidal min. → max.	−145	−120	−95	%
EW output parabolic DC level	e_{EB}	typ.	2.9	4.0	5.1	V
EW output (EW amplitude) KEY change 2 (min.)	$\Delta e_{EK(min2)}$	KEY = 2 V, trapezoidal SW: Off, trapezoidal max. → min.	−145	−120	−95	%
EW output (EW amplitude) KEY change 2 (max.)	$\Delta e_{EK(max2)}$	KEY = 3.2 V, trapezoidal SW: Off, trapezoidal min. → max.	95	120	145	%
EW output drive current 1	$I_{EW(1)}$	Pin 18: 11 V	0.7	1.1	1.5	mA
V-AGC input and output current	I_{VAGC}		0.5	0.8	1.1	mA
H-AGC input and output current	I_{HAGC}		0.7	1.0	1.3	mA

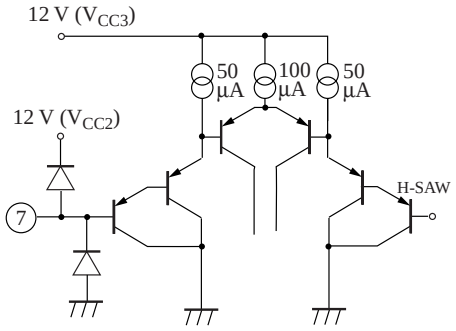
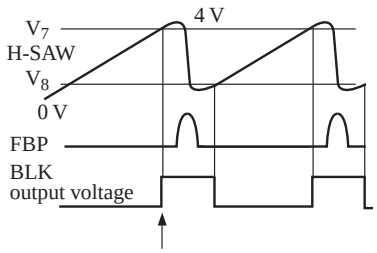
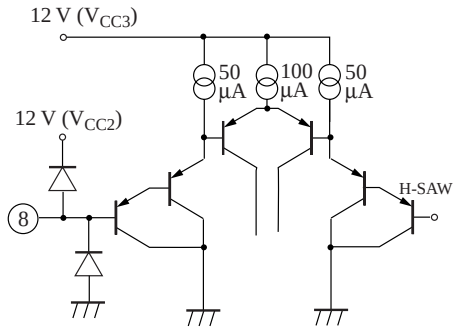
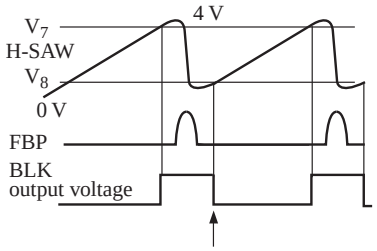
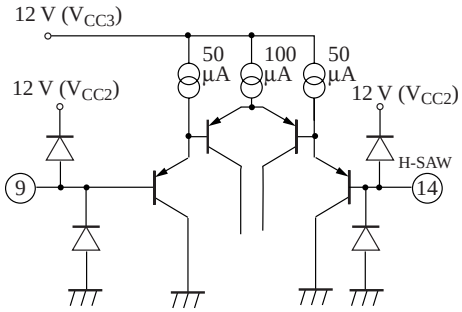
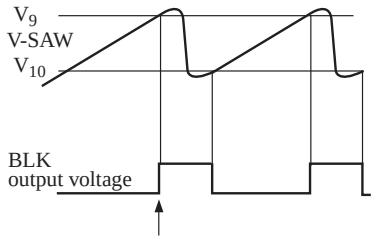
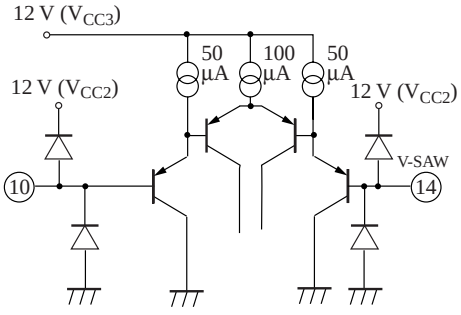
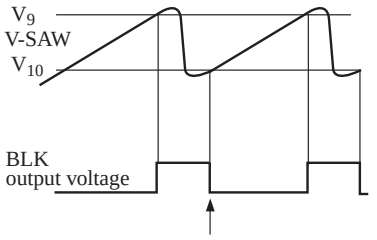
■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Ramp discharge current	I_{RD}		6.7	8.9	11.1	mA
Ramp charge current 1	$I_{RC(1)}$	Pin 24: 1 V	40	45	52	µA
Vertical output at service SW	V_{SSW}		4.55	4.95	5.35	V
Broken neck threshold voltage	V_{Neck}	Service SW: Off	0.5	0.7	0.9	V
BLK output amplitude	V_{BO}		2.8	3.1	3.4	V
H-AGC voltage 1	$V_{HAGC(1)}$	HD: 14 kHz	2.6	3.25	3.9	V
H-AGC voltage 2	$V_{HAGC(2)}$	HD: 17 kHz	3.1	3.85	4.6	V
H-AGC pulse width	f_{HA}	3 kΩ resistor between pin 11 and GND	1.5	2.2	3.0	µs
V-AGC pulse width	f_{VA}	3 kΩ resistor between pin 24 and GND	75	110	150	µs
EW output drive current 2	$I_{EW(2)}$	Pin 18: 1 V	–1.3	– 0.9	– 0.5	mA
Ramp charge current 2	$I_{RC(2)}$	Pin 24: 10 V	7	10	13	µA
H-AGC current ΔV	$V_{HAGC\Delta V}$	HD: 17 kHz ΔV	0.2	0.6	1.1	V
VD input threshold value	V_{VD}		0.9	1.3	1.7	V
FBP input threshold value	V_{FBP}		0.5	0.7	0.9	V
High-level I^2C SDA input	$V_{SDA(H)}$		4.0	—	V_{CC1}	V
low-level I^2C SDA input	$V_{SDA(L)}$		0	—	0.7	V
High-level I^2C SCL input	$V_{SCL(H)}$		4.0	—	V_{CC1}	V
Low-level I^2C SCL input	$V_{SCL(L)}$		0	—	0.7	V
Maximum input allowable frequency	$f_{i\ max}$		100	—	—	kHz
Vertical output amplitude with supply voltage fluctuation	$\Delta e_{V\text{-}Vcc}$	Difference of $V_{CC(max)} - V_{CC(min)}$	0	0.1	0.5	V
Vertical output with DC supply voltage fluctuation	$\Delta e_{VD\text{-}Vcc}$	Difference of $V_{CC(max)} - V_{CC(min)}$	0.5	1.0	1.5	V
EW output amplitude with supply voltage fluctuation	$\Delta e_{E\text{-}Vcc}$	Difference of $V_{CC(max)} - V_{CC(min)}$	0	0.1	0.5	V
EW output with DC supply voltage fluctuation	$\Delta e_{ED\text{-}Vcc}$	Difference of $V_{CC(max)} - V_{CC(min)}$	0.4	1.0	1.6	V
Sink current at ACK	I_{ACK}	Maximum value of pin 1 sink current at ACK	—	2.5	—	mA
3-bit, 4-bit, 6-bit, 7-bit DAC DNLE	$L_{3, 4, 6, 7}$	1LSB = {data (max.) – data (00)}/ 7, 15, 63, 127	0.1	1.0	1.9	LSB/ step
Vertical output drive current	$I_{V\ Out}$		7	11	15	mA

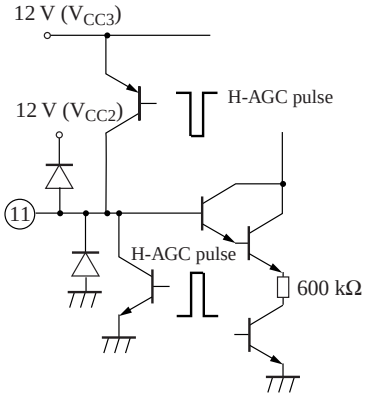
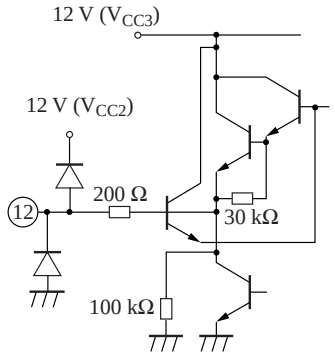
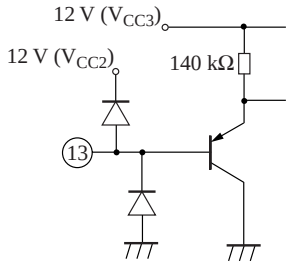
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	Voltage
1		I^2C bus data input pin: Sink current: typ. 2.5 mA	AC (Pulse)
2		I^2C bus clock input pin	AC (Pulse)
3		FBP input pin: 	AC (Pulse)
4	—	V_{CC1} (typ. 5 V): For I^2C circuit	DC 5 V
5		Test pin: Attach a capacitor (0.082 µF) for filter to GND.	DC 10.6 V

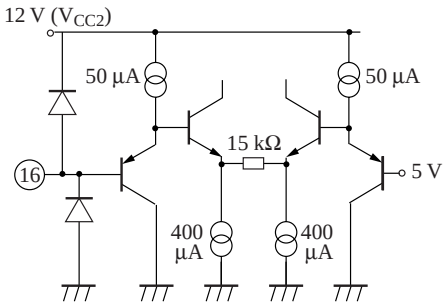
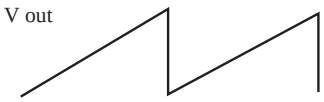
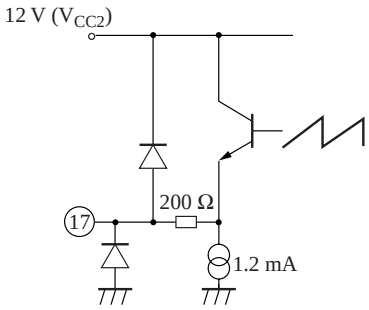
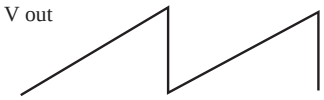
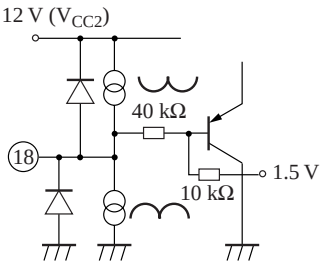
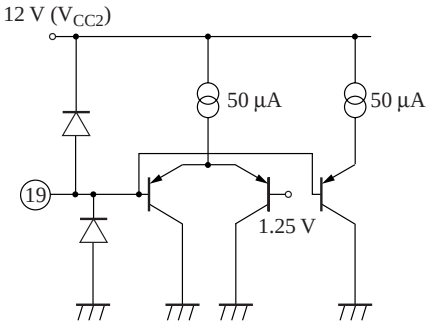
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
6	—	N.C	N.C.
7		HBLK high-level slice voltage: 	DC typ. 0 V to 4 V
8		HBLK low-level slice voltage: 	DC typ. 0 V to 4 V
9		VBLK high-level slice voltage: For I^2C circuit 	DC typ. 0 V to 10 V
10		VBLK low-level slice voltage: 	DC 0 V to 10 V

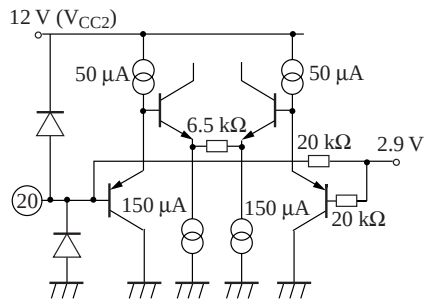
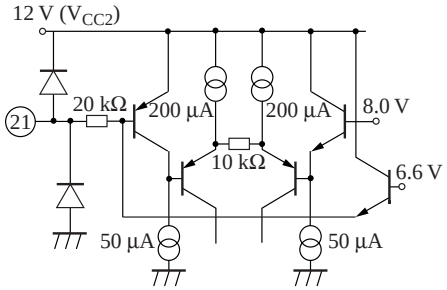
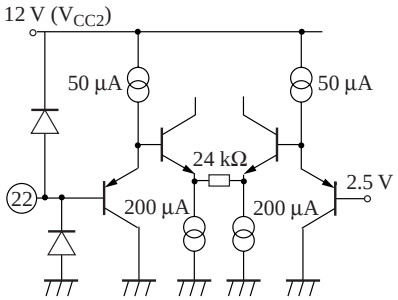
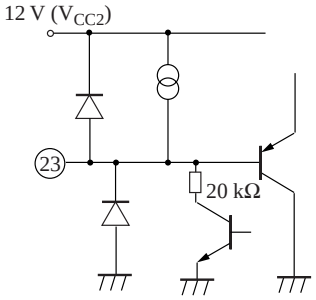
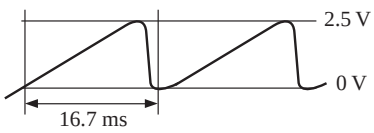
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
11		H sawtooth AGC voltage pin	DC 1.5 V to 10 V
12		Blanking pulse output pin: Horizontal/vertical BLK output pin Blanking output high-level with neck input low-level	AC (Pulse)
13		Broken neck detection pin: Normal; High-level (apply 1 V or more) Abnormal; Low-levrl (apply 0.4 V or more) (Broken neck mode) There is no broken neck operation when service SW is on.	DC
14	Refer to pin 9 and pin 10 equivalent circuit.	Sawtooth input pin for V-BLK: 	AC
15	—	V_{CC3} (typ. 12 V): For BLK pulse generation circuit.	DC 12 V

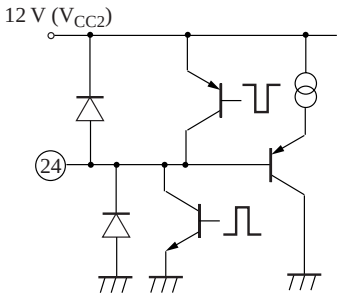
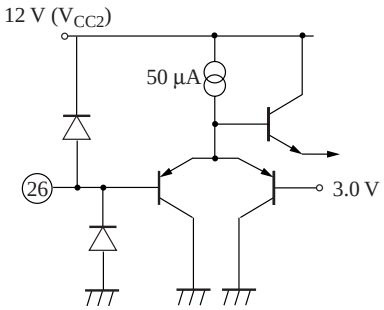
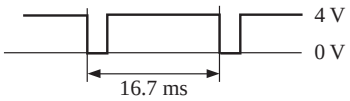
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
16		Vertical feedback input pin:  Short-circuit this pin with pin 17 in normal use	AC
17		Vertical output pin:  Short-circuit this pin with pin 16 in normal use	AC
18		EW output pin: 	AC
19		Upper and lower corner slice voltage input pin	DC 0 V to 1.5 V

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
20		EHT-AC input pin	AC Open approx. 2.9 V
21		EHT-DC input pin	DC 6 V to 10 V (typ. 8 V)
22		External shape trapezoidal correction DC control pin	DC 1.5 V to 3.5 V (typ. 2.5 V)
23		Ramp reference waveform generation pin: 	AC

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
24		AGC pin for ramp	AC
25	—	V_{CC2} (typ. 12 V): For I^2C circuit and correction system circuit	DC
26		V pulse input pin: 	AC (Pulse)
27	—	GND2: For analog circuit block	DC
28	—	GND1: For digital circuit block	DC

■ Application Circuit Example