AN5395FBP

Contour correction IC for HDTV

■ Overview

The AN5395FBP is a contour correction IC which enables correction band changeover for base band HDTV, MUSE, progressive NTSC TV.

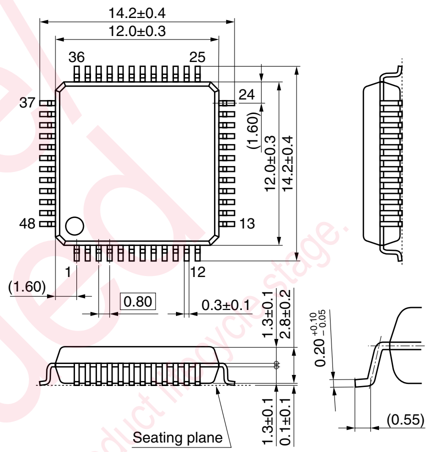
■ Features

- Contour correction for HDTV
- Contour correction for progressive TV

■ Applications

- HDTV

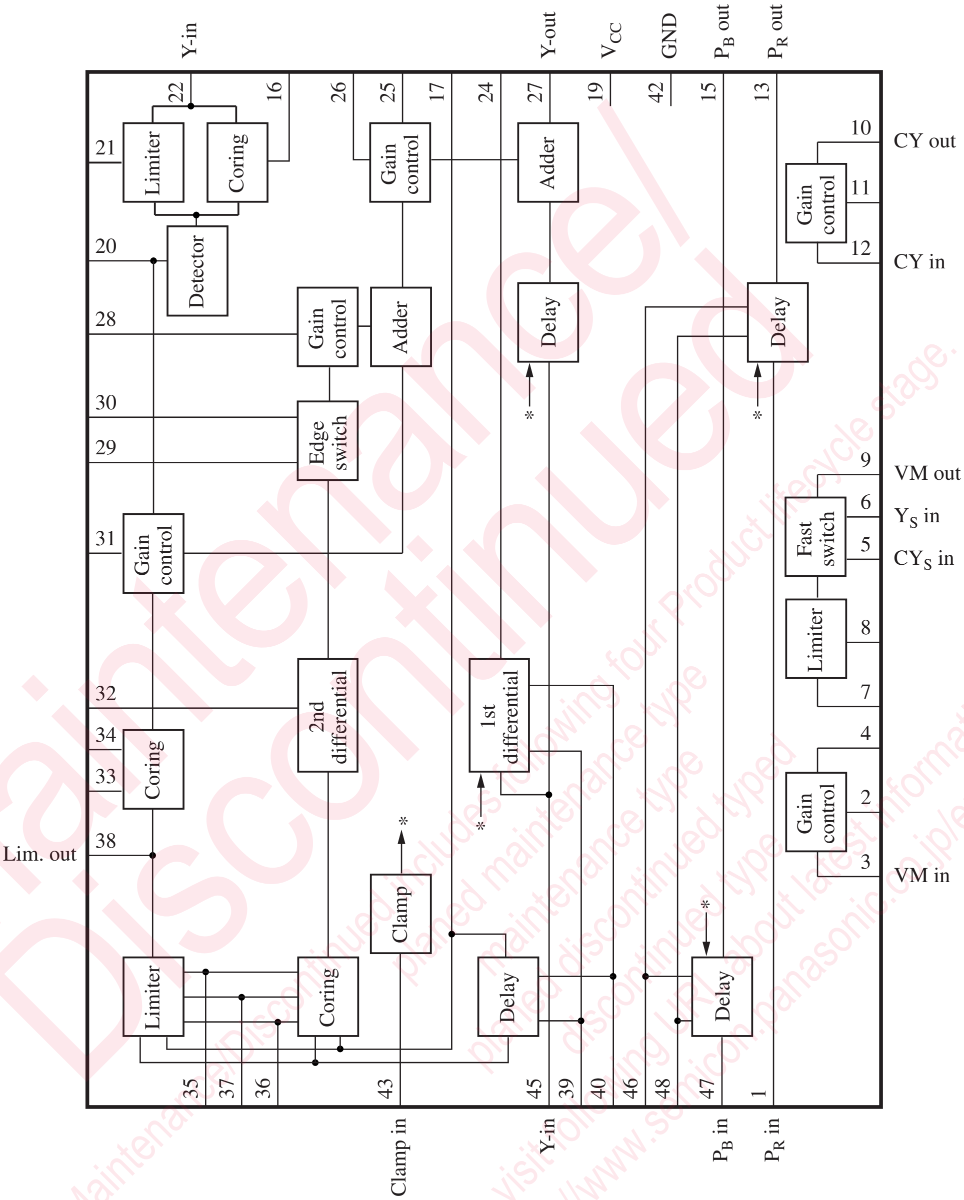
Unit: mm



QFH048-P-1212A

Note) The package of this product will be changed to lead-free type (QFH048-P-1212C). See the new package dimensions section later of this datasheet.

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	P_R input	25	Sharpness mute control
2	VM pre-amp. gain control	26	Sharpness control
3	VM pre-amp. input	27	Y output
4	VM pre-amp. output	28	Contour block gain control
5	Child picture Y_S input	29	Contour block bias
6	Y_S input	30	Secondary differentiating input
7	VM limiter amp. input	31	Detail gain control
8	VM limiter amp. gain control	32	Primary differentiating output after correction
9	VM limiter amp. output	33	Detail coring control
10	Child picture amp. output	34	Detail coring bias
11	Child picture amp. gain control	35	Differentiating signal bias 1
12	Child picture amp. input	36	Contour block and detail separation level control
13	P_R output		
14	N.C.	37	Differentiating signal bias 2
15	P_B output	38	Detail limiter output
16	DSC large signal gain control	39	Y delay line changeover switch 1
17	Primary differentiating input before correction	40	Y delay line changeover switch 2
18	N.C.	41	N.C.
19	V_{CC}	42	GND
20	DSC detection output	43	Clamp pulse input
21	DSC small signal gain control	44	N.C.
22	DSC input	45	Y input
23	DSC bias	46	C delay line changeover switch 1
24	Primary differentiating output before correction	47	P_B input
		48	C delay line changeover switch 2

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	10.0	V
Supply current	I_{CC}	100	mA
Power dissipation *2	P_D	650	mW
Operating ambient temperature *1	T_{opr}	−20 to +70	°C
Storage temperature *1	T_{stg}	−55 to +150	°C

Note) *1: Except for the operating ambient temperature and storage temperature, all ratings are for $T_a = 25°C$.
*2: The power dissipation shown is the value for $T_a = 70°C$.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	8.1 to 9.9	V

■ Electrical Characteristics at $T_a = 25°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Circuit current	I_{CC}		50	70	90	mA
Circuit voltage	V_1		4.50	5.63	6.76	V
Circuit voltage	V_2		4.40	5.86	7.33	V
Circuit voltage	V_3		2.04	2.55	3.06	V
Circuit voltage	V_4		4.64	5.80	6.96	V
Circuit voltage	V_7		2.04	2.55	3.06	V
Circuit voltage	V_9		4.60	5.75	6.90	V
Circuit voltage	V_{10}		4.64	5.80	6.96	V
Circuit voltage	V_{11}		4.40	5.86	7.33	V
Circuit voltage	V_{12}		2.04	2.55	3.06	V
Circuit voltage	V_{13}		3.74	4.67	5.60	V
Circuit voltage	V_{15}		3.74	4.67	5.60	V
Circuit voltage	V_{16}		3.80	4.75	5.70	V
Circuit voltage	V_{17}		4.50	5.63	6.76	V
Circuit voltage	V_{21}		3.40	4.25	5.10	V
Circuit voltage	V_{22}		2.12	2.65	3.18	V
Circuit voltage	V_{24}		3.70	4.62	5.54	V
Circuit voltage	V_{27}		3.44	4.30	5.16	V
Circuit voltage	V_{29}		2.93	3.66	4.39	V
Circuit voltage	V_{30}		1.96	2.45	2.94	V
Circuit voltage	V_{31}		2.71	3.61	4.51	V
Circuit voltage	V_{32}		2.12	2.65	3.18	V
Circuit voltage	V_{33}		4.27	5.34	6.41	V
Circuit voltage	V_{34}		4.55	5.69	6.83	V
Circuit voltage	V_{35}		2.65	3.31	3.97	V
Circuit voltage	V_{36}		2.40	3.00	3.60	V
Circuit voltage	V_{37}		2.65	3.31	3.97	V
Circuit voltage	V_{38}		6.25	7.81	9.37	V
Circuit voltage	V_{39}		1.80	2.90	4.00	V
Circuit voltage	V_{40}		1.80	2.90	4.00	V
Circuit voltage	V_{45}		4.50	5.63	6.76	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Circuit voltage	V_{46}		1.80	2.90	4.00	V
Circuit voltage	V_{47}		4.50	5.63	6.76	V
Circuit voltage	V_{48}		1.80	2.90	4.00	V
Circuit current	I_{23}		–1.50	0.00	1.50	µA
Circuit current	I_{43}		–1.50	0.00	1.50	µA
C-D.L block						
P_B output dynamic range	V_{DR15}	V_{IN47} = 5.18 V to 6.08 V	0.9	1.2	1.5	V[p-p]
P_R output dynamic range	V_{DR13}	V_{IN1} = 5.18 V to 6.08 V	0.9	1.2	1.5	V[p-p]
Delay time changeover switch C1 threshold level	V_{TH46}		0.9	1.5	2.1	V
Delay time changeover switch C2 threshold level	V_{TH48}		0.9	1.5	2.1	V
P_B signal output gain (HD)	$G_{A(PB,1)}$	$V_{A(PB,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
P_B signal output gain (MUSE)	$G_{B(PB,1)}$	$V_{B(PB,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
P_B signal output gain (NTSC1)	$G_{C(PB,1)}$	$V_{C(PB,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
P_B signal output gain (NTSC2)	$G_{D(PB,1)}$	$V_{D(PB,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
P_B signal output gain difference (MUSE/HD)	$G_{B/A(PB)}$	$V_{B(PB,1)}$ /$V_{A(PB,1)}$	–1	0	1	dB
P_B signal output gain difference (NTSC1/HD)	$G_{C/A(PB)}$	$V_{C(PB,1)}$ /$V_{A(PB,1)}$	–1	0	1	dB
P_B signal output gain difference (NTSC2/HD)	$G_{D/A(PB)}$	$V_{D(PB,1)}$ /$V_{A(PB,1)}$	–1	0	1	dB
P_R signal output gain (HD)	$G_{A(PR,1)}$	$V_{A(PR,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
P_R signal output gain (MUSE)	$G_{B(PR,1)}$	$V_{B(PR,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
P_R signal output gain (NTSC1)	$G_{C(PR,1)}$	$V_{C(PR,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
P_R signal output gain (NTSC2)	$G_{D(PR,1)}$	$V_{D(PR,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
P_R signal output gain difference (MUSE/HD)	$G_{B/A(PR)}$	$V_{B(PR,1)}$ /$V_{A(PR,1)}$	–1	0	1	dB
P_R signal output gain difference (NTSC1/HD)	$G_{C/A(PR)}$	$V_{C(PR,1)}$ /$V_{A(PR,1)}$	–1	0	1	dB
P_R signal output gain difference (NTSC2/HD)	$G_{D/A(PR)}$	$V_{D(PR,1)}$ /$V_{A(PR,1)}$	–1	0	1	dB
P_B, P_R signal output gain difference (HD)	$\Delta G_{A(C)}$	$V_{A(PB,1)}$ /$V_{A(PR,1)}$	–1	0	1	dB
P_B, P_R signal output gain difference (MUSE)	$\Delta G_{B(C)}$	$V_{B(PB,1)}$ /$V_{B(PR,1)}$	–1	0	1	dB
P_B, P_R signal output gain difference (NTSC1)	$\Delta G_{C(C)}$	$V_{C(PB,1)}$ /$V_{C(PR,1)}$	–1	0	1	dB
P_B, P_R signal output gain difference (NTSC2)	$\Delta G_{D(C)}$	$V_{D(PB,1)}$ /$V_{D(PR,1)}$	–1	0	1	dB
P_B signal frequency characteristics (HD)	$G_{A(PB,F)}$	$V_{A(PB,20)}$ /$V_{A(PB,1)}$	–6	–3	0	dB
P_B signal frequency characteristics (MUSE)	$G_{B(PB,F)}$	$V_{B(PB,20)}$ /$V_{B(PB,1)}$	–6	–3	0	dB
P_B signal frequency characteristics (NTSC1)	$G_{C(PB,F)}$	$V_{C(PB,16)}$ /$V_{C(PB,1)}$	–6	–3	0	dB

■ Electrical Characteristics at $T_a = 25°C$ (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
C-D.L block (continued)						
P_B signal frequency characteristics (NTSC2)	$G_{D(PB,F)}$	$V_{D(PB,16)} / V_{D(PB,1)}$	–6	–3	0	dB
P_R signal frequency characteristics (HD)	$G_{A(PR,F)}$	$V_{A(PR,20)} / V_{A(PR,1)}$	–6	–3	0	dB
P_R signal frequency characteristics (MUSE)	$G_{B(PR,F)}$	$V_{B(PR,20)} / V_{B(PR,1)}$	–6	–3	0	dB
P_R signal frequency characteristics (NTSC1)	$G_{C(PR,F)}$	$V_{C(PR,16)} / V_{C(PR,1)}$	–6	–3	0	dB
P_R signal frequency characteristics (NTSC2)	$G_{D(PR,F)}$	$V_{D(PR,16)} / V_{D(PR,1)}$	–6	–3	0	dB
Y-D.L block						
Y output dynamic range	V_{DR27}	V_{IN45} = 5.23 V to 6.43 V	1.2	1.6	2.0	V[p-p]
Clamp pulse input threshold level	V_{TH43}		0.9	1.5	2.1	V
Delay time changeover switch Y1 threshold level	V_{TH39}		0.9	1.5	2.1	V
Delay time changeover switch Y2 threshold level	V_{TH40}		0.9	1.5	2.1	V
Y signal output gain (HD)	$G_{A(Y,1)}$	$V_{A(Y,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
Y signal output gain (MUSE)	$G_{B(Y,1)}$	$V_{B(Y,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
Y signal output gain (NTSC1)	$G_{C(Y,1)}$	$V_{C(Y,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
Y signal output gain (NTSC2)	$G_{D(Y,1)}$	$V_{D(Y,1)}$ / 0.1 V[p-p]	1.81	2.92	3.91	dB
Y signal output gain difference (MUSE/HD)	$G_{B/A(Y)}$	$V_{B(Y,1)} / V_{A(Y,1)}$	–1	0	1	dB
Y signal output gain difference (NTSC1/HD)	$G_{C/A(Y)}$	$V_{C(Y,1)} / V_{A(Y,1)}$	–1	0	1	dB
Y signal output gain difference (NTSC2/HD)	$G_{D/A(Y)}$	$V_{D(Y,1)} / V_{A(Y,1)}$	–1	0	1	dB
Y_1 signal output gain (HD)	$G_{A(Y1,1)}$	$V_{A(Y1,1)}$ / 0.1 V[p-p]	12	15	18	dB
Y_1 signal output gain (MUSE)	$G_{B(Y1,1)}$	$V_{B(Y1,1)}$ / 0.1 V[p-p]	12	15	18	dB
Y_1 signal output gain(NTSC1)	$G_{C(Y1,1)}$	$V_{C(Y1,1)}$ / 0.1 V[p-p]	12	15	18	dB
Y_1 signal output gain (NTSC2)	$G_{D(Y1,1)}$	$V_{D(Y1,1)}$ / 0.1 V[p-p]	12	15	18	dB
Y_1 signal output gain difference (MUSE/HD)	$G_{B/A(Y1)}$	$V_{B(Y1,1)} / V_{A(Y1,1)}$	–1	0	1	dB
Y_1 signal output gain difference (NTSC1/HD)	$G_{C/A(Y1)}$	$V_{C(Y1,1)} / V_{A(Y1,1)}$	–1	0	1	dB
Y_1 signal output gain difference (NTSC2/HD)	$G_{D/A(Y1)}$	$V_{D(Y1,1)} / V_{A(Y1,1)}$	–1	0	1	dB
Y signal frequency characteristics (HD)	$G_{A(Y,F)}$	$V_{A(Y,30)} / V_{A(Y,1)}$	–4	–1	2	dB
Y signal frequency characteristics (MUSE)	$G_{B(Y,F)}$	$V_{B(Y,20)} / V_{B(Y,1)}$	–4	–1	2	dB
Y signal frequency characteristics (NTSC1)	$G_{C(Y,F)}$	$V_{C(Y,16)} / V_{C(Y,1)}$	–4	–1	2	dB
Y signal frequency characteristics (NTSC2)	$G_{D(Y,F)}$	$V_{D(Y,16)} / V_{D(Y,1)}$	–4	–1	2	dB

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Sharpness block						
Sharpness mute switch threshold level	V_{TH25}		1.10	2.65	4.20	V
Contour part max. gain	V_{Rmax}		1.40	1.75	2.10	V[p-p]
Contour part sharpness typ. gain	$V_{R.SHtyp}$		640	800	960	mV[p-p]
Contour part sharpness min. gain	$V_{R.SHmin}$		0	15	30	mV[p-p]
Contour part sharpness gain ratio	$G_{R.SHtyp/max}$	$V_{R.SHtyp}/V_{Rmax}$	–8	–6	–4	dB
Detail part max. gain	V_{Smax}		390	520	650	mV[p-p]
Detail part sharpness typ. gain	$V_{S.SHtyp}$		195	260	325	mV[p-p]
Detail part sharpness min. gain	$V_{S.SHmin}$		0	5	10	mV[p-p]
Detail part sharpness gain ratio	$G_{S.SHtyp/max}$	$V_{S.SHtyp}/V_{Smax}$	–9	–6	–3	dB
Detail part sharpness mute max. gain (on)	$V_{S.SH(M.ON)}$		0	5	10	mV[p-p]
Detail part sharpness mute gain ratio (on/off)	$G_{S.SH(M.ON/OFF)}$	$V_{S.SH(M.ON)}/V_{Smax}$	–60	–50	–40	dB
Contour part						
Coring characteristics (on)	$V_{R.CO(ON)}$		210	280	350	mV[p-p]
Coring characteristics (off)	$V_{R.CO(OFF)}$		0	30	60	mV[p-p]
Correction primary differentiating signal gain (8 MHz)	$V_{R.CO(8M)}$		0.64	0.8	0.96	V[p-p]
Correction primary differentiating signal gain (4 MHz)	$V_{R.CO(4M)}$		1.16	1.45	1.74	V[p-p]
Correction primary differentiating signal gain ratio	$G_{R.CO(8M/4M)}$	$V_{R.CO(8M)}/V_{R.CO(4M)}$	–7	–5	–3	dB
Contour gain switch (LO)	$V_{R.SW(LO)}$		0.88	1.1	1.32	V[p-p]
Contour gain switch gain ratio	$G_{R.SW(L/H)}$	$V_{R.SW(LO)}/V_{Rmax}$	–5	–3	–1	dB
Detail part						
Typ. gain 1	V_{SG1typ}		210	280	350	mV[p-p]
Typ. gain 2	V_{SG2typ}		210	280	350	mV[p-p]
Gain ratio 1	$G_{SG1typ/max}$	V_{SG1typ}/V_{Smax}	–7	–5	–3	dB
Gain ratio 2	$G_{SG2typ/max}$	V_{SG2typ}/V_{Smax}	–7	–5	–3	dB
Detail part coring typ. gain	$V_{S.COtyp}$		225	315	445	mV[p-p]
Detail part coring min. gain	$V_{S.COmin}$		0	75	150	mV[p-p]
Detail part coring gain ratio	$G_{S.COtyp/max}$	$V_{S.COtyp}/V_{Smax}$	–8	–5	–2	dB
Detail part limiter max. gain	$V_{S.Lmax}$		460	580	700	mV[p-p]
Detail part limiter typ. gain	$V_{S.Ltyp}$		320	400	480	mV[p-p]
Detail part limiter gain ratio	$G_{S.Ltyp/max}$	$V_{S.Ltyp}/V_{S.Lmax}$	–5.5	–3.5	–1.5	dB

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DSC block						
DSC detection characteristics (–35 dB)	$V_{DSC(-35)}$		2.7	3.4	4.1	V
DSC detection characteristics (–20 dB)	$V_{DSC(-20)}$		7	8.7	9	V
DSC detection characteristics (–15 dB)	$V_{DSC(-15)}$		6.9	8.6	9	V
DSC detection characteristics (–5 dB)	$V_{DSC(-5)}$		0.26	0.33	0.40	V
DSC coring characteristics	$V_{D.CO(-5)}$		6.9	8.6	9	V
DSC limiter characteristics	$V_{D.LIM(-20)}$		2.7	3.4	4.1	V
Child picture amp. block						
Child picture amp. max. gain	G_{CAmax}		10	12	14	dB
Child picture amp. typ. gain	G_{CAtyp}		3.5	5.5	7.5	dB
Child picture amp. gain ratio	$G_{CAtyp/max}$	V_{CAtyp} / V_{CAmax}	–8.5	–6.5	–4.5	dB
Child picture amp. frequency characteristics 1	$G_{CA(20M)}$	$V_{CA(20M)}$ / 0.1 V[p-p]	9.5	11.5	13.5	dB
Child picture amp. frequency characteristics 2	$G_{CA(1M)}$	$V_{CA(1M)}$ / 0.1 V[p-p]	9.5	11.5	13.5	dB
Child picture amp. frequency characteristics 3	$G_{CA(F)}$	$V_{CA(20M)}$ / $V_{CA(1M)}$	–1	0	1	dB
VM pre-amp. block						
VM pre-amp. max. gain	G_{VMPmax}		10	12	14	dB
VM pre-amp. typ. gain	G_{VMPtyp}		3.5	5.5	7.5	dB
VM pre-amp. gain ratio	$G_{VMPtyp/max}$	V_{VMPtyp} / V_{VMPmax}	–8.5	–6.5	–4.5	dB
VM pre-amp. frequency characteristics 1	$G_{VMP(20M)}$	$V_{VMP(20M)}$ / 0.1 V[p-p]	9.5	11.5	13.5	dB
VM pre-amp. frequency characteristics 2	$G_{VMP(1M)}$	$V_{VMP(1M)}$ / 0.1 V[p-p]	9.5	11.5	13.5	dB
VM pre-amp. frequency characteristics 3	$G_{VMP(F)}$	$V_{VMP(20M)}$ / $V_{VMP(1M)}$	–1	0	1	dB
VM limiter amp. block						
CY_S switch threshold level	V_{TH5}		0.45	0.75	1.05	V
Y_S switch threshold level	V_{TH6}		0.45	0.75	1.05	V
Output DC step (CY_S)	$\Delta V_{VML(CYS)}$		–50	0	50	mV
Output DC step (Y_S)	$\Delta V_{VML(YS)}$		–50	0	50	mV
VM limiter amp. max. gain	G_{VMLmax}	V_{VMLmax} / 0.1 V[p-p]	13.5	15.5	17.5	dB
VM limiter amp. typ. gain	G_{VMLtyp}	V_{VMLtyp} / 0.1 V[p-p]	10.5	12.5	14.5	dB
VM limiter amp. gain ratio	$G_{VMLtyp/max}$	V_{VMLtyp} / V_{VMLmax}	–4.5	–2.5	– 0.5	dB
VM limiter amp. frequency characteristics 1	$G_{VML(20M)}$	$V_{VML(20M)}$ / 0.1 V[p-p]	12.5	14.5	16.5	dB
VM limiter amp. frequency characteristics 2	$G_{VML(1M)}$	$V_{VML(1M)}$ / 0.1 V[p-p]	14.5	16.5	18.5	dB

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VM limiter amp. block (continued)						
VM limiter amp. frequency characteristics 3	$G_{VML(F)}$	$V_{VML(20M)}$ / $V_{VML(1M)}$	−4	−2	0	dB
VM limiter amp. limiter characteristics 1	$G_{VML(LIMmax)}$	$V_{VML(LIM.max)}$ / 0.2 V[p-p]	14	16	18	dB
VM limiter amp. limiter characteristics 2	$G_{VML(LIMtyp)}$	$V_{VML(LIM.typ)}$ / 0.2 V[p-p]	6	8	10	dB
VM limiter amp. limiter characteristics 3	$G_{VML(LIM)}$	$V_{VML(LIM.typ)}$ / $V_{VML(LIM.max)}$	−10	−8	−6	dB
Y_S operation characteristics	$G_{VML(YS)}$	$V_{VML(YS)}$ / $V_{VML(max)}$	−36	−30	−24	dB
CY_S operation characteristics	$G_{VML(CYS)}$	$V_{VML(CYS)}$ / $V_{VML(max)}$	−36	−30	−24	dB

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
C-D.L block						
P_B signal delay time (HD)	$t_{A(PB)}$	At DL = HD	40	50	60	ns
P_B signal delay time (MUSE)	$t_{B(PB)}$	At DL = MUSE	52	65	78	ns
P_B signal delay time (NTSC1)	$t_{C(PB)}$	At DL = NTSC1	60	75	90	ns
P_B signal delay time (NTSC2)	$t_{D(PB)}$	At DL = NTSC2	72	90	108	ns
P_B signal delay time variation amount (MUSE to HD)	$t_{1(PB)}$	$t_{B(PB)} - t_{A(PB)}$	12	16	20	ns
P_B signal delay time variation amount (NTSC1 to HD)	$t_{2(PB)}$	$t_{C(PB)} - t_{A(PB)}$	20	26	32	ns
P_R signal delay time (HD)	$t_{A(PR)}$	At DL = HD	40	50	60	ns
P_R signal delay time (MUSE)	$t_{B(PR)}$	At DL = MUSE	52	65	78	ns
P_R signal delay time (NTSC1)	$t_{C(PR)}$	At DL = NTSC1	60	75	90	ns
P_R signal delay time (NTSC2)	$t_{D(PR)}$	At DL = NTSC2	72	90	108	ns
P_R signal delay time variation amount (MUSE to HD)	$t_{1(PR)}$	$t_{B(PR)} - t_{A(PR)}$	12	16	20	ns
P_R signal delay time variation amount (NTSC1 to HD)	$t_{2(PR)}$	$t_{C(PR)} - t_{A(PR)}$	20	26	32	ns
P_B, P_R delay time difference (HD)	$\Delta t_{A(C)}$	$t_{A(PB)} - t_{A(PR)}$	−6	0	6	ns
P_B, P_R delay time difference (MUSE)	$\Delta t_{B(C)}$	$t_{B(PB)} - t_{B(PR)}$	−6	0	6	ns
P_B, P_R delay time difference (NTSC1)	$\Delta t_{C(C)}$	$t_{C(PB)} - t_{C(PR)}$	−6	0	6	ns
P_B, P_R delay time difference (NTSC2)	$\Delta t_{D(C)}$	$t_{D(PB)} - t_{D(PR)}$	−6	0	6	ns

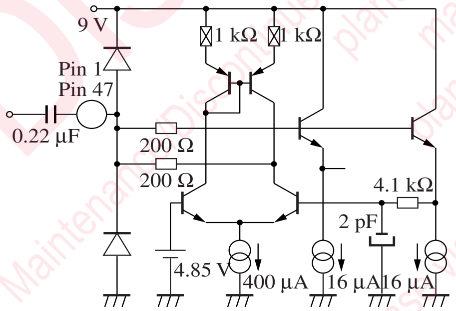
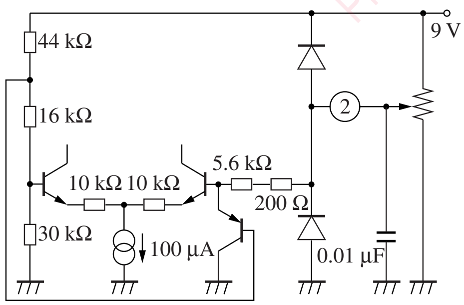
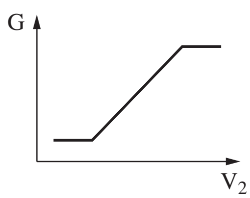
■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data

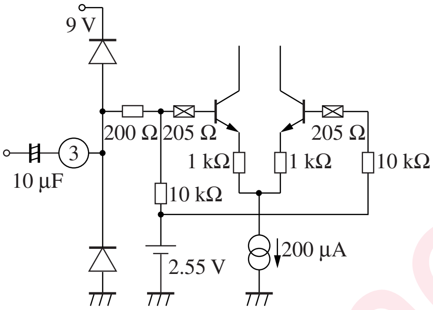
Note) The characteristics listed below are theoretical values based on the IC design and not guaranteed.

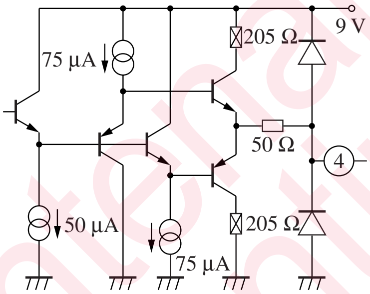
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-D.L block						
Y signal delay time (HD)	$t_{A(Y)}$	At DL = HD	40	50	60	ns
Y signal delay time (MUSE)	$t_{B(Y)}$	At DL = MUSE	52	65	78	ns
Y signal delay time (NTSC1)	$t_{C(Y)}$	At DL = NTSC1	60	75	90	ns
Y signal delay time (NTSC2)	$t_{D(Y)}$	At DL = NTSC2	72	90	108	ns
Y signal delay time variation amount (MUSE to HD)	$t_{1(Y)}$	$t_{B(Y)}-t_{A(Y)}$	12	16	20	ns
Y signal delay time variation amount (NTSC1 to HD)	$t_{2(Y)}$	$t_{C(Y)}-t_{A(Y)}$	20	26	32	ns
Y_1 signal delay time (HD)	$t_{A(Y1)}$	At DL = HD	32	40	48	ns
Y_1 signal delay time (MUSE)	$t_{B(Y1)}$	At DL = MUSE	40	50	60	ns
Y_1 signal delay time (NTSC1)	$t_{C(Y1)}$	At DL = NTSC1	44	55	66	ns
Y_1 signal delay time (NTSC2)	$t_{D(Y1)}$	At DL = NTSC2	48	60	72	ns
Y_1 signal delay time variation amount (MUSE to HD)	$t_{1(Y1)}$	$t_{B(Y1)}-t_{A(Y1)}$	4	8	12	ns
Y_1 signal delay time variation amount (NTSC1 to HD)	$t_{2(Y1)}$	$t_{C(Y1)}-t_{A(Y1)}$	10	14	18	ns

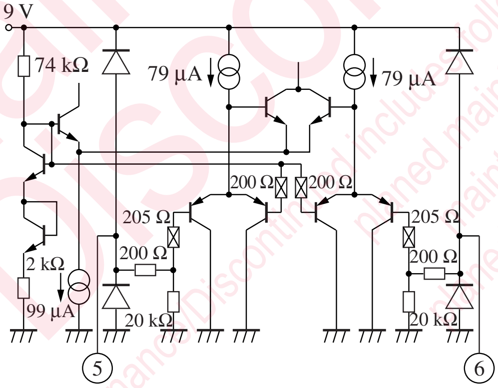
■ Terminal Equivalent Circuits

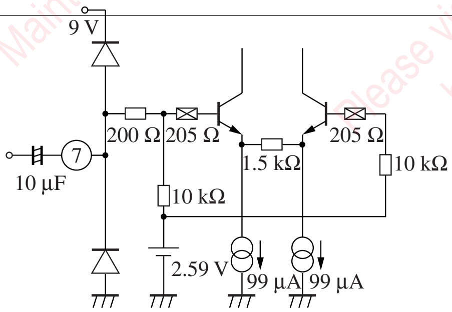
Pin No.	Equivalent circuit	Description
1		Pin 1: P_R input signal pin: Pin 47: P_B input signal pin: • Clamps input signal with clamp pulse of pin 43 • Drive with low impedance. • Recommended application method: Don't apply DC voltage directly to pin.
2		VM pre-amp. input pin: • Control voltage: typ. 3V  • Recommended application range: 0 V to V_{CC}

■ Terminal Equivalent Circuits (continued)

<table>
<tr><th>Pin No.</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>3</td><td>
</td><td>VM pre-amp. input pin:

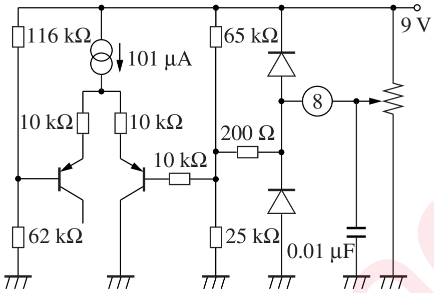
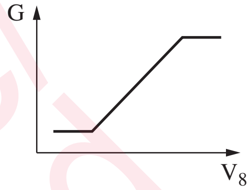
• Drive with low impedance.
• Recommended application method:
Don't apply DC voltage directly to pin.</td></tr>
<tr><td>4</td><td>
</td><td>VM pre-amp. output pin:

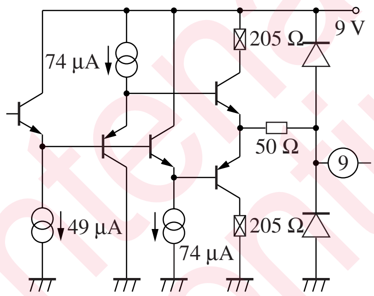
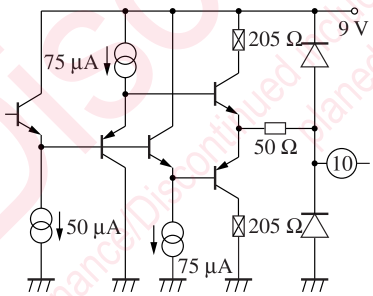
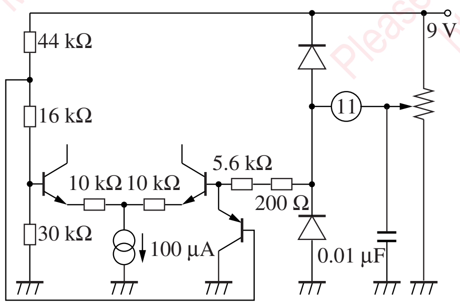
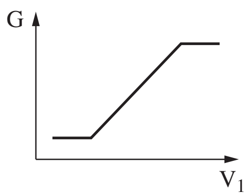
• Recommended application range:
−3.2 mA to +3.2 mA</td></tr>
<tr><td>5
6</td><td>
</td><td>Pin5: Child picture Y_S input pin:
Pin6: Y_S input pin:

• Control pin for on/off of VM limiter amp.
High: Off
Low: On (V_{TH} = 0.75 V)
• Recommended application range: 0 V to V_{CC}</td></tr>
<tr><td>7</td><td>
</td><td>VM limiter amp. input pin:

• Drive with low impedance.
• Recommended application method: Don't apply DC voltage directly to pin.</td></tr>
</table>

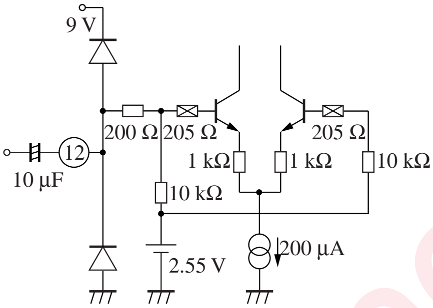
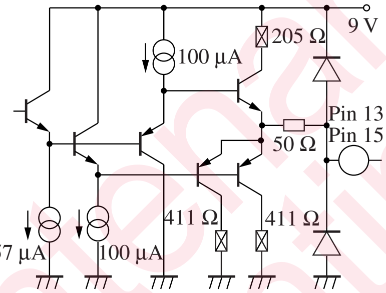
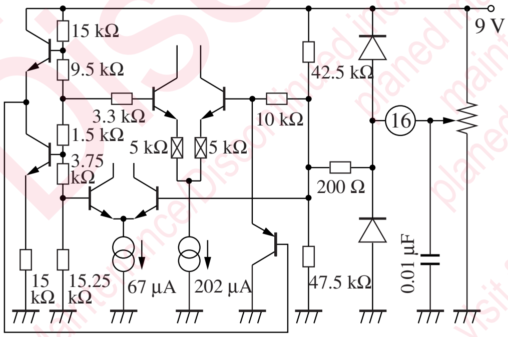
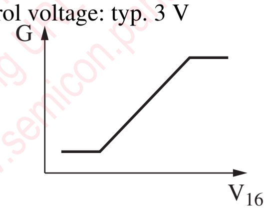
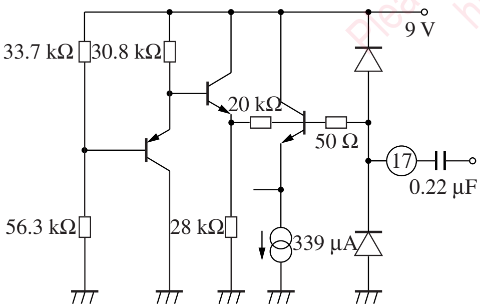
■ Terminal Equivalent Circuits (continued)

<table>
<tr><th>Pin No.</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>8</td><td>
</td><td>VM limiter amp. gain control pin:
• Control voltage: typ. 2.5 V


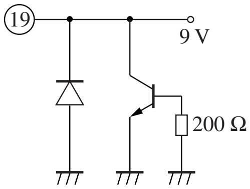
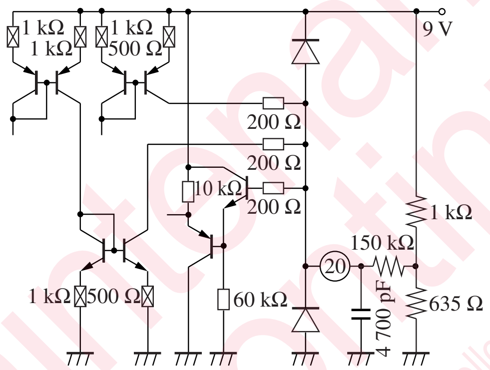
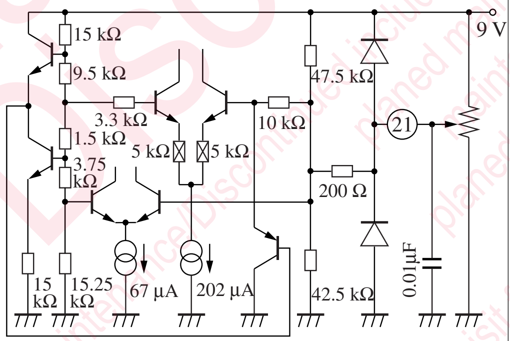
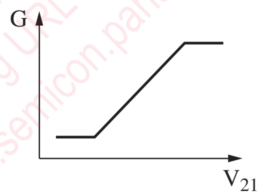
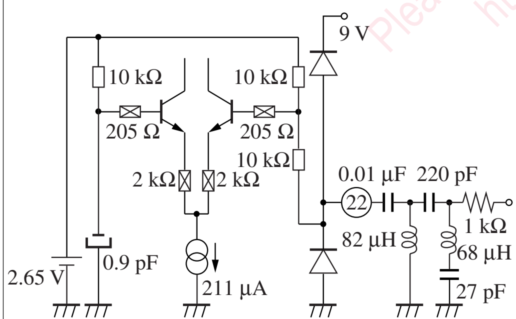
• Recommended application range: 0 V to V_{CC}</td></tr>
<tr><td>9</td><td>
</td><td>VM limiter amp. output pin:
• Recommended application range:
−3.2 mA to +3.2 mA</td></tr>
<tr><td>10</td><td>
</td><td>Child picture amp. output pin:
• Recommended application range:
−3.2 mA to +3.2 mA</td></tr>
<tr><td>11</td><td>
</td><td>Child picture amp. gain control pin:
• Control voltage: typ. 3 V


• Recommended use range: 0 V to V_{CC}</td></tr>
</table>

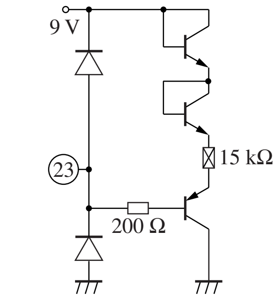
■ Terminal Equivalent Circuits (continued)

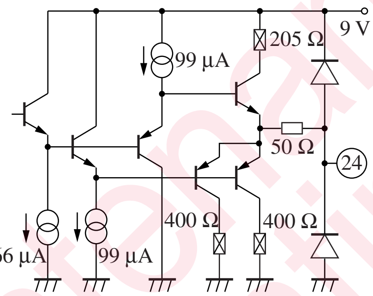
Pin No.	Equivalent circuit	Description
12		Child picture amp. input pin: • Drive with low impedance. • Recommended application method: Don't apply DC voltage directly to pin.
13		Pin 13: P_R output signal pin: Pin 15: P_B output signal pin: • Recommended application range: −1.6 mA to +1.6 mA
14	—	N.C. pin: • Keep grounded
15	Refer to pin 13	Refer to pin 13
16		DSC large signal gain control pin: • Controls gain of large signal coring amp. on DSC detection. • Control voltage: typ. 3 V  • Recommended application range: 0 V to V_{CC}
17		Primary differentiating input pin before correction: • Y1 primary differentiating signal outputted from pin 24 is inputted with capacitor coupling. • Drive with low impedance. • Recommended application method: Don't apply DC voltage directly to pin.

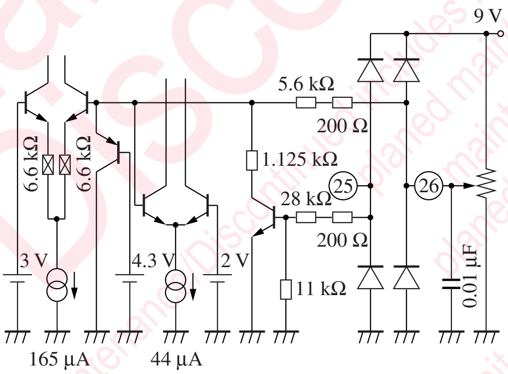
■ Terminal Equivalent Circuits (continued)

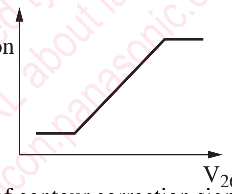
Pin No.	Equivalent circuit	Description
18	—	N.C. pin: • Keep grounded
19		Power supply pin: • Apply 9 V when use
20		DSC detection output pin: • Controls voltage of DSC. • Left diagram shows recommended external circuit. • Recommended application range: −1.6 mA to +1.6 mA
21		DSC small signal gain control pin: • Controls gain of small signal limiter amp. on DSC detection. • Control voltage: typ. 3 V  • Recommended application range: 0 V to V_{CC}
22		DSC input pin: • Y signal is inputted for DSC detection. • Left diagram shows recommended external circuit. • Recommended application method: Not apply DC voltage directly to pin.

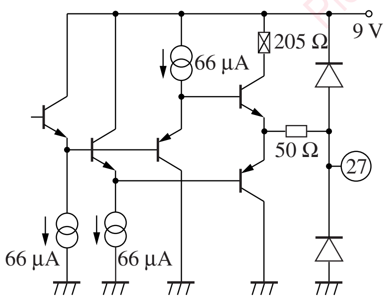
■ Terminal Equivalent Circuits (continued)

<table>
<tr><th>Pin No.</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>23</td><td>
</td><td>DSC bias pin:

• No use. Keep it connected to V_{CC}
• Recommended application range: 0 V to V_{CC}</td></tr>
<tr><td>24</td><td>
</td><td>Primary differentiating input pin before correction:

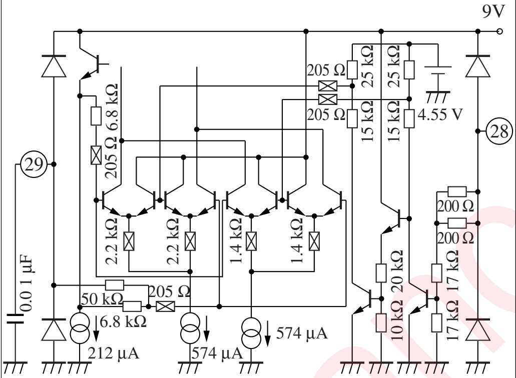
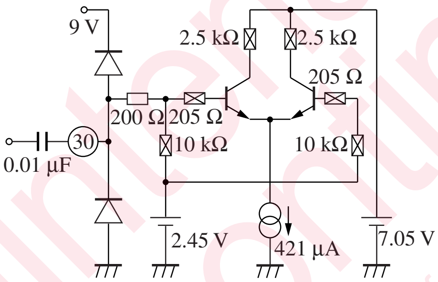
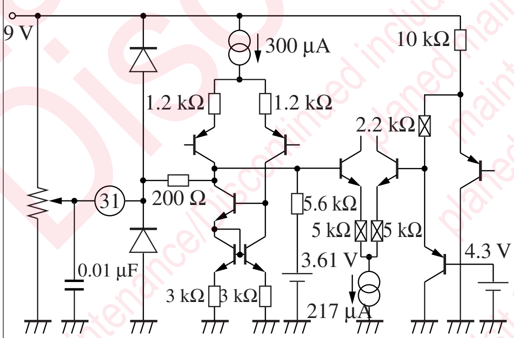
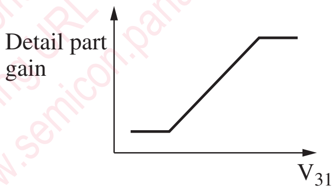
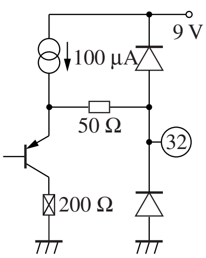
• Output Y1 primary differentiating signal which is made by Y signal inputted from pin 45.
• Recommended application range:
−1.6 mA to +1.6 mA</td></tr>
<tr><td>25
26</td><td>
</td><td>Pin 25: Sharpness mute control pin:
Pin 26: Sharpness gain control pin:

• Controls contour correction amount of pin 27 Y output signal by pin 26 voltage.
$V_{26typ} = 3$ V


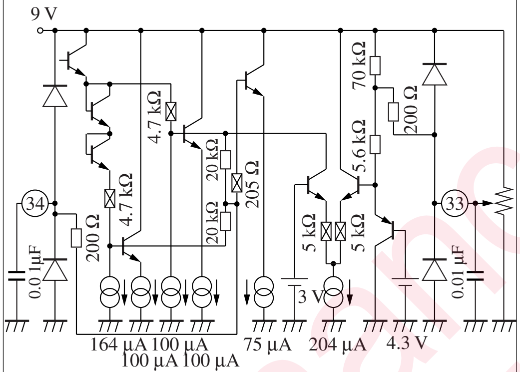
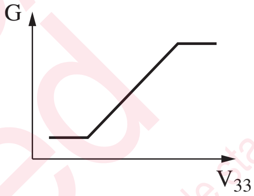
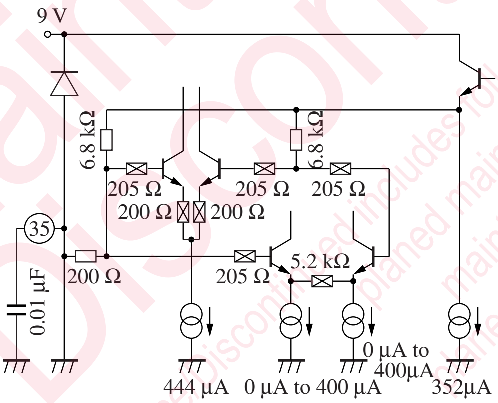
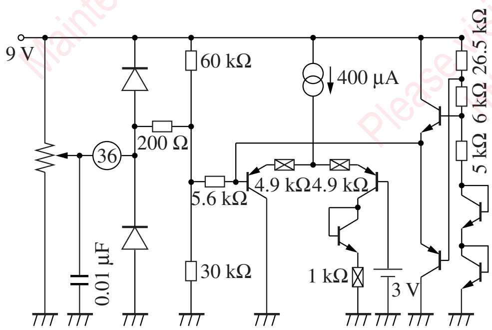
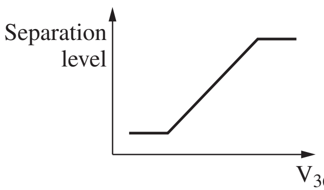
• On/off pin of contour correction signal by high/low of pin 25.
• High: Off
Low: On ($V_{TH} = 2.65$ V)
• Recommended application range: 0 V to V_{CC}</td></tr>
<tr><td>27</td><td>
</td><td>Y output pin:

• Outputs Y signal in which contour correction signal has been added on Y signal inputted from pin 45.
• Recommended application range:
−3.2 mA to +3.2 mA</td></tr>
</table>

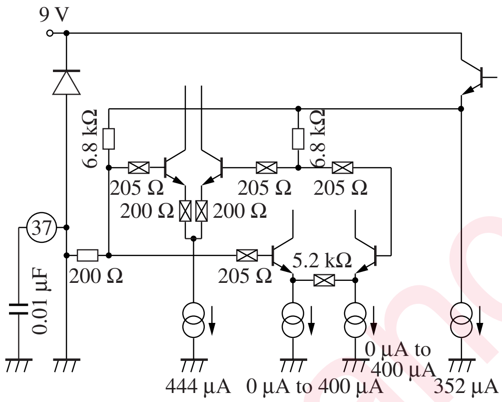
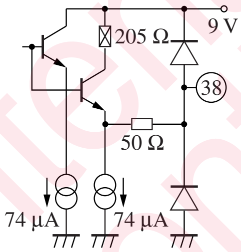
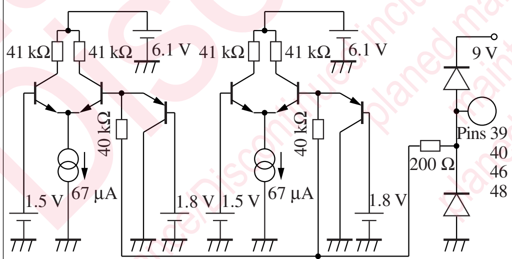
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
28 29		Pin 28: Contour part gain control pin: Pin 29: Contour part bias pin: • Contour part amp. gain can be switched in 2 steps by high/low of pin 28 voltage. • High: Contour part gain high Low: Contour part gain low (V_{TH} = 1.5 V) • Smoothes pin 29 signal by an external capacitor. • Recommended application range (pin 28): 0 V to V_{CC} • Recommended application method (pin 29): Don't apply DC voltage directly to pin.
30		Secondary differentiating input pin: • With an external circuit, differentiate the primary differential signal that has been done contour correction and which is outputted from pin 32, then input it to pin 30. • Recommended application method: Don't apply DC voltage directly to pin.
31		Detail part gain control pin: • Controls gain of small signal detail part amp. by pin 31 voltage. V_{31typ} = 3 V  • Recommended application range: 0 V to V_{CC}
32		Primary differentiating output after correction pin: • Outputs a primary differentiated signal as a signal for contour part edge switching. • Recommended application range: −1.6 mA to +1.6 mA

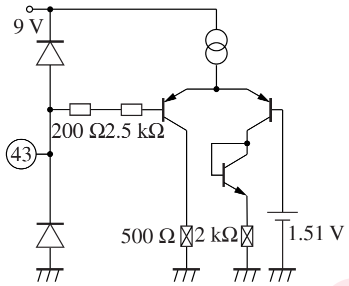
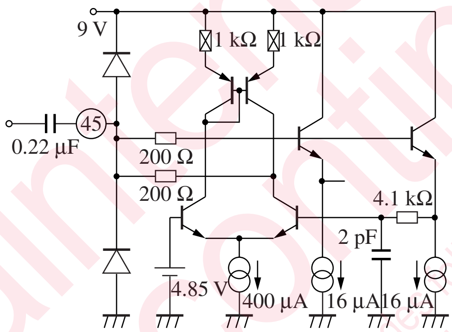
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
33 34		Pin 33: Detail part coring control pin: Pin 34: Detail part coring bias pin: • Controls gain of detail part coring amp. by pin 33 voltage. $V_{33typ} = 3$ V  • Smoothes pin 34 signal with an external capacitor. • Recommended application range (pin 33): 0 V to V_{CC} • Recommended application method (pin 34): Don't apply DC voltage directly to pin.
35		Differentiating signal bias 1 pin: • Makes a necessary bias by smoothing with an external capacitor to run a contour correction for the primary differentiating signal inputted from pin 17. • Recommended application method: Don't apply DC voltage directly to pin.
36		Contour part and detail part separation level control pin: • Controls separation level of contour part (large signal) and detail part (small signal) by pin 36 voltage $V_{36typ} = 3$ V  • Recommended application range: 0 V to V_{CC}

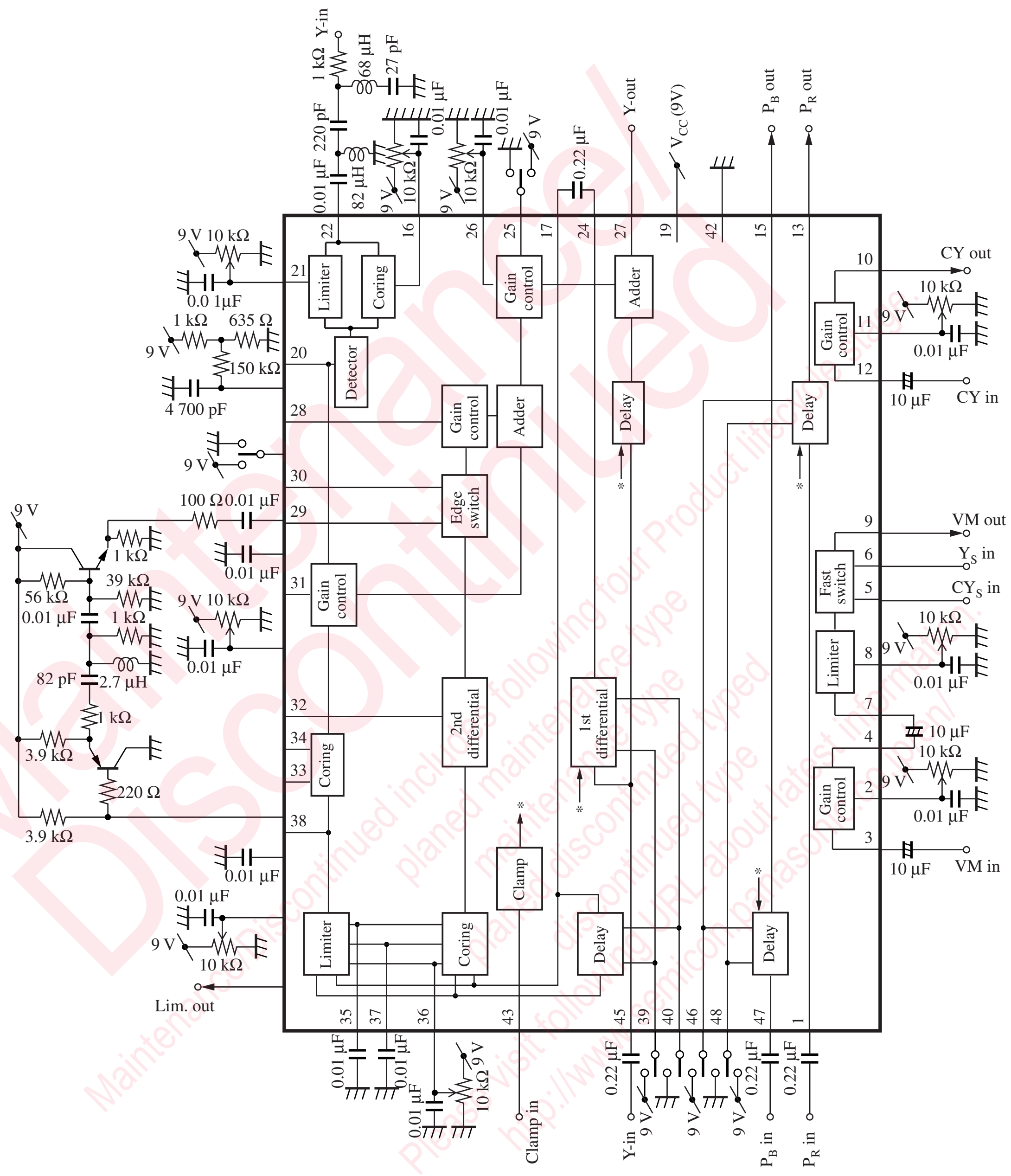
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
37		Differentiating signal bias 2 pin: • Necessary bias is made by an smoothing external capacitor in order to correct contour of primary differentiating signal inputted from Pin17 • Recommended application method: Don't apply DC voltage directly to pin.
38		Detail part limiter output pin: • Outputs detail part limiter signal • Recommended application range: −1.6 mA to +1.6 mA
39 40		Pin 39: Y delay line changeover switch-1 pin: Pin 40: Y delay line changeover switch-2 pin: Pin 46: C delay line changeover switch-1 pin: Pin 48: C delay line changeover switch-2 pin: • Correction amount of Y, C delay line are switched by high/low of each pin voltage. (V_{TH} = 1.5 V) • Pin 39, pin 46 High: Off, low: +10 ns • Pin 40, pin 48 High: Off, low: +20 ns • Recommended application range: 0 V to V_{CC}
41	—	N.C. pin: • Keep grounded
42	—	GND pin:

■ Terminal Equivalent Circuits (continued)

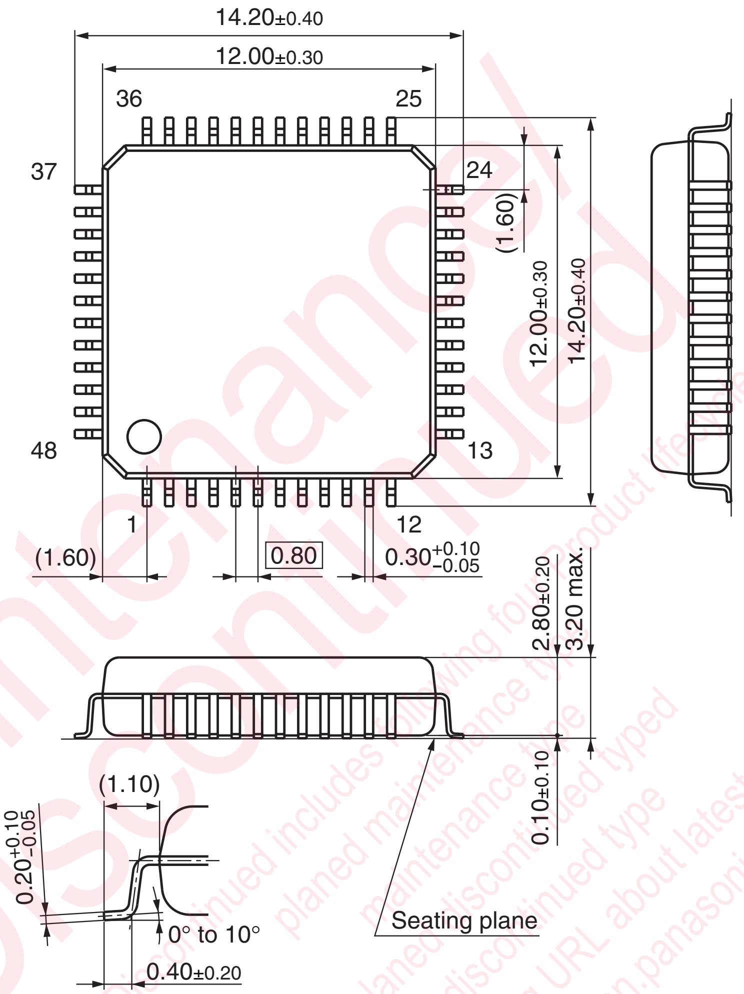
Pin No.	Equivalent circuit	Description
43		Clamp pulse input pin: • Clamps inputted signal from each pin of pin 45, pin 47, pin 1 (V_{TH} = 1.5 V) • High: Clamp on • Low: Clamp off • Recommended pulse width (clamp on period) NTSC: 2.5 µs HD: 1.0 µs • Recommended application range: 0 V to V_{CC}
44	—	N.C. pin: • Keep grounded
45		Y input signal pin: • Clamps input signal with Pin43 clamp pulse • Drive with low impedance • Recommended application method: Don't apply DC voltage directly to pin.
46	Refer to pin 39	Refer to pin 39
47	Refer to pin 1	Refer to pin 1
48	Refer to pin 39	Refer to pin 39

■ Application Circuit Example (Basic Circuit)



■ New Package Dimensions (Unit: mm)

• QFH048-P-1212C (Lead-free package)



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