Panasonic

AN32182A

http://www.semicon.panasonic.co.jp/en/

6 x 6 Dots Matrix LED Driver IC

FEATURES

- 6 × 6 LED Matrix Driver
  (Total LED that can be driven = 36)
- LED Selectable Maximum Current
- LED Music Synchronizing function
- I²C interface (Standard Mode, Fast Mode and Fast Mode Plus)
  (4 Slave address selectable)
- 20 pin Plastic Quad Flat Non-leaded Package (QFN Type)

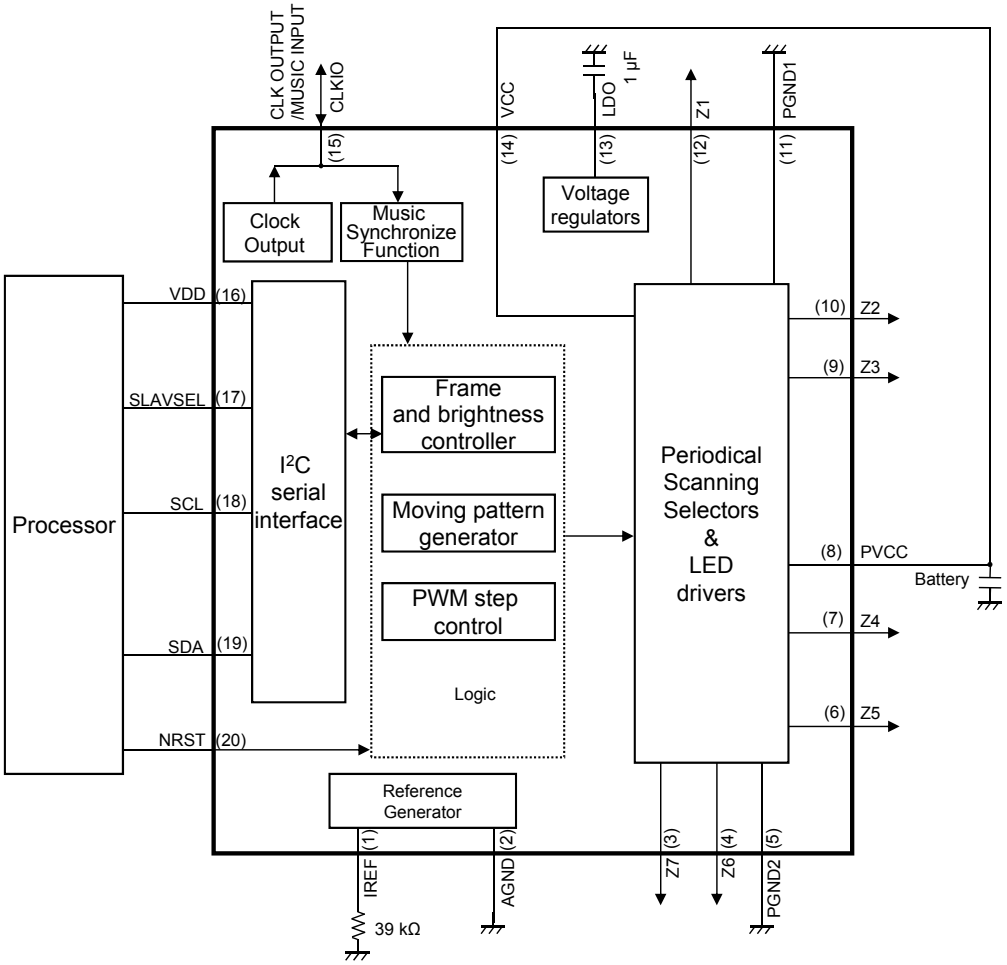
DESCRIPTION

AN32182A is a 36 dots Matrix LED driver.
It can drive up to 12 RGB LEDs.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note:
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

Established : 2011-07-29
Revised : 2014-01-22

CONTENTS

Established : 2011-07-29
Revised : 2014-01-22

ORDERING INFORMATION

Order Number	Feature	Package	Output Supply
AN32182A-VB	LED Driver for Illumination	20 pin QFN	Emboss Taping

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VCC_{MAX}	6.0	V	*1
	VDD_{MAX}	6.0	V	*1
Operating ambience temperature	T_{opr}	– 30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	$V_{SLAVSEL}$, V_{SCL}, V_{SDA}, V_{CLKIO}, V_{NRST}	– 0.3 to 6.0	V	—
Output Voltage Range	V_{IREF}, V_{LDO}, V_{CLKIO}, V_{Z1}, V_{Z2}, V_{Z3}, V_{Z4}, V_{Z5}, V_{Z6}, V_{Z7}	– 0.3 to 6.0	V	—
ESD	HBM	2.0	kV	—

Note: This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1: VCC_{MAX} = VCC, VDD_{MAX} = VDD.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for operating ambient temperature, operating junction temperature and storage temperature, all ratings are for Ta = 25°C.

POWER DISSIPATION RATING

Package	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
20 pin Plastic Quad Flat Non-leaded Package (QFN Type)	189.2 °C /W	0.529 W	0.212 W

Note: For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

Established : 2011-07-29
Revised : 2014-01-22

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	V_{CC}	3.1	3.6	5.5	V	—
	V_{DD}	1.7	1.85	5.5	V	—
Input Voltage Range	$V_{SLAVSEL}$, V_{SCL}, V_{SDA}, V_{CLKIO}	– 0.3	—	V_{DD} + 0.3	V	*1
	V_{NRST}	– 0.3	—	V_{CC} + 0.3	V	*1
Output Voltage Range	V_{IREF}, V_{LDO}, V_{CLKIO}, V_{Z1}, V_{Z2}, V_{Z3}, V_{Z4}, V_{Z5}, V_{Z6}, V_{Z7}	– 0.3	—	V_{CC} + 0.3	V	*1

Note: Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for GND.
V_{CC} is voltage for VCC. V_{DD} is voltage for VDD.
Do not apply external currents or voltages to any pin not specifically mentioned.
*1 : (V_{CC} + 0.3) V must not exceed 6 V. (V_{DD} + 0.3) V must not exceed 6 V.

Established : 2011-07-29
Revised : 2014-01-22

ELECTRICAL CHARACTERISTICS

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Notes: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Circuit Current							
Circuit Current (1) OFF Mode	I_{CC1}	NRST = 0 V	—	0	1	µA	—
Circuit Current (2) OFF Mode	I_{CC2}	NRST = 3.6V	—	250	500	µA	—
Internal Oscillator							
Oscillation Frequency	FDC1	V_{CC} = 3.6 V	1.92	2.40	2.88	MHz	—
SCAN Switch							
Switch On Resistance	RSCAN	V_{CC} = 3.6 V $I_{Z1\sim Z7}$ = – 20 mA	—	1.5	3	Ω	—
Constant Voltage Source (LDO)							
Output voltage (1)	V_{L1}	I_{LDO} = – 10 µA	2.75	2.85	2.95	V	—
Output voltage (2)	V_{L2}	I_{LDO} = – 15 mA	2.75	2.85	2.95	V	—
CLKIO							
High Level Input Voltage Range	V_{IH1}	High Level Acknowledged Voltage (At External CLK Input Mode)	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Input Voltage Range	V_{IL1}	Low Level Acknowledged Voltage (At External CLK Input Mode)	– 0.3	—	0.3 × V_{DD}	V	—
High Level Output Voltage	V_{OH1}	I_{CLKIO} = – 1 mA (At Internal CLK Output Mode)	0.8 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Output Voltage	V_{OL1}	I_{CLKIO} = 1 mA (At Internal CLK Output Mode)	– 0.3	—	0.2 × V_{DD}	V	—
High Level input Current	I_{IH1}	V_{CC} = 5.5 V V_{CLKIO} = 5.5 V	– 1	0	1	µA	—
Low Level input Current	I_{IL1}	V_{CC} = 5.5 V V_{CLKIO} = 0 V	– 1	0	1	µA	—

Established : 2011-07-29
Revised : 2014-01-22

ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Notes: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Constant Current Source (Matrix LED)							
Output Current (1)	I_{MX1}	LED Current Setting = 20 mA I_{MAX} = [011], BRTXX = [1010] $V_{Z1\sim Z7}$ = 1 V	19	20	21	mA	*1
DAC Current Step	DACSTEP	DAC Constant Current Mode LED Current Setting = 20 mA I_{MAX} = [011], BRTXX = [1010] $V_{Z1\sim Z7}$ = 1 V, IDAC1 = $I_{Z1\sim Z7}$ LED Current Setting = 22 mA I_{MAX} = [011], BRTXX = [1011] $V_{Z1\sim Z7}$ = 1 V, IDAC2 = $I_{Z1\sim Z7}$ DACSTEP = IDAC2 – IDAC1	0	2	4	mA	*2
OFF Mode Leak Current1	I_{MXOFF1}	V_{CC} = 5.5 V, V_{DD} = 5.5 V MTXON = 0 $V_{Z1\sim Z7}$ = 5.5 V	– 1	—	1	µA	*3
OFF Mode Leak Current2	I_{MXOFF2}	V_{CC} = 5.5 V, V_{DD} = 5.5 V MTXON = 0 $V_{Z1\sim Z7}$ = 0 V	– 1	—	1	µA	*3
Channel Difference	I_{MXCH}	LED Current Setting = 20 mA I_{MAX} = [011], BRTXX = [1010] Difference of Z1 to 7 current from the average current value	– 5	—	5	%	—
Voltage at which LED driver can keep constant current value							
LED Driver Voltage	V_{LD2}	LED Current Setting = 20 mA I_{MAX} = [011], BRTXX = [1010] Voltage at which LED Current change within ±5% compared with LED Current of pin voltage = 0.5 V.	0.4	—	—	V	—

Note: * 1: This is allowable value when recommended parts (ERJ2RHD393X) are used for the terminal IREF.

* 2: Current step for individual channels (Z1~Z7).

* 3: Please refer to page 18 for more information on the setting.

Established : 2011-07-29
Revised : 2014-01-22

ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Notes: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SLAVSEL							
High Level Input Voltage Range	V_{IH2}	High Level Acknowledged Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Input Voltage Range	V_{IL2}	Low Level Acknowledged Voltage	– 0.3	—	0.3 × V_{DD}	V	—
High Level Input Current	I_{IH2}	V_{CC} = 5.5 V $V_{SLAVSEL}$ = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	I_{IL2}	V_{CC} = 5.5 V $V_{SLAVSEL}$ = 0 V	– 1	0	1	µA	—
NRST							
High Level Input Voltage Range	V_{IH3}	High Level Acknowledged Voltage	1.5	—	V_{CC} + 0.3	V	—
Low Level Input Voltage Range	V_{IL3}	Low Level Acknowledged Voltage	– 0.3	—	0.6	V	—
High Level Input Current	I_{IH3}	V_{CC} = 5.5 V V_{NRST} = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	I_{IL3}	V_{CC} = 5.5 V V_{NRST} = 0 V	– 1	0	1	µA	—
I²C bus (Internal I/O stage characteristics)							
Low-level input voltage	V_{IL}	Voltage which recognized that SDA and SCL are Low-level	–0.5	—	0.3 × V_{DD}	V	*4
High-level input voltage	V_{IH}	Voltage which recognized that SDA and SCL are High-level	0.7 × V_{DD}	—	VDD_{MAX} + 0.5	V	*4
Low-level output voltage 1	V_{OL1}	V_{DD} > 2 V I_{SDA} = 3 mA	0	—	0.4	V	—
Low-level output voltage 2	V_{OL2}	V_{DD} < 2 V I_{SDA} = 3 mA	0	—	0.2 × V_{DD}	V	—
Low-level output current	I_{OL}	V_{SDA} = 0.4 V	20	—	—	mA	—
Input current each I/O pin	I_i	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{SCL}, V_{SDA} = 0.1 VDD_{MAX} to 0.9 VDD_{MAX}	–10	0	10	µA	—
SCL clock frequency	f_{SCL}	—	0	—	1 000	kHz	—

Note: VDD_{Max} refers to the maximum operating supply voltage of V_{DD}.

*4 : The input threshold voltage of I²C bus (Vth) is linked to V_{DD} (I²C bus I/O stage supply voltage).
In case the pull-up voltage is not V_{DD}, the threshold voltage (Vth) is fixed to ((V_{DD} / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.
In this case, pay attention to Low-level (max.) value (V_{ILMAX}).
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (V_{DD}).

Established : 2011-07-29
Revised : 2014-01-22

ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Notes: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
TSD (Thermal shutdown protection circuit)							
Detection temperature	Tdet	Temperature which Constant current circuit, and Matrix SW turn off.	—	150	—	°C	*5 *6
Constant Voltage Source (LDO)							
Ripple rejection ratio (1)	PSL11	V_{CC} = 3.6 V + 0.3 V [p-p] f = 1 kHz I_{LDO} = – 15 mA PSL11 = 20 log (acV_{LDO} / 0.3)	—	– 50	—	dB	*6
Ripple rejection ratio (2)	PSL12	V_{CC} = 3.6 V + 0.3 V[p-p] f = 10 kHz I_{LDO} = – 15 mA PSL12 = 20 log (acV_{LDO} / 0.3)	—	– 40	—	dB	*6
Short-circuit protection current	IPT1	V_{LDO} = 0 V	—	40	—	mA	*6
I²C bus (Internal I/O stage characteristics) (Continued)							
Hysteresis of Schmitt trigger input 1	V_{hys1}	V_{DD} > 2 V, Hysteresis of SDA, SCL	0.05 × V_{DD}	—	—	V	*7 *8
Hysteresis of Schmitt trigger input 2	V_{hys2}	V_{DD} < 2 V, Hysteresis of SDA, SCL	0.1 × V_{DD}	—	—	V	*7 *8
Output fall time from V_{IHmin} to V_{ILmax}	t_{of}	Bus capacitance :10pF to 550pF $I_P \leq$ 20 mA (V_{OLmax} = 0.4 V) I_P : Max. sink current	—	—	120	ns	*7 *8
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	—	0	—	50	ns	*7 *8
Capacitance for each I/O pin	C_i	—	—	—	10	pF	*7 *8

Note: *5 : Constant current circuit, and Matrix SW turn off and IC reset when TSD operates.

*6 : Typical Design Value

*7 : The timing of Fast-mode Plus devices in I²C-bus is specified in page 10. All values referred to V_{IHMIN} and V_{ILMAX} level.

*8 : These are values checked by design but not production tested.

Established : 2011-07-29
Revised : 2014-01-22

ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Notes: T_a = 25°C±2°C unless otherwise noted.

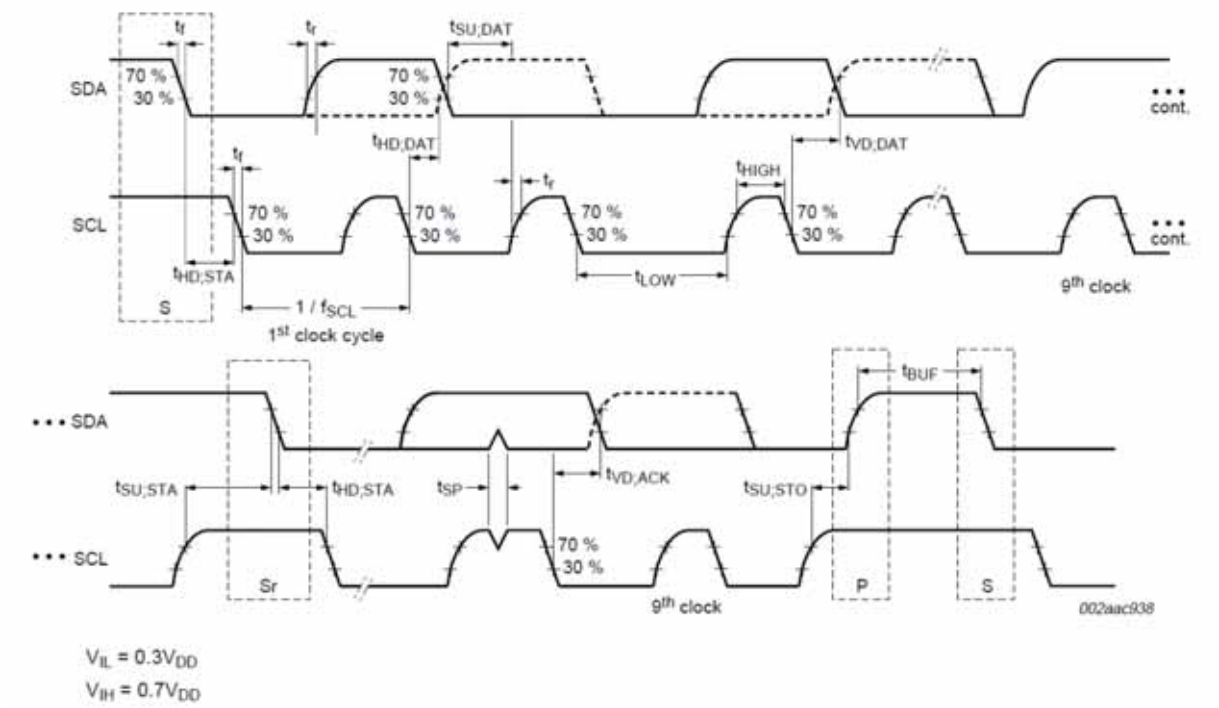
Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Bus line specifications) (Continue)							
Hold time (repeated) START condition	$t_{HD:STA}$	The first clock pulse is generated after $t_{HD:STA.}$	0.26	—	—	µs	*7 *8
Low period of the SCL clock	t_{LOW}	—	0.5	—	—	µs	*7 *8
High period of the SCL clock	t_{HIGH}	—	0.26	—	—	µs	*7 *8
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.26	—	—	µs	*7 *8
Data hold time	$t_{HD:DAT}$	—	0	—	—	µs	*7 *8
Data set-up time	$t_{SU:DAT}$	—	50	—	—	ns	*7 *8
Rise time of both SDA and SCL signals	t_r	—	—	—	120	ns	*7 *8
Fall time of both SDA and SCL signals	t_f	—	—	—	120	ns	*7 *8
Set-up time of STOP condition	$t_{SU:STO}$	—	0.26	—	—	µs	*7 *8
Bus free time between STOP and START condition	t_{BUF}	—	0.5	—	—	µs	*7 *8
Capacitive load for each bus line	C_b	—	—	—	550	pF	*7 *8
Data valid time	$t_{VD:DAT}$	—	—	—	0.45	µs	*7 *8
Data valid acknowledge	$t_{VD:ACK}$	—	—	—	0.45	µs	*7 *8
Noise margin at the Low-level for each connected device	V_{nL}	—	0.1 × V_{DD}	—	—	V	*7 *8
Noise margin at the High-level for each connected device	V_{nH}	—	0.2 × V_{DD}	—	—	V	*7 *8

Note: *7 : The timing of Fast-mode Plus devices in I²C-bus is specified in page 10. All values referred to V_{IHMIN} and V_{ILMAX} level.

*8 : These are values checked by design but not production tested.

Established : 2011-07-29
Revised : 2014-01-22

ELECTRICAL CHARACTERISTICS (Continued)

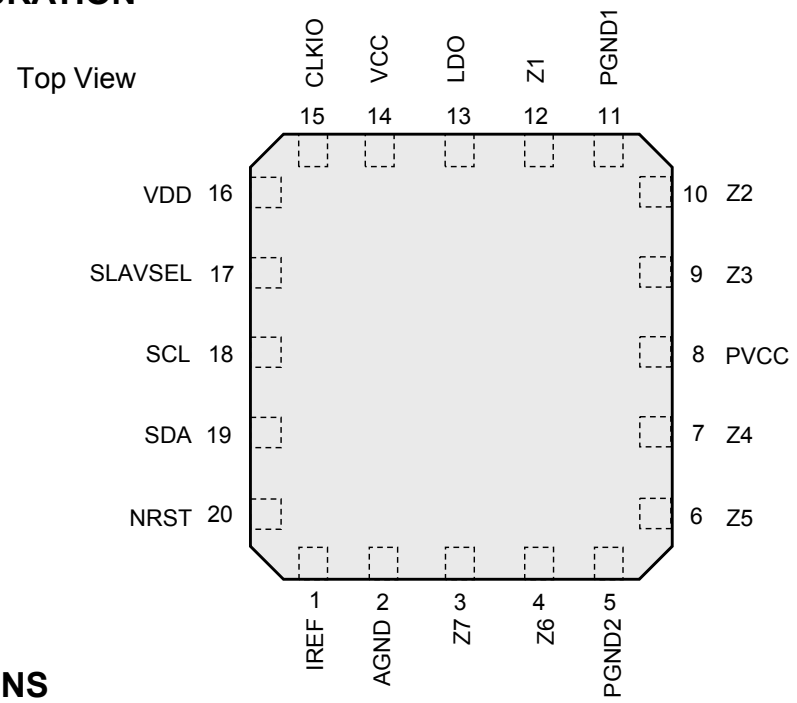


$V_{IL} = 0.3V_{DD}$
$V_{IH} = 0.7V_{DD}$

S : START condition
Sr : Repetitive START condition
P : STOP condition

Established : 2011-07-29
Revised : 2014-01-22

PIN CONFIGURATION

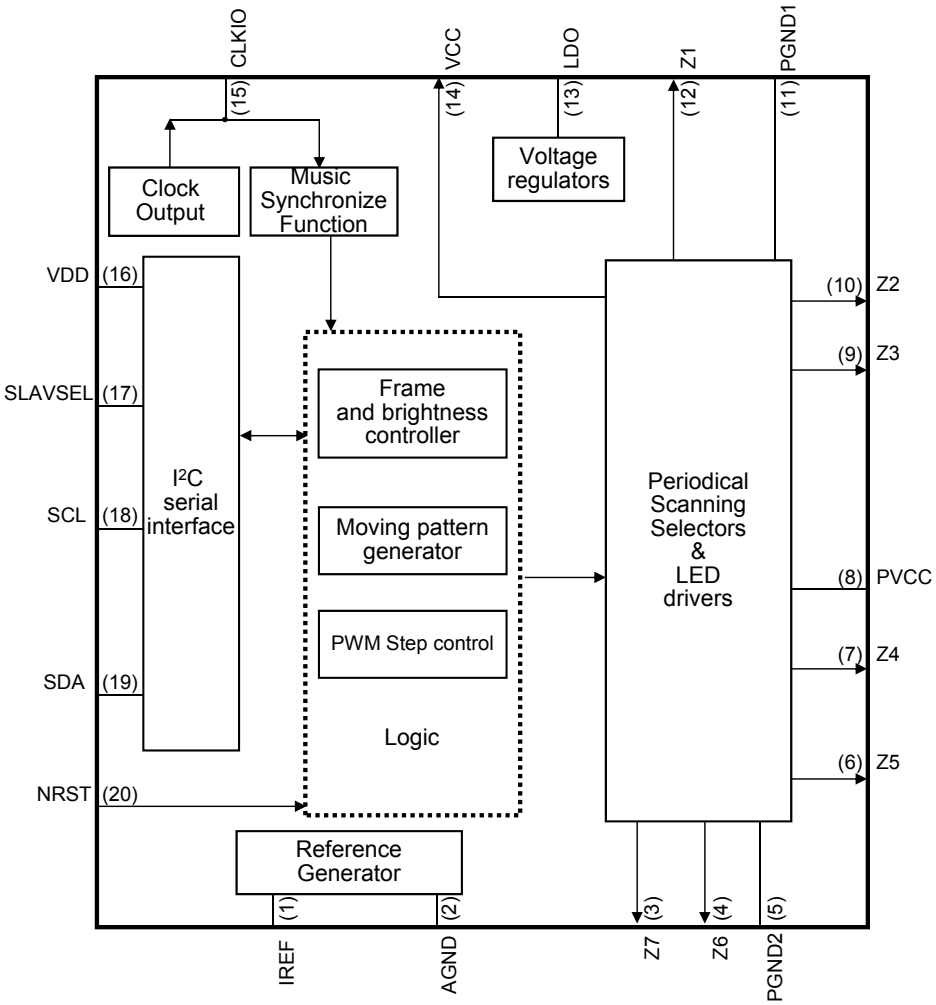


PIN FUNCTIONS

Pin No.	Pin name	Type	Description	Pin processing at unused
1	IREF	Output	Resistor connection pin for constant current setup	(Required pin)
2	AGND	Ground	Ground pin	(Required pin)
3	Z7	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
4	Z6	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
5 11	PGND2 PGND1	Ground	Power Ground pin	(Required pin)
6	Z5	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
7	Z4	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
8	PVCC	Power supply	Power supply for matrix driver	Battery or External power supply
9	Z3	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
10	Z2	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
12	Z1	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
13	LDO	Output	LDO output pin	(Required pin)
14	VCC	Power supply	Power supply for Internal reference circuit	Battery or External power supply
15	CLKIO	Input/Output	Reference clock input output / Music Input pin	Open
16	VDD	Power supply	Power supply for I^2C interface	(Required pin)
17	SLAVSEL	Input	Slave address selection pin for I^2C interface	(Required pin)
18	SCL	Input	Clock input pin for I^2C interface	(Required pin)
19	SDA	Input/Output	Data input / output pin for I^2C interface	(Required pin)
20	NRST	Input	Reset input pin	(Required pin)

Established : 2011-07-29
Revised : 2014-01-22

FUNCTIONAL BLOCK DIAGRAM



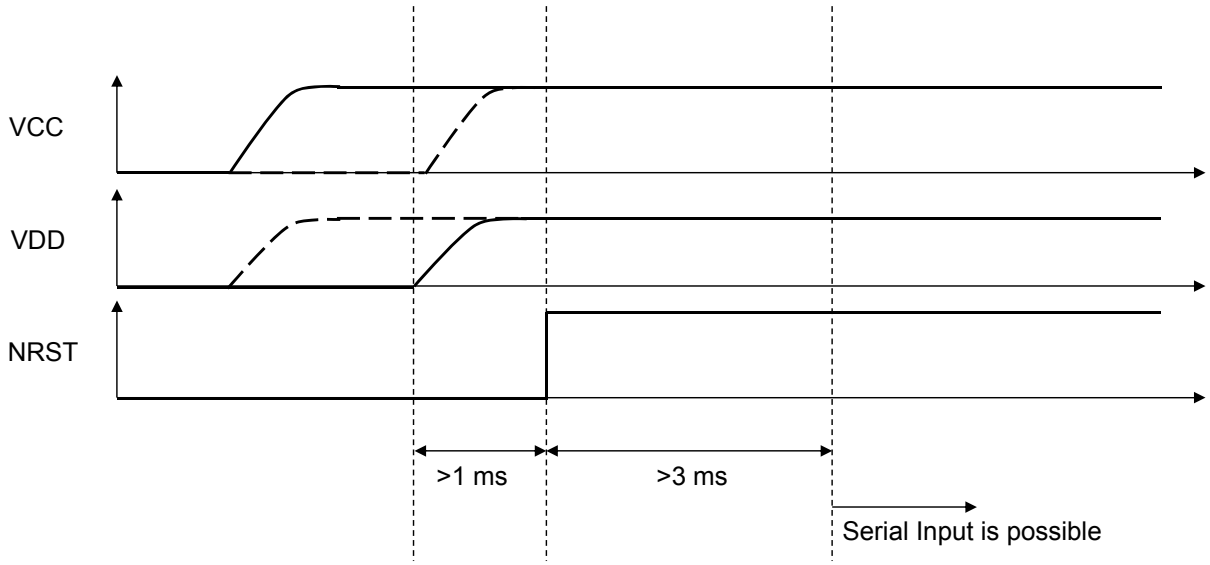
Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION

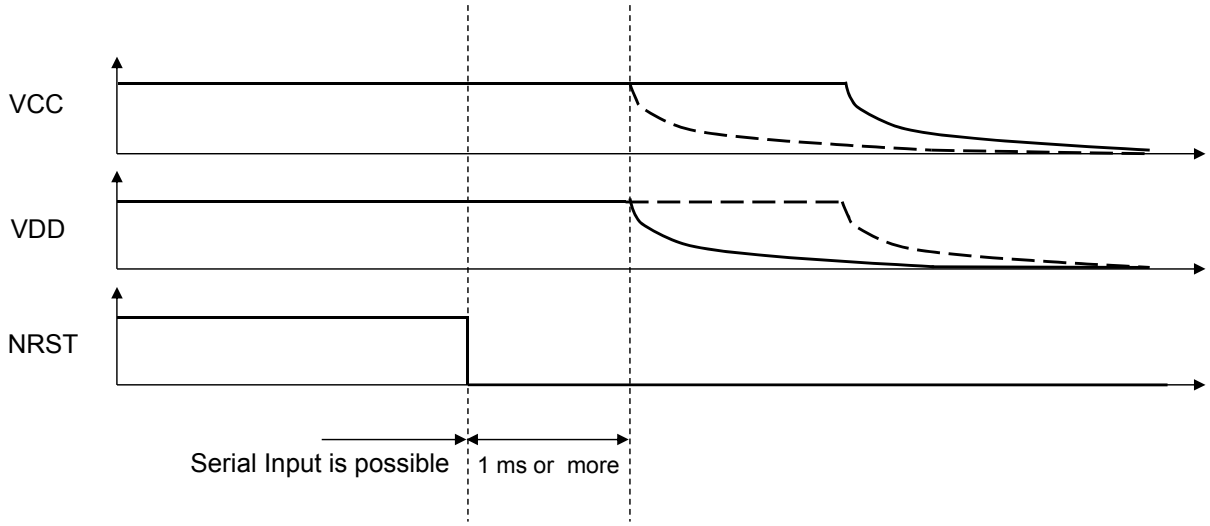
1. Power Supply Sequence

1.1 Power ON



Note: For the Startup Timing of VCC and VDD, it is possible to be changed.

1.2 Power OFF



Note: For the Shut down Timing of VCC and VDD, it is possible to be changed.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

2. Register Map

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
00h											
01h	RST	00h	W	--	--	--	--	--	--	RAMRST	SRST
02h	POWERCNT	00h	R/W	--	--	--	--	--	--	--	OSCEN
03h	reserved	--	--	--	--	--	--	--	--	--	--
04h	OPTION	00h	R/W	--	--	--	--	ZPDEN	MLDACT	CLKOUT	EXTCLK
05h	MTXON	1Eh	R/W	--	--	--	IMAX Reserved	IMAX[2:0]			MTXON
06h	PWMEN1	00h	R/W	--	--	PWMA6	PWMA5	PWMA4	PWMA3	PWMA2	PWMA1
07h	PWMEN2	00h	R/W	--	--	PWMB6	PWMB5	PWMB4	PWMB3	PWMB2	PWMB1
08h	PWMEN3	00h	R/W	--	--	PWMC6	PWMC5	PWMC4	PWMC3	PWMC2	PWMC1
09h	PWMEN4	00h	R/W	--	--	PWMD6	PWMD5	PWMD4	PWMD3	PWMD2	PWMD1
0Ah	PWMEN5	00h	R/W	--	--	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1
0Bh	PWMEN6	00h	R/W	--	--	PWMF6	PWMF5	PWMF4	PWMF3	PWMF2	PWMF1
0Ch	MLDEN1	00h	R/W	--	--	MLDA6	MLDA5	MLDA4	MLDA3	MLDA2	MLDA1
0Dh	MLDEN2	00h	R/W	--	--	MLDB6	MLDB5	MLDB4	MLDB3	MLDB2	MLDB1
0Eh	MLDEN3	00h	R/W	--	--	MLDC6	MLDC5	MLDC4	MLDC3	MLDC2	MLDC1
0Fh	MLDEN4	00h	R/W	--	--	MLDD6	MLDD5	MLDD4	MLDD3	MLDD2	MLDD1
10h	MLDEN5	00h	R/W	--	--	MLDE6	MLDE5	MLDE4	MLDE3	MLDE2	MLDE1
11h	MLDEN6	00h	R/W	--	--	MLDF6	MLDF5	MLDF4	MLDF3	MLDF2	MLDF1
12h	MDLMODE1	00h	R/W	--	--	--	--	GRP6_3	GRP6_2	GRP6_1	GRP6_0
13h	MLDCOM	01h	R/W	--	--	--	--	--	MLDCOM[2:0]		
14h	THOLD	00h	R/W	THOLD[7:0]							
15h	CONSTX	00h	R/W	--	X7	X6	X5	X4	X3	X2	X1
16h	CONSTY	00h	R/W	--	--	Y6	Y5	Y4	Y3	Y2	Y1
17h	YMSK	00h	R/W	--	--	Y6MSK	Y5MSK	Y4MSK	Y3MSK	Y2MSK	Y1MSK
18h	SLPTIME	A0h	R/W	SCANSET[2:0]			FADTIM	SLOPEEXTL[1:0]		SLOPEEXTH[1:0]	
19h	DTA1	00h	R/W	DTA1[7:0]							
1Ah	DTA2	00h	R/W	DTA2[7:0]							
1Bh	DTA3	00h	R/W	DTA3[7:0]							
1Ch	DTA4	00h	R/W	DTA4[7:0]							
1Dh	DTA5	00h	R/W	DTA5[7:0]							
1Eh	DTA6	00h	R/W	DTA6[7:0]							

Note: "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used.
For data bits indicated by "--" in other registers except from "reversed" registers, will return "zero" value if these bits are read. Writing to these bits will be ignored.
IMAX Reserved will give default value [1].

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
1Fh	DTB1	00h	R/W	DTB1[7:0]							
20h	DTB2	00h	R/W	DTB2[7:0]							
21h	DTB3	00h	R/W	DTB3[7:0]							
22h	DTB4	00h	R/W	DTB4[7:0]							
23h	DTB5	00h	R/W	DTB5[7:0]							
24h	DTB6	00h	R/W	DTB6[7:0]							
25h	DTC1	00h	R/W	DTC1[7:0]							
26h	DTC2	00h	R/W	DTC2[7:0]							
27h	DTC3	00h	R/W	DTC3[7:0]							
28h	DTC4	00h	R/W	DTC4[7:0]							
29h	DTC5	00h	R/W	DTC5[7:0]							
2Ah	DTC6	00h	R/W	DTC6[7:0]							
2Bh	DTD1	00h	R/W	DTD1[7:0]							
2Ch	DTD2	00h	R/W	DTD2[7:0]							
2Dh	DTD3	00h	R/W	DTD3[7:0]							
2Eh	DTD4	00h	R/W	DTD4[7:0]							
2Fh	DTD5	00h	R/W	DTD5[7:0]							
30h	DTD6	00h	R/W	DTD6[7:0]							
31h	DTE1	00h	R/W	DTE1[7:0]							
32h	DTE2	00h	R/W	DTE2[7:0]							
33h	DTE3	00h	R/W	DTE3[7:0]							
34h	DTE4	00h	R/W	DTE4[7:0]							
35h	DTE5	00h	R/W	DTE5[7:0]							
36h	DTE6	00h	R/W	DTE6[7:0]							
37h	DTF1	00h	R/W	DTF1[7:0]							
38h	DTF2	00h	R/W	DTF2[7:0]							
39h	DTF3	00h	R/W	DTF3[7:0]							
3Ah	DTF4	00h	R/W	DTF4[7:0]							
3Bh	DTF5	00h	R/W	DTF5[7:0]							
3Ch	DTF6	00h	R/W	DTF6[7:0]							
3Dh	A1	00h	R/W	BRTA1[3:0]				--	SDTA1[2:0]		
3Eh	A2	00h	R/W	BRTA2[3:0]				--	SDTA2[2:0]		
3Fh	A3	00h	R/W	BRTA3[3:0]				--	SDTA3[2:0]		
40h	A4	00h	R/W	BRTA4[3:0]				--	SDTA4[2:0]		

Note: Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
Writing to these bits will be ignored.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
41h	A5	00h	R/W	BRTA5[3:0]				--	SDTA5[2:0]		
42h	A6	00h	R/W	BRTA6[3:0]				--	SDTA6[2:0]		
43h	B1	00h	R/W	BRTB1[3:0]				--	SDTB1[2:0]		
44h	B2	00h	R/W	BRTB2[3:0]				--	SDTB2[2:0]		
45h	B3	00h	R/W	BRTB3[3:0]				--	SDTB3[2:0]		
46h	B4	00h	R/W	BRTB4[3:0]				--	SDTB4[2:0]		
47h	B5	00h	R/W	BRTB5[3:0]				--	SDTB5[2:0]		
48h	B6	00h	R/W	BRTB6[3:0]				--	SDTB6[2:0]		
49h	C1	00h	R/W	BRTC1[3:0]				--	SDTC1[2:0]		
4Ah	C2	00h	R/W	BRTC2[3:0]				--	SDTC2[2:0]		
4Bh	C3	00h	R/W	BRTC3[3:0]				--	SDTC3[2:0]		
4Ch	C4	00h	R/W	BRTC4[3:0]				--	SDTC4[2:0]		
4Dh	C5	00h	R/W	BRTC5[3:0]				--	SDTC5[2:0]		
4Eh	C6	00h	R/W	BRTC6[3:0]				--	SDTC6[2:0]		
4Fh	D1	00h	R/W	BRTD1[3:0]				--	SDTD1[2:0]		
50h	D2	00h	R/W	BRTD2[3:0]				--	SDTD2[2:0]		
51h	D3	00h	R/W	BRTD3[3:0]				--	SDTD3[2:0]		
52h	D4	00h	R/W	BRTD4[3:0]				--	SDTD4[2:0]		
53h	D5	00h	R/W	BRTD5[3:0]				--	SDTD5[2:0]		
54h	D6	00h	R/W	BRTD6[3:0]				--	SDTD6[2:0]		
55h	E1	00h	R/W	BRTE1[3:0]				--	SDTE1[2:0]		
56h	E2	00h	R/W	BRTE2[3:0]				--	SDTE2[2:0]		
57h	E3	00h	R/W	BRTE3[3:0]				--	SDTE3[2:0]		
58h	E4	00h	R/W	BRTE4[3:0]				--	SDTE4[2:0]		
59h	E5	00h	R/W	BRTE5[3:0]				--	SDTE5[2:0]		
5Ah	E6	00h	R/W	BRTE6[3:0]				--	SDTE6[2:0]		
5Bh	F1	00h	R/W	BRTF1[3:0]				--	SDTF1[2:0]		
5Ch	F2	00h	R/W	BRTF2[3:0]				--	SDTF2[2:0]		
5Dh	F3	00h	R/W	BRTF3[3:0]				--	SDTF3[2:0]		
5Eh	F4	00h	R/W	BRTF4[3:0]				--	SDTF4[2:0]		
5Fh	F5	00h	R/W	BRTF5[3:0]				--	SDTF5[2:0]		
60h	F6	00h	R/W	BRTF6[3:0]				--	SDTF6[2:0]		

Note: Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
Writing to these bits will be ignored.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

3. Register Map Detailed Explanation

Register Name		RST							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
01h	W	--	--	--	--	--	--	RAMRST	SRST
Default	00h	0	0	0	0	0	0	0	0

D1 : RAMRST RAM reset
[0] : RAM can be overwrite (default)
[1] : Clear all PWM duty setting and intensity setting

D0 : SRST Soft reset control
[0] : Reset release state (default)
[1] : Reset reset

・This register will auto-return to zero when written with "High" logic value.

Register Name		POWERCNT							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
02h	R/W	--	--	--	--	--	--	--	OSCEN
Default	00h	0	0	0	0	0	0	0	0

D0 : OSCEN Internal oscillator ON/OFF bit
[0] : Internal oscillator OFF (default)
[1] : Internal oscillator ON

・Oscillator will auto turn ON if any of the LED drivers are enabled (MTXON = 1) even if this bit is Low.

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		OPTION							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
04h	R/W	--	--	--	--	ZPDEN	MLDACT	CLKOUT	EXTCLK
Default	00h	0	0	0	0	0	0	0	0

D3 : ZPDEN Ghost Image Prevention Enable
[0] : Turn off ghost image prevention (default)
[1] : Turn on ghost image prevention

D2 : MLDACT External Melody Input Selection
[0] : Turn off melody mode (default)
[1] : Turn on melody mode

D1 : CLKOUT Internal clock output enable
[0] : Internal clock is not output from CLKOUT (default)
[1] : Internal clock is output from CLKOUT

D0 : EXTCLK Internal/external synchronous clock selection
[0] : Internal clock operation (default)
[1] : External clock operation

- For D2, D1 and D0 cannot be set to High at the same time. In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.

Register Name		MTXON							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
05h	R/W	--	--	--	IMAX Reserved	IMAX[2:0]			MTXON
Default	1Eh	0	0	0	1	1	1	1	0

D3-1 : IMAX Maximum current setup selection
[000] : 7.5 mA
[001] : 15 mA
[010] : 22.5 mA
[011] : 30 mA
[100] : 37.5 mA
[101] : 45 mA
[110] : 52.5 mA
[111] : 60 mA (default)

D0 : MTXON LED Matrix Set up ON/OFF control
[0] : OFF (default)
[1] : ON

- For better accuracy, it is advisable to set IMAX at 30 mA (IMAX = 011). The brightness can be adjusted lower by using brightness register (BRT*[3:0] (register #3Dh to #60h)) or PWM register (DT*[7:0] (register #19h to #3Ch)).

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		PWMEN1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
06h	R/W	--	--	PWMA6	PWMA5	PWMA4	PWMA3	PWMA2	PWMA1
Default	00h	0	0	0	0	0	0	0	0

D5 : PWMA6 A6 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D4 : PWMA5 A5 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D3 : PWMA4 A4 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D2 : PWMA3 A3 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D1 : PWMA2 A2 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D0 : PWMA1 A1 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

- The definition for register addresses #07h to #0Bh is the same as address #06h.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		MDLEN1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0Ch	R/W	--	--	MLDA6	MLDA5	MLDA4	MLDA3	MLDA2	MLDA1
Default	00h	0	0	0	0	0	0	0	0

D5 : MLDA6 A6 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D4 : MLDA5 A5 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D3 : MLDA4 A4 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D2 : MLDA3 A3 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D1 : MLDA2 A2 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D0 : MLDA1 A1 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

- The definition for register addresses #0Dh to #11h is the same as address #0Ch.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		MDLMODE1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
12h	R/W	--	--	--	--	GRP6_3	GRP6_2	GRP6_1	GRP6_0
Default	00h	0	0	0	0	0	0	0	0

D3 : GRP6_3 Column 6 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (F6 (TH1) → E6 (TH2) → D6 (TH3) → C6 (TH4) → B6 (TH6) → A6 (TH8))

D2 : GRP6_2 Column 5 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (F5 (TH1) → E5 (TH2) → D5 (TH3) → C5 (TH4) → B5 (TH6) → A5 (TH8))

D1 : GRP6_1 Column 2 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (F2 (TH1) → E2 (TH2) → D2(TH3) → C2 (TH4) → B2 (TH6) → A2 (TH8))

D0 : GRP6_0 Column 1 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (F1 (TH1) → E1 (TH2) → D1 (TH3) → C1 (TH4) → B1 (TH6) → A1 (TH8))

GRP6_*	MLD*	Melody Modes
0	0	Normal mode
1	x	Bar meter mode of selected group
0	1	Melody mode of selected LED

A1	A2	A3	A4	A5	A6	Threshold 8
B1	B2	B3	B4	B5	B6	Threshold 6
C1	C2	C3	C4	C5	C6	Threshold 4
D1	D2	D3	D4	D5	D6	Threshold 3
E1	E2	E3	E4	E5	E6	Threshold 2
F1	F2	F3	F4	F5	F6	Threshold 1
GRP6_0	GRP6_1			GRP6_2	GRP6_3	

- During Bar Mode, auto threshold detection should be used.
  This IC does not support Bar Mode with fixed threshold setting.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		MLDCOM							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
13h	R/W	--	--	--	--	--	MLDCOM[2:0]		
Default	01h	0	0	0	0	0	0	0	1

D2-0 : MLDCOM LED Turn on time compensation in melody mode

[000] : 0s
[001] : 1.28 µs (default)
[010] : 2.56 µs
[011] : 3.85 µs
[100] : 5.13 µs
[101] : 6.41 µs
[110] : 7.7 µs
[111] : 8.98 µs

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		THOLD							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
14h	R/W	THOLD[7:0]							
Default	00h	0	0	0	0	0	0	0	0

D7 : THOLD[7] Threshold 8 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 8 is used. (Threshold 8 is about 1.93 V)

D6 : THOLD[6] Threshold 7 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 7 is used. (Threshold 7 is about 1.80 V)

D5 : THOLD[5] Threshold 6 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 6 is used. (Threshold 6 is about 1.67 V)

D4 : THOLD[4] Threshold 5 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 5 is used. (Threshold 5 is about 1.55 V)

D3 : THOLD[3] Threshold 4 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 4 is used. (Threshold 4 is about 1.42 V)

D2 : THOLD[2] Threshold 3 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 3 is used. (Threshold 3 is about 1.30 V)

D1 : THOLD[1] Threshold 2 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 2 is used. (Threshold 2 is about 1.17 V)

D0 : THOLD[0] Threshold 1 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 1 is used. (Threshold 1 is about 1.04 V)

- When all bits are set zero, threshold is in auto-detection mode (default)
- Do not set more than 1 register bit to logic "High" value at the same time.
- If 2 bits are set to "High" at the same time, system will only recognize the first "High" bit threshold that is set.

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		CONSTX							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
15h	R/W	--	X7	X6	X5	X4	X3	X2	X1
Default	00h	0	0	0	0	0	0	0	0

D6 : X7 X7CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X7CNT is fixed to High. The LED F1's current setting is used.

D5 : X6 X6CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X6CNT is fixed to High. The LED A6's current setting is used.

D4 : X5 X5CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X5CNT is fixed to High. The LED A5's current setting is used.

D3 : X4 X4CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X4CNT is fixed to High. The LED A4's current setting is used.

D2 : X3 X3CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X3CNT is fixed to High. The LED A3's current setting is used.

D1 : X2 X2CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X2CNT is fixed to High. The LED A2's current setting is used.

D0 : X1 X1CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X1CNT is fixed to High. The LED A1's current setting is used.

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		CONSTY							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
16h	R/W	--	--	Y6	Y5	Y4	Y3	Y2	Y1
Default	00h	0	0	0	0	0	0	0	0

D5 : Y6 Y6CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y6CNT is fixed to High.

D4 : Y5 Y5CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y5CNT is fixed to High.

D3 : Y4 Y4CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y4CNT is fixed to High.

D2 : Y3 Y3CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y3CNT is fixed to High.

D1 : Y2 Y2CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y2CNT is fixed to High.

D0 : Y1 Y1CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y1CNT is fixed to High.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		YMSK							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
17h	R/W	--	--	Y6MSK	Y5MSK	Y4MSK	Y3MSK	Y2MSK	Y1MSK
Default	00h	0	0	0	0	0	0	0	0

D5 : Y6MSK Y6CNT is fixed to Low mode.
[0] : Y6CNT output (default)
[1] : Y6CNT is fixed to Low.

D4 : Y5MSK Y5CNT is fixed to Low mode.
[0] : Y5CNT output (default)
[1] : Y5CNT is fixed to Low.

D3 : Y4MSK Y4CNT is fixed to Low mode.
[0] : Y4CNT output (default)
[1] : Y4CNT is fixed to Low.

D2 : Y3MSK Y3CNT is fixed to Low mode.
[0] : Y3CNT output (default)
[1] : Y3CNT is fixed to Low.

D1 : Y2MSK Y2CNT is fixed to Low mode.
[0] : Y2CNT output (default)
[1] : Y2CNT is fixed to Low.

D0 : Y1MSK Y1CNT is fixed to Low mode.
[0] : Y1CNT output (default)
[1] : Y1CNT is fixed to Low.

Mode priority (X*CNT) (* = 1 to 7)

X*	Y*MSK	Y*	XCNT
1	X	X	High
0	X	1	Low
0	X	0	X*CNT

Mode priority (Y*CNT) (* = 1 to 6)

X*	Y*MSK	Y*	YCNT
1	X	X	Low
0	1	X	Low
0	0	1	High
0	0	0	Y*CNT

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		SLPTIME							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
18h	R/W	SCANSET[2:0]			FADTIM	SLOPEEXTL[1:0]		SLOPEEXTH[1:0]	
Default	A0h	1	0	1	0	0	0	0	0

D7-5 : SCANSET Scan number control.

[000] : Only scan the first column.
[001] : Only scan the first 2 column.
[010] : Only scan the first 3 column.
[011] : Only scan the first 4 column.
[100] : Only scan the first 5 column.
[101] : Scan all column (default)
[110] : Scan all column
[111] : Scan all column

- For D7-5, any value above [101] will scan all column.

D4 : FADTIM Fade out time control.

[0] : T3 = T1 (default)
[1] : T3 = T1 × 2.

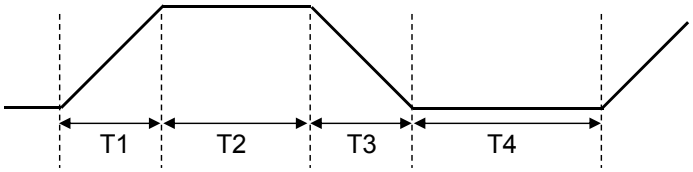
- This bit also affect in PWM fade out mode. Fade out time becomes 2 times of fade in time when FADTIM = 1.

D3-2 : SLOPEEXTL T4 time extent control.

[00] : T4 = T1 (default)
[01] : T4 = T1 × 0.25
[10] : T4 = T1 × 0.5
[11] : T4 = T1 × 2

D1-0 : SLOPEEXTH T2 time extent control.

[00] : T2 = T1 (default)
[01] : T2 = T1 × 0.25
[10] : T2 = T1 × 0.5
[11] : T2 = T1 × 2



- T1 time is controlled by the register #3Dh to #60h.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		DTA1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
19h	R/W	DTA1[7:0]							
Default	00h	0	0	0	0	0	0	0	0

D7-0 : DTA1 A1 PWM duty control.
[0000_0000] : 0%. (default)
[0000_0001] : 0.39%. (1/256)
[0000_0010] : 0.78%. (2/256)
[0000_0011] : 1.17%. (3/256)
…
[1111_1100] : 98.8%. (253/256)
[1111_1110] : 99.2%. (254/256)
[1111_1111] : 99.6%. (255/256)

- This duty setting is only effective when PWMA1 is High.
- The definition for register addresses #1Ah to #3Ch is the same as address #19h.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

3. Register Map Detailed Explanation (continued)

Register Name		A1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
3Dh	R/W	BRTA1[3:0]				--	SDTA1[2:0]		
Default	00h	0	0	0	0	0	0	0	0

D7-4 : BRTA1 Luminance set up of LED A1 (in case of IMAX [2:0] = [011])

[0000] : 0 mA (default)
[0001] : 2 mA
[0010] : 4 mA
[0011] : 6 mA
…
[1100] : 24 mA
[1101] : 26 mA
[1110] : 28 mA
[1111] : 30 mA

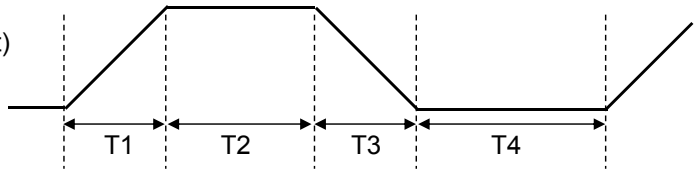
D2-0 : SDTA1 (SCANSET = [101], default setting)

(1) Firefly Operation (PWMA1 = 0)

[000] : Constant current mode (default)
[001] : 0.165 s
[010] : 0.5 s
[011] : 1 s
[100] : 1.5 s
[101] : 2 s
[110] : 2.5 s
[111] : 3 s

(2) PWM Fade-in/out Operation (PWMA1 = 1)

[000] : Instant change mode (default)
[001] : 1.3 ms
[010] : 3.9 ms
[011] : 7.8 ms
[100] : 11.7 ms
[101] : 15.5 ms
[110] : 19.4 ms
[111] : 23.3 ms



- In case of PWM duty change from 0 to 255, the longest time is 255 × 23.3 ms = 5.94 s.
- T1 time is also controlled by SCANSET in register #18h. The calculation method is as follow:

SCANSET = 000 : T1 = (1/6) × T_default
SCANSET = 001 : T1 = (2/6) × T_default
SCANSET = 010 : T1 = (3/6) × T_default
SCANSET = 011 : T1 = (4/6) × T_default
SCANSET = 100 : T1 = (5/6) × T_default
SCANSET = 101 : T1 = (6/6) × T_default

- The definition for register addresses #3Eh to #60h is the same as address #3Dh.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

4. Operation Mode Priority

MTXON	X*	PWM*	SDT*	Operation Mode
0	x	x	x	OFF
1	1	x	x	X*CNT constant mode
1	0	1	x	PWM mode
1	0	0	!= 0	Firefly mode
1	0	0	0	Constant current mode

OPERATION (continued)

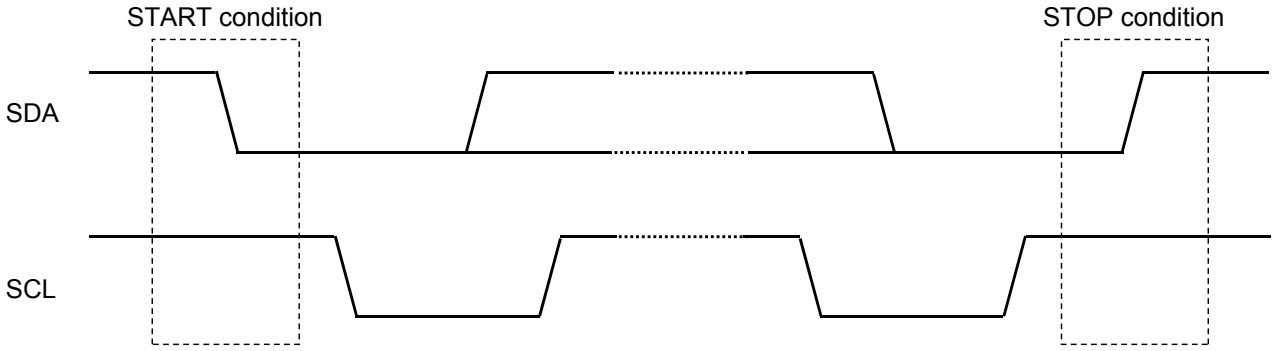
5. I²C Bus Interface

5.1 Basic Rules

- This IC, I²C-bus, is designed to correspond to the Standard-mode (100 kbps), Fast-mode(400 kbps) and Fast-mode plus (1 000 kbps) devices in the version 03 of NXP's specification. However, it does not correspond to the HS-mode (to 3.4 Mbps).
- This IC will operate as a slave device in the I²C-bus system. This IC will not operate as a master device.
- The program operation check of this IC has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this IC to the CBUS receiver also has not been checked. Please confirm with our company if it will be used in these mode systems.
- The I²C is the brand of NXP.

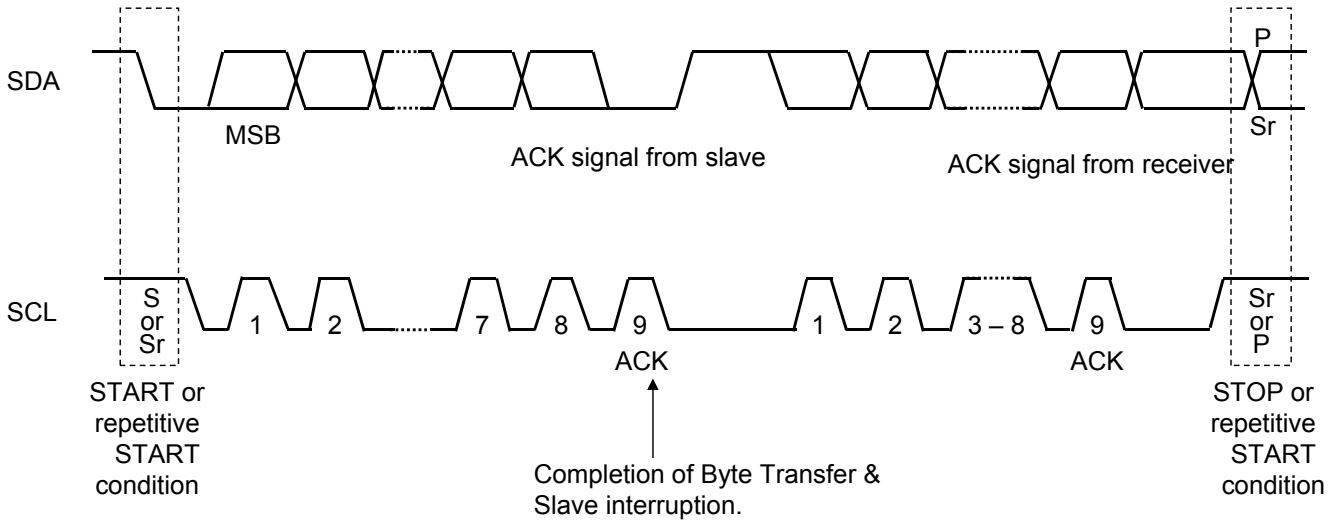
5.2 START and STOP conditions

When SDA signal changes from "High" to "Low" while SCL is "High" will trigger START condition. Whereas, STOP condition will be triggered when SDA signal changes from "Low" to "High" while SCL is "High". START condition and STOP condition are always formed by the master. After the START condition occurs, the bus becomes busy state. After STOP condition occurs, the bus becomes free again.



5.3 Data Transfer

Length of each byte output to SDA line is always 8 bits. There is no limitation in the number of bytes that can be transmitted at 1 time. Many bytes can be sent. The acknowledge bit is necessary for each byte. Data is sequentially transmitted from most significant bit (MSB).



Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

5. I²C Bus Interface (continued)

5.4 I²C Interface - Data Format

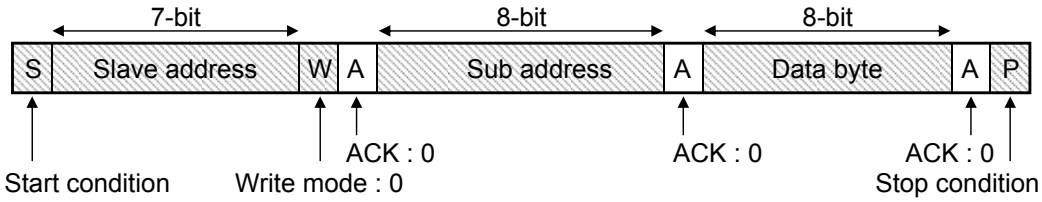
In this IC, 4 different Slave addresses can be changed by selecting SLAVSEL ("Low" or "High" or "SCL" or "SDA").

The slave addresses of this IC are as follow:

SLAVSEL	Slave address
Low	1011 000X
High	1011 001X
SCL	1011 010X
SDA	1011 011X

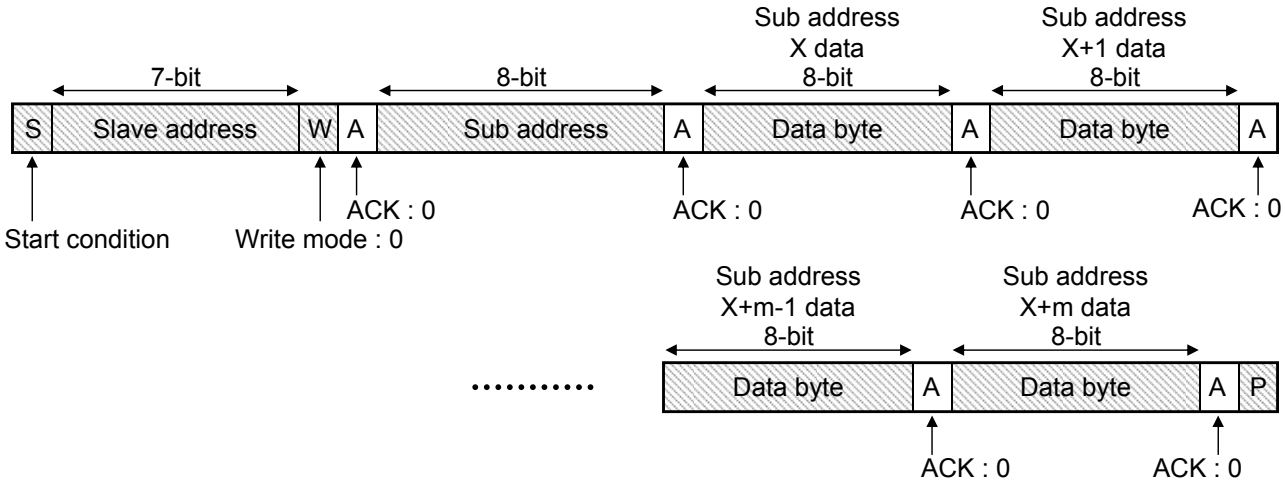
• Write mode

Sub address is not incremented automatically.
The next data byte is written in the same Sub address by transmitting data byte continuously.



• Write mode (Auto increment mode)

Data byte can be written in Sub address by transmitting data byte continuously.
Sub address is incremented automatically.



: Data transmission from Master

: Data transmission from Slave

Established : 2011-07-29
Revised : 2014-01-22

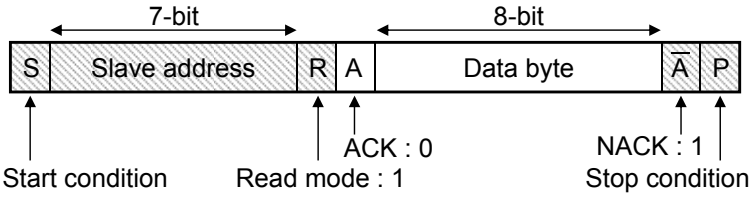
OPERATION (continued)

5. I²C Bus Interface (continued)

5.4 I²C Interface - Data Format (continued)

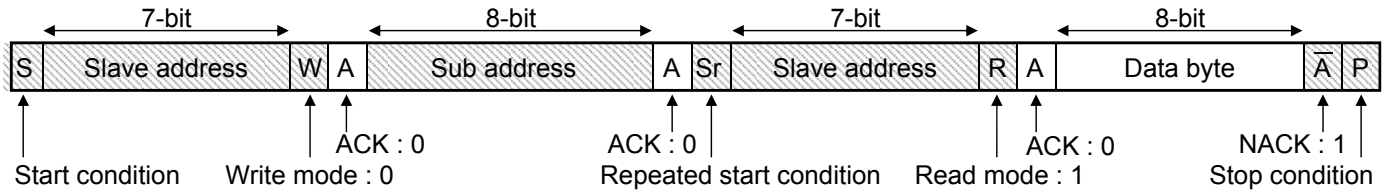
- Read mode (in case Sub address is not specified)

When Sub address 8 bit is not specified and data is read, this IC allows to read the value of adjacent Sub address specified in the last Write mode.
The next data byte reads the same Sub address by transmitting data byte continuously.



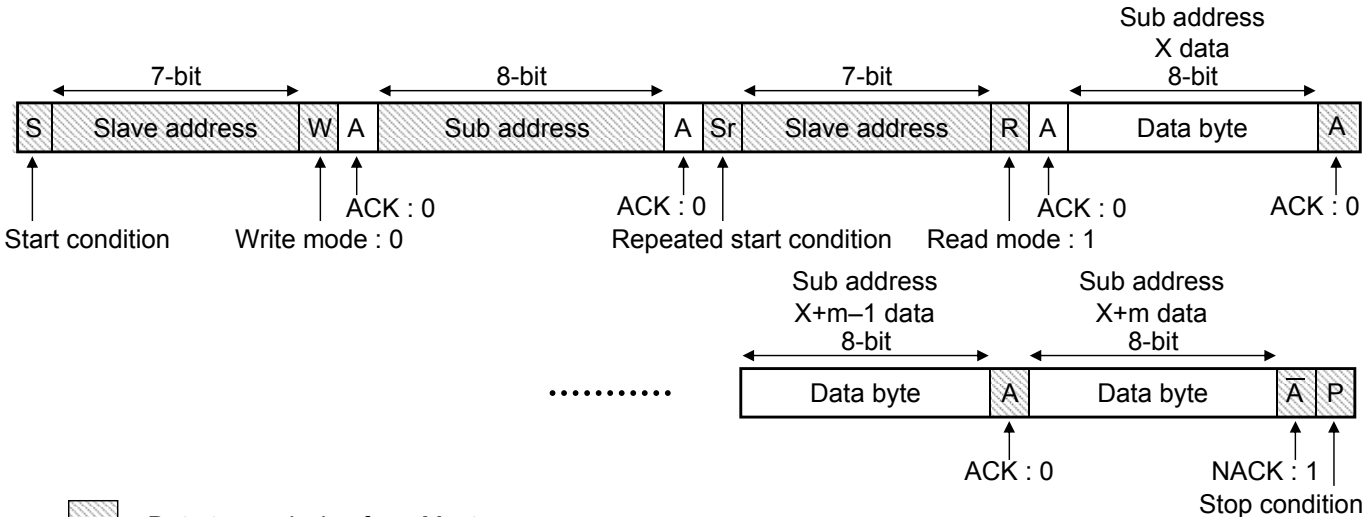
- Read mode (in case Sub address is specified)

Sub address is not incremented automatically.
The next data byte reads the same Sub address by transmitting data byte continuously.



- Read mode (Auto increment mode)

It is possible to read data byte in continuous Sub address by transmitting data byte continuously.
Sub address is incremented automatically.



: Data transmission from Master

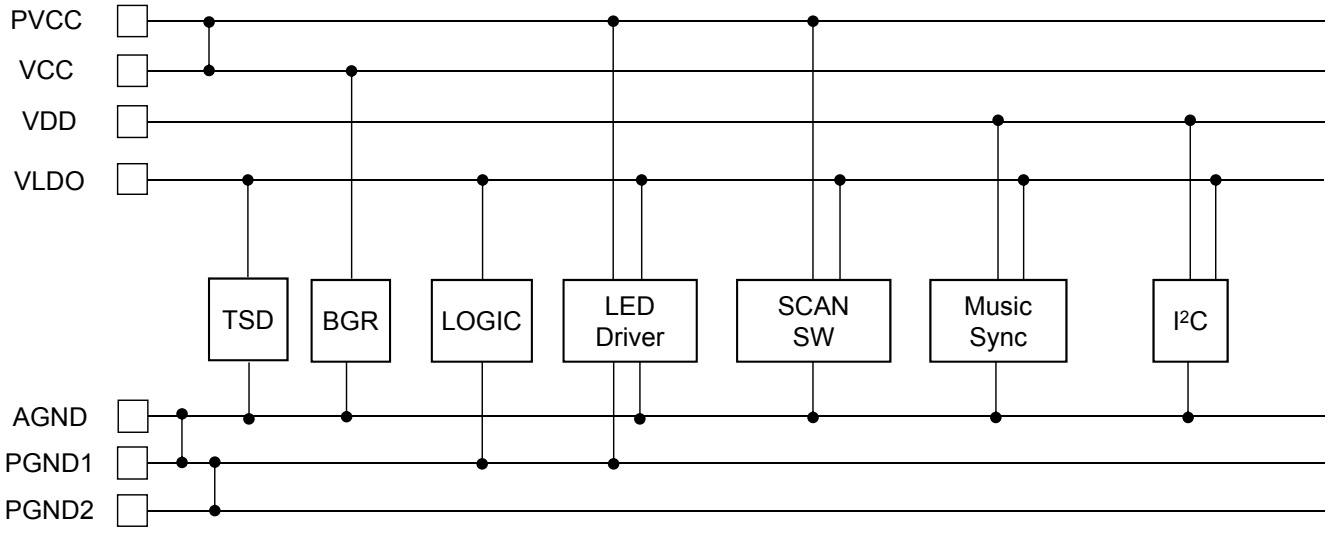
: Data transmission from Slave

Established : 2011-07-29
Revised : 2014-01-22

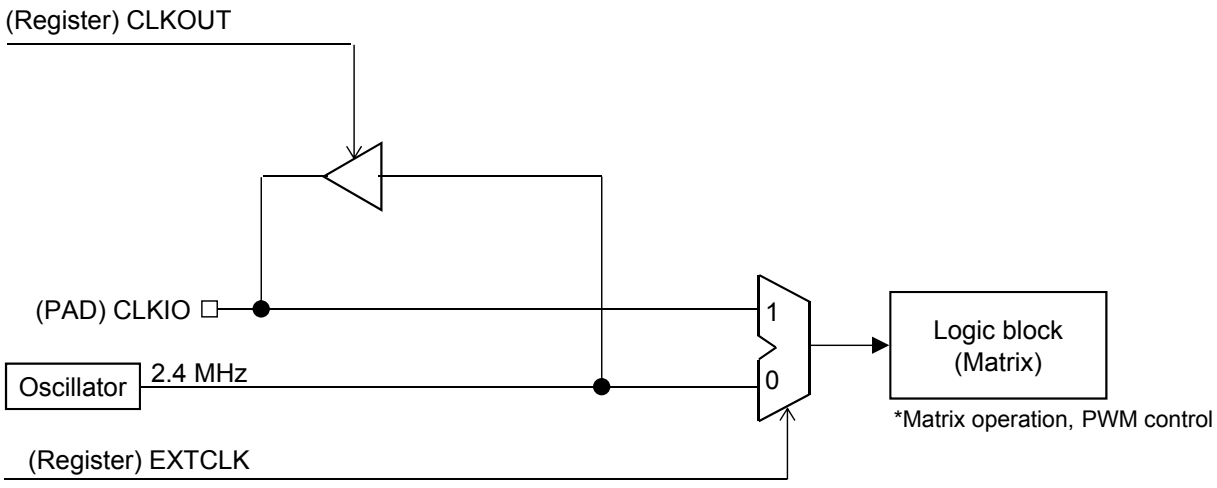
OPERATION (continued)

6. Signal distribution diagram

6.1 Distribution diagram of power supply



6.2 Distribution diagram of control / clock system



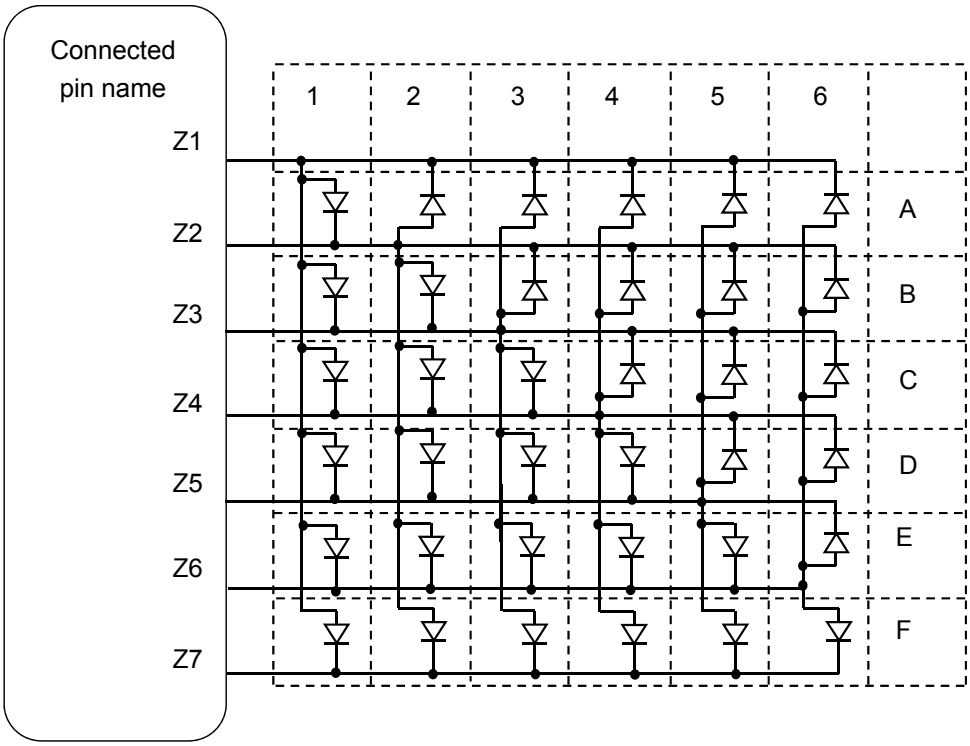
Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

7. Block Configuration of Matrix LED

7.1 Matrix LED descriptions, Matrix LED's numbers

LED matrix driver circuit individually drives LED of 6 x 6 matrix. In total, the IC can drive and light up 36 LED.
In this specification, LED's number controlled by each pin corresponds as follows.
The internal logic circuit is operated by using an internal clock or the external clock input to the terminal CLKIO.



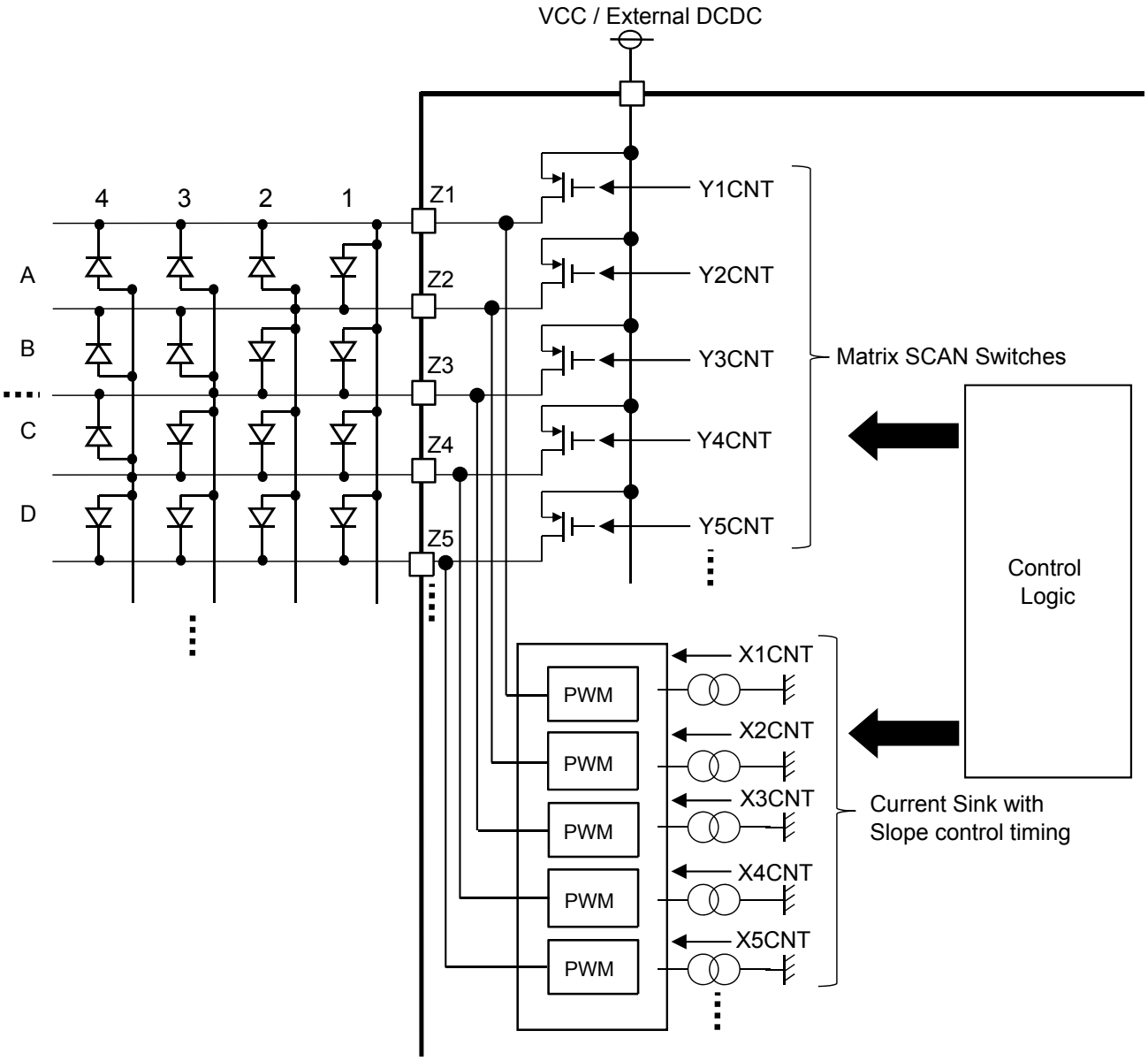
Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

7. Block Configuration of Matrix LED (continued)

7.2 Driver Configuration

- Actual driver configuration is shown in the following figure.
- The anode and cathode of each LED are connected to different Z pin as shown in figure below.
- Z7 pin consists of only Current Sink and Slope control timing driver. Thus, LED anodes are not to be connected to Z7 pin.
- Please do not remove any of the LED inside the matrix if it is not used. If LED are to be removed, it is advised to remove the entire row (e.g: all LED in row A) instead of removing only 1 LED. If only one LED in the row is removed instead of the whole row, user needs to avoid using LED of which reverse breakdown voltage is lower than the operating VCC level.
- Internal control logic according to user register settings is used to control Y1 to Y6CNT(PMOS ON/OFF Scan Switches) as well as X1 to X7CNT (Current sink value as well as PWM/Slope timing for lighting effects)



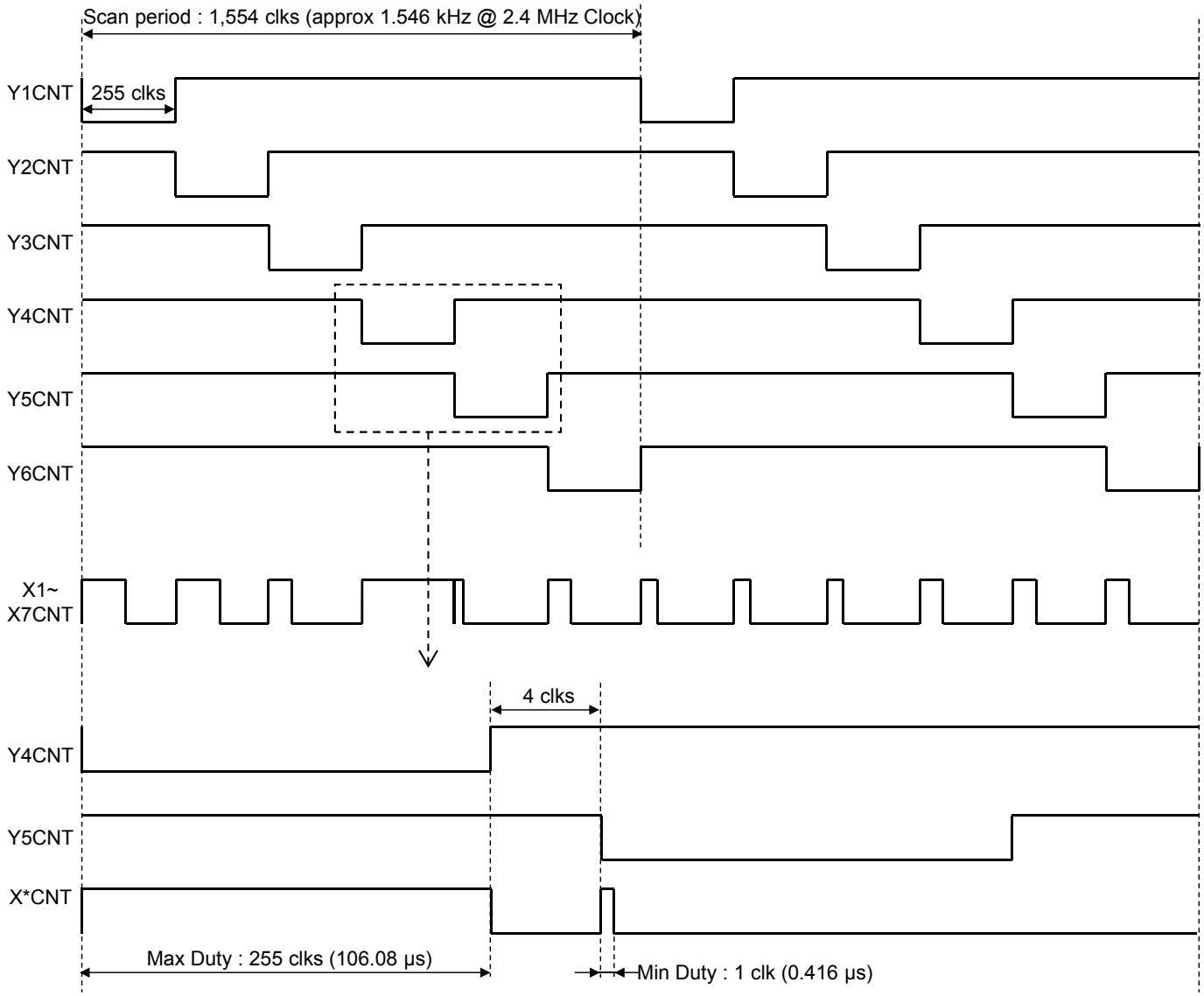
Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

7. Block Configuration of Matrix LED (continued)

7.3 Timing Chart when in operation

- The figure below shows the timing chart when in operation.
- Timing can be controlled according to the external clock frequency input to CLKIO pin.
- In default condition, it is controlled by internal 2.4 MHz clock.
- Y1 to Y6CNT are scan timing which is turned on one at a time. The ON period of each pin is constant 255 clks (106.08 µs) and includes the interval of 4 clks (1.664 µs).
- 36 LED (6 x 6 matrix) are controlled by X1 to X7CNT according to below figure.
- When Yx = Xx = Low, the actual waveform of Zx is set to Hi-Z.



- Duty can be set using register DT*[7:0] from registers #19h to #3Ch. Additional brightness control is provided through register BRT*[3:0] (registers #3Dh to #60h).

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

8. LED Driver Block Function

- Functions Table for LED Driver

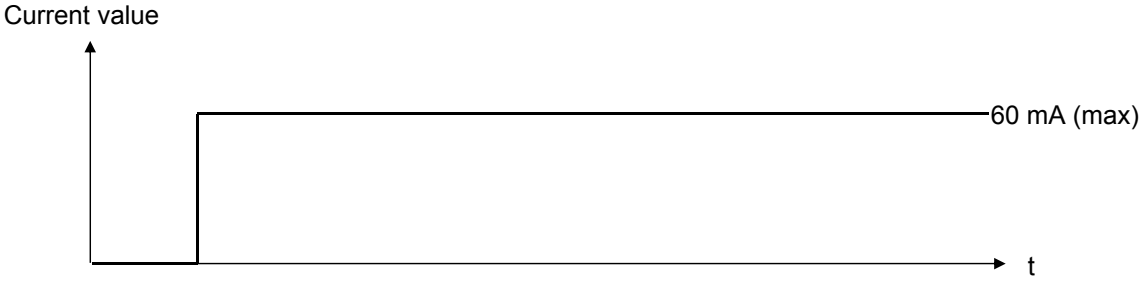
No.	Features	Setting Range
1	Constant current mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step
2	PWM mode and Fade-in/out mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Adjustable detention Time for each step : (1.3 ms to 23.3 ms / step)
3	Firefly mode	Fixed Current at 100% Duty IMAX Setting :7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Adjustable detention Time for each step : (0.165 s to 3 s / step)
4	Melody mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Each LED can synchronize with Music Input from CLKIO pin
5	Bar mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Group LED can synchronize with Music Input from CLKIO pin Bar mode has more priority than Melody mode.

8.1 Constant Current Mode

Maximum current setting value can be set up as 60mA using register IMAX[2:0] (register 05h). Brightness can be set through the register BRT*[3:0] (register #3Dh ~ #60h) for individual LED.

Example)

E.g. If user sets register IMAX[2:0](#05h) = 011 and BRT*[3:0] = 1111, the current will be 30 mA.
E.g. If user sets register IMAX[2:0](#05h) = 111 and BRT*[3:0] = 1111, the current will be 60 mA.
E.g. If user sets register IMAX[2:0](#05h) = 111 and BRT*[3:0] = 0111, the current will be 28 mA.



Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

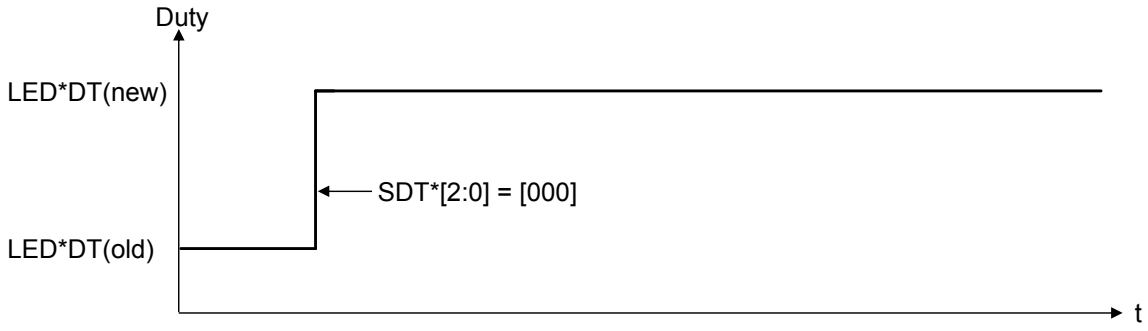
8. LED Driver Block Function (continued)

8.2 PWM Mode and Fade-in/out Mode

This operation is characterized by PWM signal having variable duty depending on register DT*[7:0] (registers #19h to #3Ch). However, any changes in duty are not instantaneous, but rather it will step to the new duty at time determined by register SDT*[2:0].

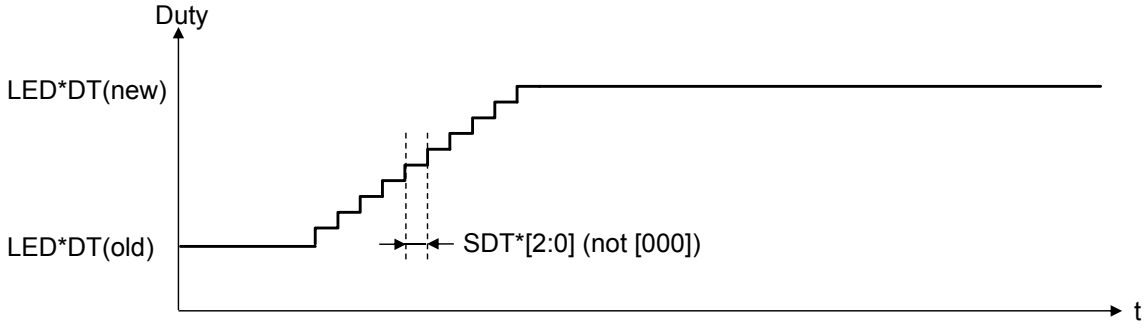
Example)

Case 1 : LED*DT(new) > LED*DT(old) (PWM Mode without Fade in/out control)



In Case 1, PWM duty has been changed from low to high duty. But the register SDT*[2:0] setting is [000] meaning there is no Fade in/out control. Therefore, PWM duty changes instantaneously. Users can see that LED becomes brighter instantaneously once PWM duty has been changed.

Case 2 : LED*DT(new) > LED*DT(old) (PWM Mode with Fade in control)



In Case 2, PWM duty has also been changed from low to high duty. Unlike in case 1, the register SDT*[2:0] setting is not [000] in case 2. Therefore, PWM duty has changed according to the register SDT*[2:0] setting. This is called PWM mode with Fade in control. Users can see that LED becomes brighter slowly according to the timing set in register SDT*[2:0].

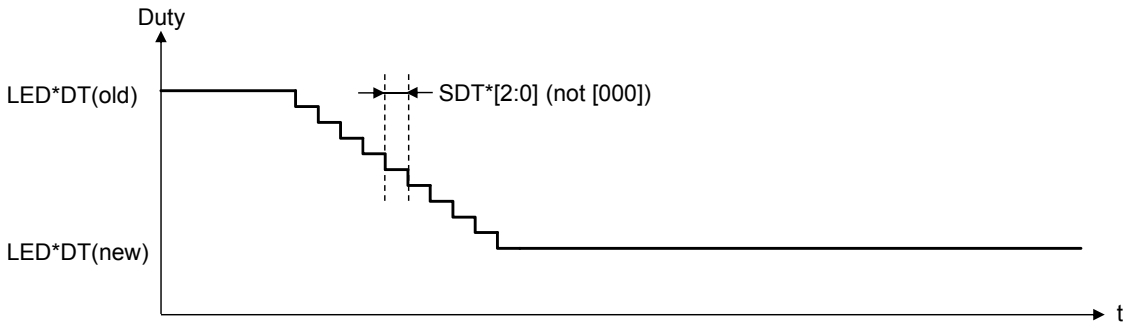
OPERATION (continued)

8. LED Driver Block Function (continued)

8.2 PWM Mode and Fade-in/out Mode (continued)

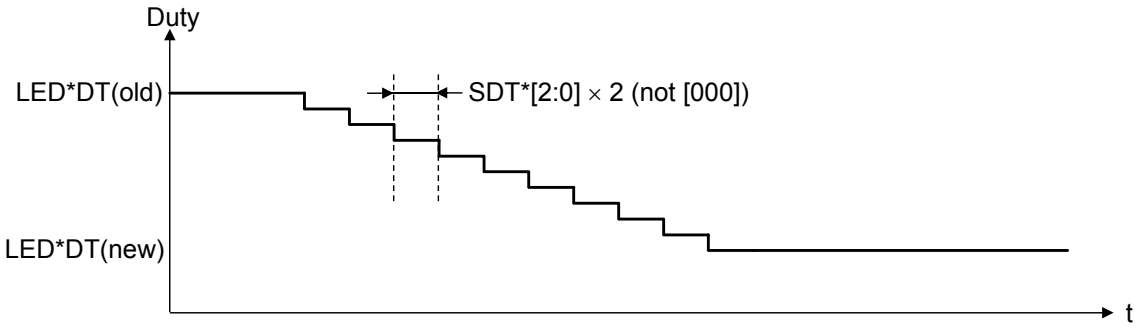
Example) (continued)

Case 3 : LED*DT(new) < LED*DT(old), FADTIM = 0 (PWM Mode with Fade out control)



In Case 3, PWM duty has been changed from high to low duty. Unlike in case 1, the register SDT*[2:0] setting is not [000] in case 3. Therefore, PWM duty has changed according to the register SDT*[2:0] setting. This is called PWM mode with Fade out control. Users can see that LED becomes dimmer slowly according to the timing set in register SDT*[2:0].

Case 4 : LED*DT(new) < LED*DT(old), FADTIM = 1 (PWM Mode with Fade out control)



In Case 4, PWM duty has also been changed from high to low duty. Unlike in case 3, the register FADTIM is not [0]. Again, the register SDT*[2:0] setting is also not [000] in case 4. PWM duty has changed according to the register SDT*[2:0] setting. Users can see that LED becomes dimmer slowly. It is slower than Case3 as FADTIM register is high (2 times slower than Case 3 Fade out control).

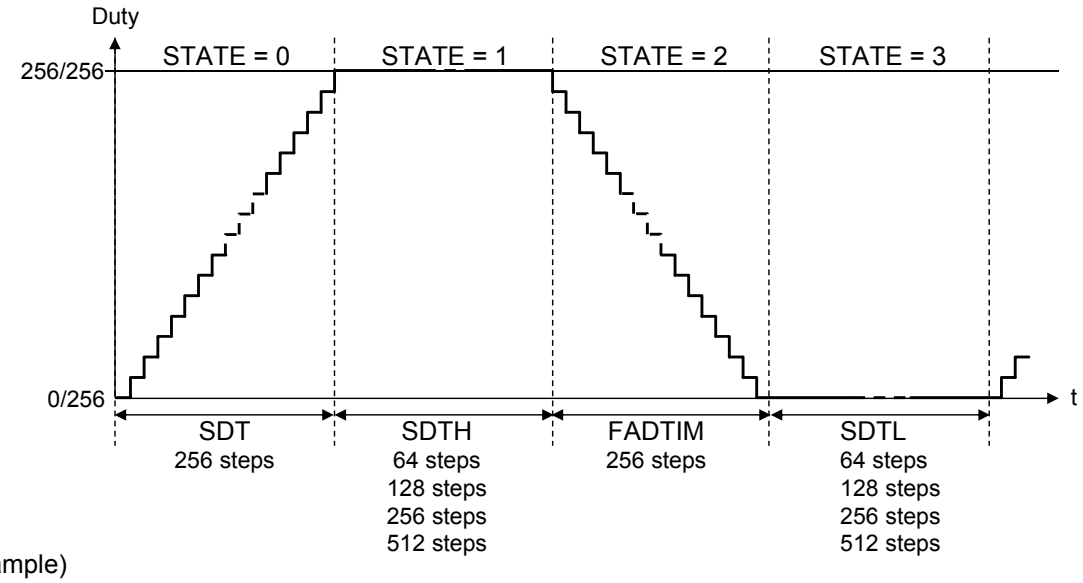
DT*[7:0] is set through register #19h to #3Ch. FADTIM is set through register #18h. SDT*[2:0] is set through register #3Dh to #60h.

OPERATION (continued)

8. LED Driver Block Function (continued)

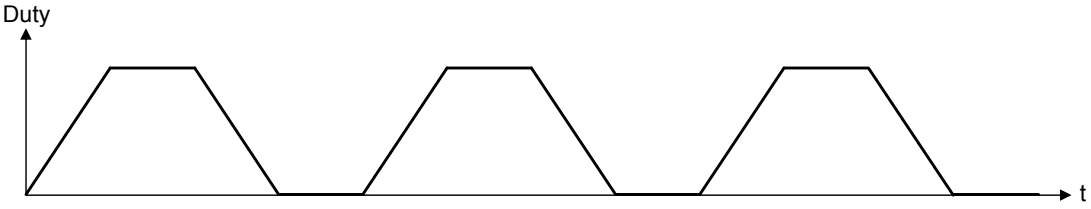
8.3 Firefly Control

This operation is characterized by PWM signal cycling from minimum to maximum duty and vice versa with auto repeat function at time step determined by register SDT*[2:0]. Unlike PWM Fade in/out mode, firefly is auto repeat and thus creating LED blinking function effect.

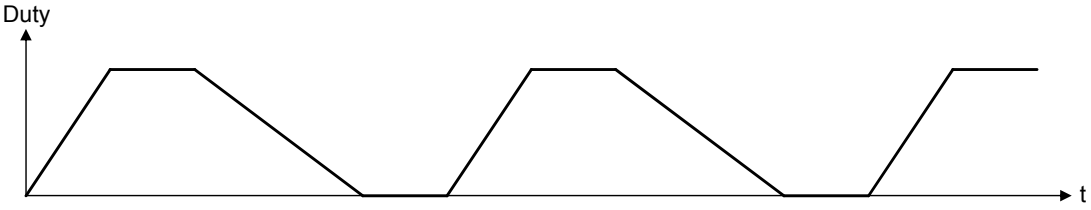


Example)

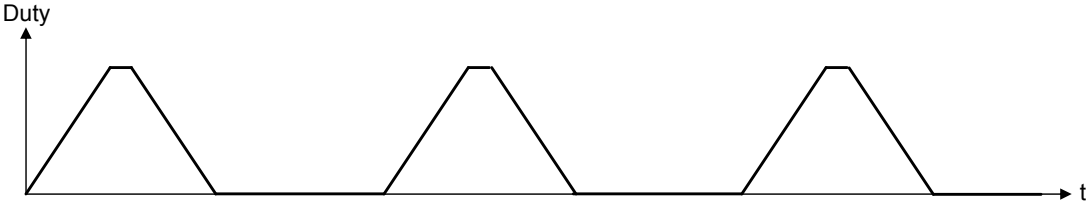
Example 1 : SDTH = 00 (SDT × 1), SDTL = 00 (SDT × 1), FADTIM = 0



Example 2 : SDTH = 00 (SDT × 1), SDTL = 00 (SDT × 1), FADTIM = 1 (SDT × 2)



Example 3 : SDTH = 01 (SDT × 0.25), SDTL = 11 (SDT × 2), FADTIM = 0



The SDTH is controlled by SLOPEEXTH[1:0] register, SDTL is controlled by SLOPEEXTL[1:0] register. All these register, SLOPEEXTH[1:0], SLOPEEXTL[1:0] and FADTIM can be set through register #18h. SDT*[2:0] registers are set individually through register #3Dh to #60h. All other combinations of SDTH, SDTL and FADTIM is possible.

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

8. LED Driver Block Function (continued)

8.4 Melody Mode Explanation

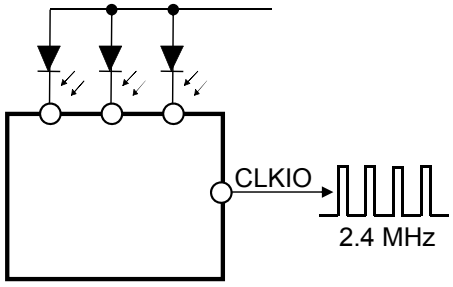
Melody mode is to synchronize LED to external music signal. Melody mode can be set through register MLDACT from register 04h. Each of the 36 LED matrix can be individually enabled for external music synchronization through register data (address #0Ch to #11h when register 04h is 04h).

External Music Signal can be injected from CLKIO pin. CLKIO pin serve as both input and output. CLKIO pin can output internal oscillator frequency by using CLKOUT register (register 04h).

CLKIO pin can be used as input for external signal by using EXTCLK register (register 04h). External clock frequency is typically 2.4 MHz. It is advisable to use external clock frequency from 1.2 MHz to 4.8 MHz .

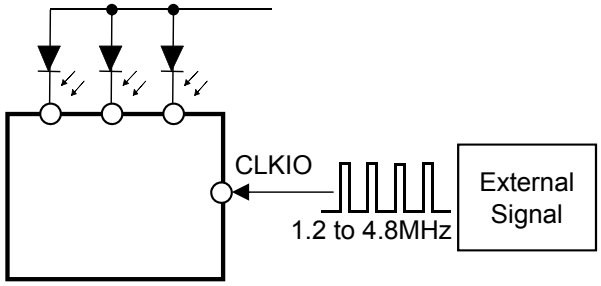
Please do not set MLDACT, EXTCLK and CLKOUT register to "High" at the same time. In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.

Case 1 : CLKIO as output pin



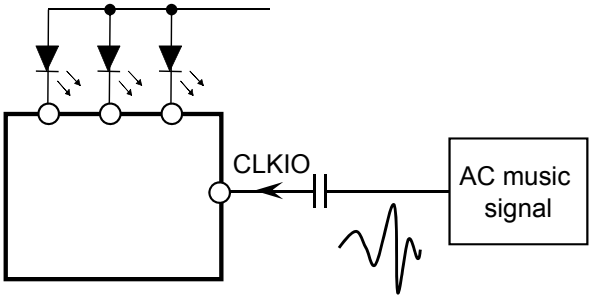
CLKIO output internal frequency by using CLKOUT register

Case 2 : CLKIO as input for external clock



CLKIO uses as external input by using EXTCLK register

Case 3 : CLKIO as input for music signal during melody mode



CLKIO uses as music input when melody mode is enabled by register MLDACT from register 04h.

Note : If input CLKIO voltage is higher than VDD, there will be back flow current to VDD. It can be calculated as below :

$$I_{BackFlow} = \frac{(V_{CLKIO} - 0.7\ V - VDD)}{393\ k\Omega}$$

Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

8. LED Driver Block Function (continued)

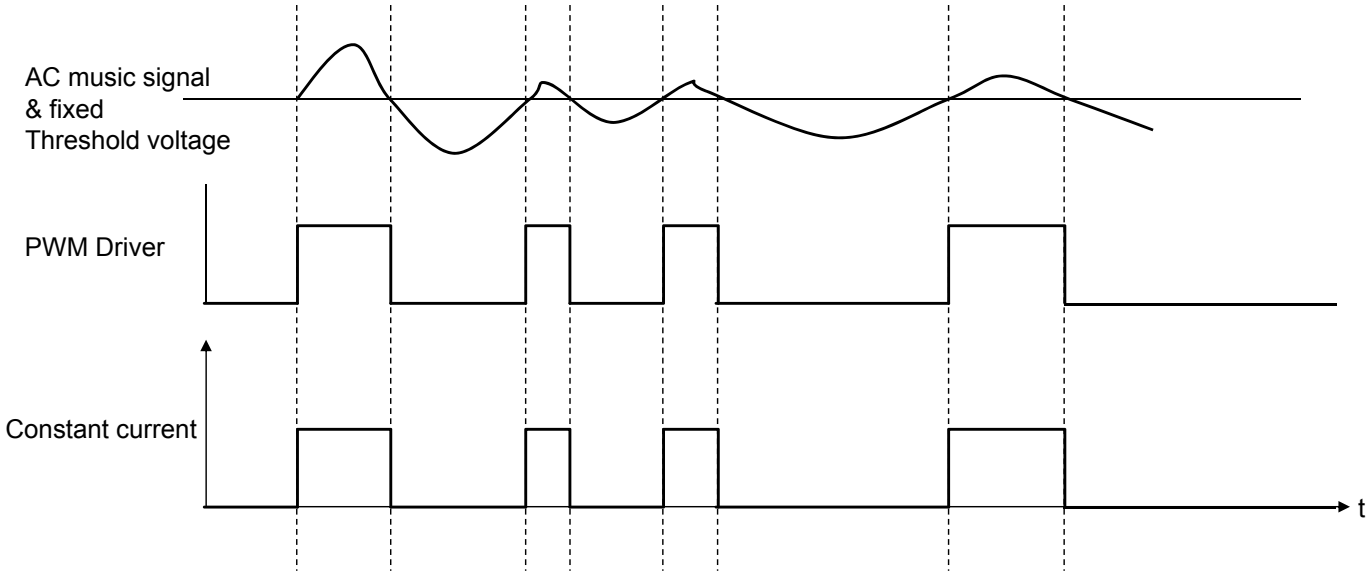
8.4 Melody Mode Explanation (continued)

AC music signal input from CLKIO pin will be compared with internal threshold setting. Based on the comparison of music signal and threshold voltage, PWM driver control will change and control the LED ON/OFF. Therefore, LED light ON/OFF control will synchronize with music tempo while LED brightness will synchronize with music loudness.
There are two threshold modes, one is auto threshold and the other is fixed threshold mode.

There are 8 threshold voltage levels in this IC as defined in the register 14h (THOLD[7:0]). Auto threshold mode means that the 8 threshold voltages will be scanned automatically from the lowest to highest threshold voltages at a fixed frequency higher than audio frequency. Input music signal will be compared with these scanning threshold voltages to control PWM Driver in order to have music synchronization effects. This mode allows user to easily use music synchronize function without having the trouble of manually setting the detection threshold. When melody mode is enabled, auto threshold mode will be the default mode.

Fixed threshold mode means that the threshold voltage is fixed at one threshold level. It can be set using register 14h (THOLD[7:0]). Input music signal will be compared with this fixed threshold voltage set by the user. During fixed threshold mode, do not set more than 1 register bit to logic "High" value at the same time. If user set more register bits to logic "High" after setting 1 register bit to "High", system will only recognise the first "High" bit threshold that is set. In this mode, user can have the flexibility to configure different threshold voltage levels to achieve the desired LED music synchronizing visual effect according to the system music input level.

It is also advised that AC music signal peak to peak voltage to be at least 0.35 V and not more than 2.8 V.



Example of Fixed threshold mode

• Brightness Compensation in Melody Mode

Additional brightness compensation in melody mode can be achieved by increasing or decreasing the turning on period of LED. Using brightness compensation register #13h, LED turning on period can be controlled and LED can become brighter or dimmer.

This additional brightness compensation will be effective only in auto threshold mode. If fixed threshold mode is used, this register will not be able to control LED brightness.

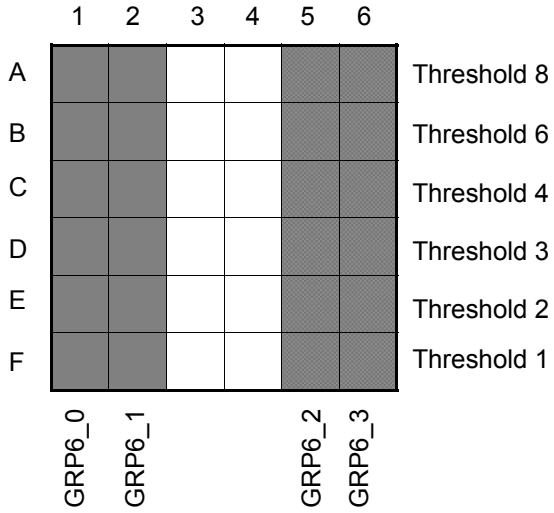
Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

8. LED Driver Block Function (continued)

8.5 Bar Mode Explanation

Bar Mode operation is another method of external melody mode wherein a group of LEDs are used instead of individual LED. Bar Mode has higher priority than individual LED melody mode.



In the above diagram, column 1 = group6_0, column 2 = group6_1, column 5 = group6_2 and column 6 = group6_3.
Each group can be enabled through register GRP6_0, 6_1, 6_2, 6_3 (address #12h). The LED in the all groups will be synchronized to threshold signals as follow:

Threshold Signal	Bar Mode Group LED ON	
Threshold 1	Row's	F
Threshold 2	Row's	E, F
Threshold 3	Row's	D, E, F
Threshold 4	Row's	C, D, E, F
Threshold 6	Row's	B, C, D, E, F
Threshold 8	Row's	A, B, C, D, E, F

All other LEDs not in bar mode can operate in individual external melody mode or other modes. During bar mode, auto threshold detection should be used. This IC does not support bar mode with fixed threshold setting. It is also recommended not to use other modes together with bar mode of LED in group 6_0 to 6_3 (i.e. LED A to F1, 2, 5, 6)

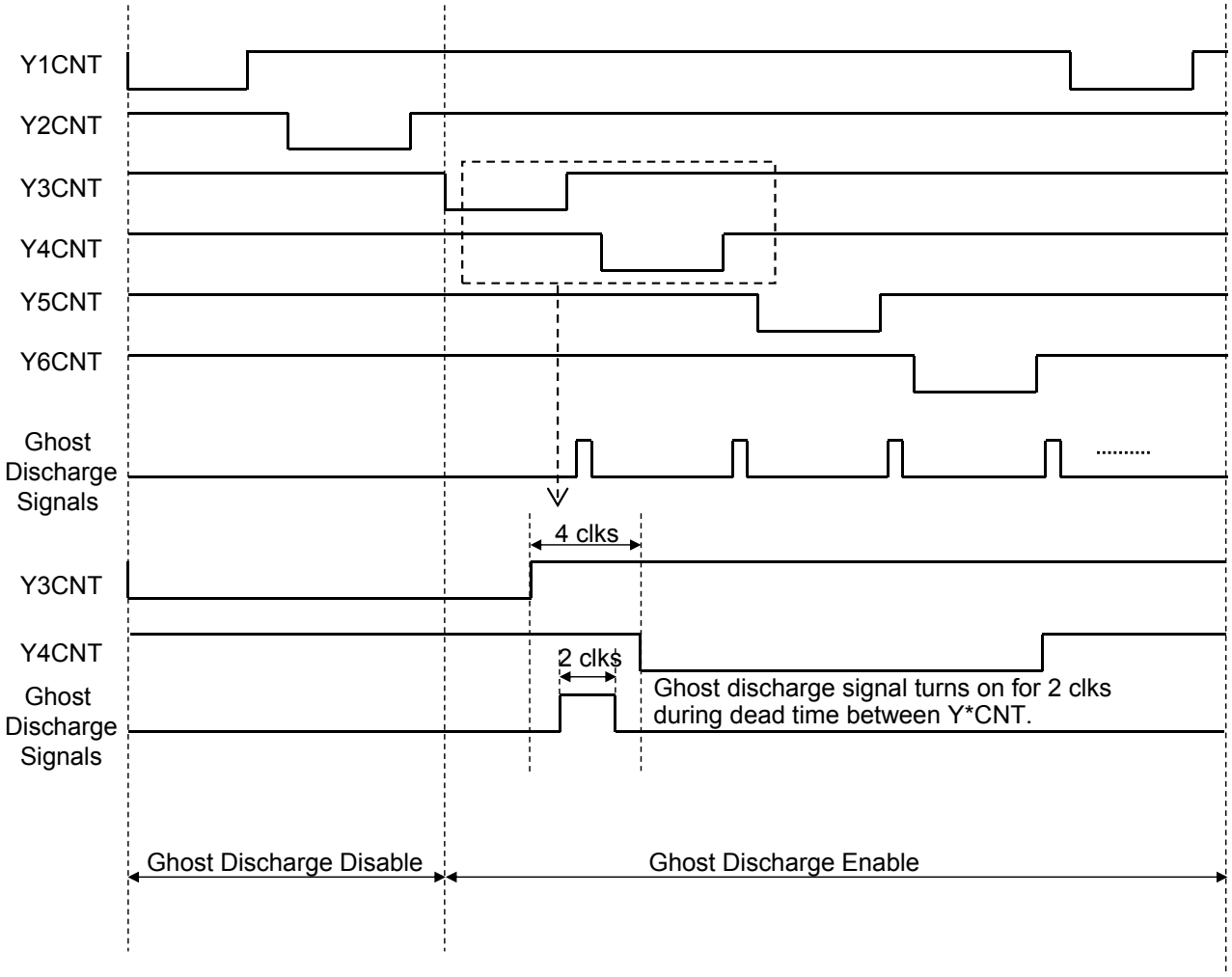
Established : 2011-07-29
Revised : 2014-01-22

OPERATION (continued)

9. Ghost Image Prevention Function

Ghost images sometimes appear during LED matrix mode operation. Very dim light can appear in some LED even during OFF condition. This is called Ghost Image. In this IC, Ghost Image Prevention Function is included to prevent Ghost Image. Ghost Image Prevention Function can be enable through register ZPDEN (register 04h).

• Ghost Image Prevention may not remove the ghost image perfectly. It depends on the LED color combination and LED connection method.



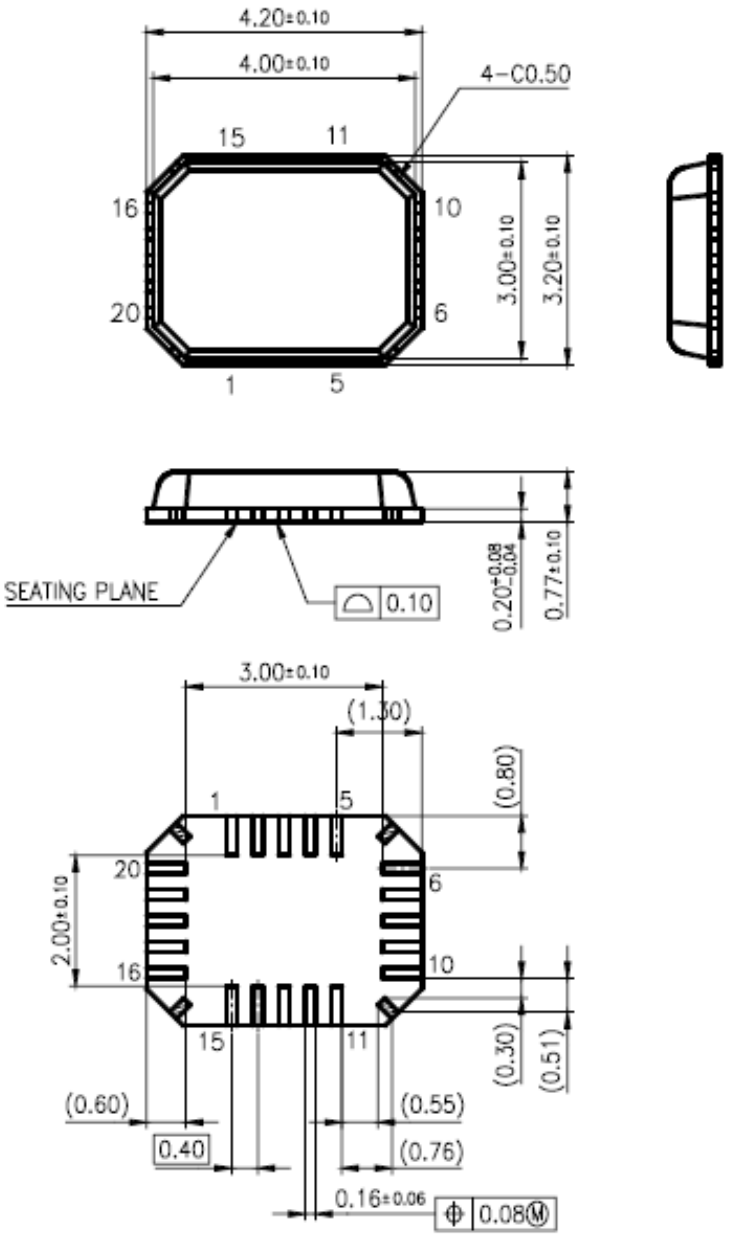
During normal operation, ghost discharge signal will be always low. When ghost image prevention function is enabled through register 04h, ghost discharge signal will turn on for 2 clks cycle during 4 clks dead time between each YCNT. During on period of 2 clks cycle, output Z pin will be forced to half of VCC.

Established : 2011-07-29
Revised : 2014-01-22

PACKAGE INFORMATION (Reference Data)

Unit:mm

Package Code : *QFN020-P-0304C



Body Material	:	Br / Sb Free Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	Pd Plating

Established : 2011-07-29
Revised : 2014-01-22

IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Verify the risks which might be caused by the malfunctions of external components.

Established : 2011-07-29
Revised : 2014-01-22

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application, unless our company agrees to your using the products in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

20100202