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One-Chip "Slide Rule" Works with Logs, Antilogs for Real-Time Processing

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An analog computer IC multiplies and divides signals, takes powers, and also roots. A log-antilog section raises dynamic range during division.

An analog divider circuit seems to promise something for nothing. Just divide any number by zero and the result is infinity. But in theory, if numbers approaching zero are in the denominator, the divider must achieve infinite gain, and its input offset error must be smaller than the input signal.

In practice, analog divider chips fail to achieve even the modest 100-to-1 dynamic range vital to a wide-range circuit. A viable device calls for gains greater than 40 dB and input offset voltages under 100 μV.

But all is not lost. The AD538 multifunction IC's 1000-to-1 dynamic range surpasses the 50-to-1 limit of earlier one-chip dividers. Noise is held to only 25 μV—referenced to the input—over a 1000-Hz bandwidth, with its offset voltages under 100 μV.

A truly versatile analog computer on a chip, the 538 tackles one-quadrant multiplication and one- and two-quadrant division. It also calculates powers and roots of ratios. Like all analog computers, it runs in real time, making it the chip of choice when linearizing signals from transducers.

Its basic transfer function:

$$V_{out} = V_Y (V_Z/V_X)^M$$

makes the circuit simple to configure for a particular function. All that need be done is to connect specific pins and—in some cases—add one or two external resistors. Depending on the application, one, several, or all sections of the chip can be called into play.

The analog IC basically consists of an accurate 10-V/2-V reference and five precision op amps, all with offset voltages that are laser-trimmed to under 100 μV (Fig. 1). But the chip is more than the sum of its parts. It is designed as a complete analog computer whose system performance is specified for both voltage and current inputs. Its low input and output offset voltages, excellent linearity, and modest noise levels all contribute to its wide dynamic range—guaranteed from 1 mV to 10 V (80 dB).

The user's free access to the summing junctions of four of the chip's op amps gives it much of its versatility. External input resistors can change the pretrimmed offset or scaling voltages and allow multiple signals to be summed at each input terminal. The IC's power supply ranges from ± 4 to ± 18 V, letting

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it run from standard split ±15-V supplies, as well as from ±12-V and even ±5-V units. The 2-V reference is particularly useful for driving the chip from ±5-V sources.

The op amps form three of the device's four major function blocks. The log ratio amplifier section harnesses three of them; the log and antilog section, one; and the output current-to-voltage stage, the last.

A logging operation

The V_Z and V_X inputs connect directly to the log-ratio section. This block furnishes an output voltage proportional to the difference between the natural logarithms, Ln, of the input voltages V_Z and V_X (Ln V_Z − Ln V_X). The transfer function between these inputs and the section's output pin (B) is given by

$$V_{out} = \frac{kT}{q} \text{Ln} \frac{V_Z}{V_X}$$

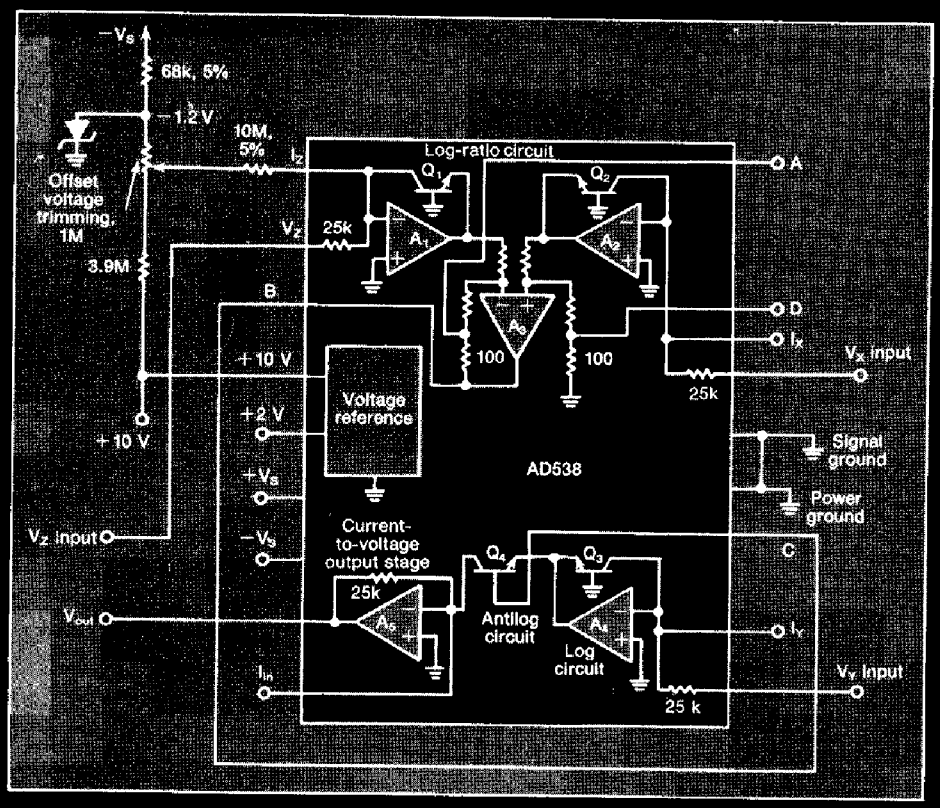
where k is Boltzmann's constant, T is the absolute Kelvin temperature, and q is the unit charge (1.60219×10^{-19}C).

The log ratio section may be used on its own (to compress the ratio of two signals) by temperature-compensating and scaling its output. To do so, its output (B) is joined to the summing junction of the output amplifier (I_{in}) through two external resistors. A 60-Ω 1% metal-film device is hooked in series with a 1-kΩ temperature-compensating resistor with a temperature coefficient of +3500 ppm/°C.

For most applications, however, the log ratio section is linked to the input of the antilog section (pin V_Y). That converts the signal from the logarithmic into the linear domain, according to the transfer function:

$$V_{out} = V_Y e^{(V_C q/kT)}$$

where V_C is the voltage at pin C. This section, like the



1. The transfer function of the AD538 one-chip analog computer is $V_{out} = V_Y (V_Z/V_X)^M$ when M is between 1/5 and 5. The flexibility of the transfer function allows the chip, which works in real time, to replace a microcomputer as well as several data converters.

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log ratio block, may be used alone in order to expand a signal. Combining the transfer functions of both sections by tying together the B and C outputs results in the equation:

$$V_{out} = V_Y e^{\left(\frac{kT}{q} \times \frac{q}{kT} \times Ln \frac{V_Z}{V_X}\right)}$$

when $V_B = V_C$. This expression reduces to the multiplier-divider transfer function:

$$V_{out} = V_Y \frac{V_Z}{V_X}$$

Raising V_Z/V_X to the Mth power with an external resistor results in the analog computer chip's overall transfer function:

$$V_{out} = V_Y (V_Z/V_X)^M$$

where $\frac{1}{5} < M < 5$.

In most applications the V_Y input is used to set a convenient scale factor. The linear V_Y input signal is multiplied by adding the log of the V_Y input to the signal at C, which is already in the log domain. The chip's third section, the output current-to-voltage converter, buffers and scales the output from the antilog block.

Finally, the band-gap reference section supplies either +2 or +10 V, accurate to ±0.5% with a tempco of 25 ppm/°C. The 10-V reference is buffered and available at the ±10-V pin. The 2-V output is unbuffered. It is derived from the ±10-V pin by adding a resistive divider between the buffer's output and its summing point input.

As a result, any load on the 2-V output changes the feedback circuit and thus the 10-V reference voltage as well. To buffer the 2-V output, it is simply tied to the 10-V output.

Go forth and multiply

Taking the chip's sections singly—or even in pairs—only hints at its overall power. The device is easily configured as a high-performance, one-quadrant multiplier-divider (Fig. 1 again). As such, it handles only positive input voltages. Its transfer function:

$$V_{out} = V_Y (V_Z/V_X)$$

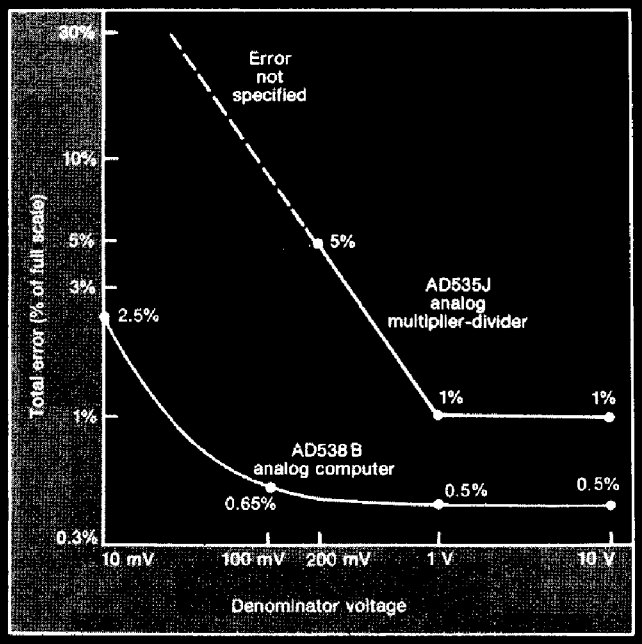
works with three input variables. That is, the chip carries out three-input calculations simultaneously—a task impossible with a conventional analog multiplier or even with a digital one.

What's more, the job is performed by the 538 in real time. When two input variables and a fixed reference are specified, the chip's dynamic range permits it to outclass such analog multipliers as the AD534. (The latter, though, performs four-quadrant multiplications—each of its two inputs may be a plus or minus voltage.)

In the circuit, if V_X is connected to either the 10- or the 2-V reference, a traditional one-quadrant analog multiplier results. (V_X, or any other input, may also be driven by a digital-to-analog converter, enabling the constant, or scaling, voltage, which establishes the output scale factor, to be set automatically or remotely.) With V_X tied to 10 V, the transfer function becomes:

$$V_{out} = (V_Y)(V_Z)/10\ V.$$

Typically, the circuit achieves a bandwidth of 400 kHz when V_X varies over a range of 100 mV to 10 V. Maximum error with both inputs swinging



2. When used for division, the AD538 has a lower total error and a much wider denominator dynamic range than an analog multiplier-divider such as the AD535—which has even been specially trimmed to serve as a divider.

from 0 to 10 V is ±0.5% of the reading. Employing an external scaling voltage and the offset trim resistor (R_1) will halve the error.

Merely switching the 10-V reference from V_X to V_Y changes the circuit to a classical one-quadrant linear divider with 10-V scaling. V_X now serves as the denominator input terminal. The transfer function is specified as follows:

$$V_{out} = (10\ V)\,(V_Z)/(V_X)$$

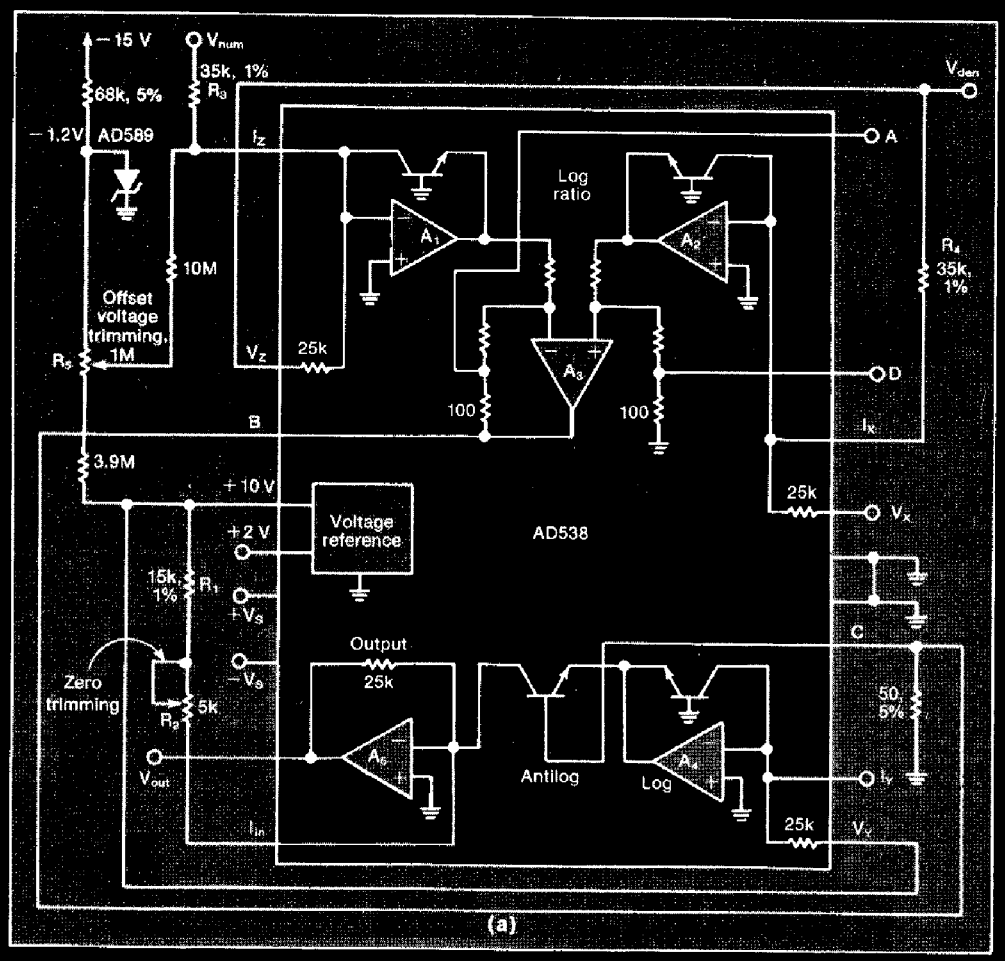
The voltage applied to V_Z is divided by that applied to V_X. The internal trimming resistor reduces offset errors to less than 100 μV.

The typical −3-dB bandwidth of the one-quadrant divider is 370 kHz for inputs between 1 and 10 V, dropping slowly to 200 kHz for 2-mV signals. Its 74-dB dynamic range (from a 2-mV noise threshold at the input to a 10-V output clipping level) is much wider than that supplied by a conventional divider circuit using an analog multiplier.

As for harmonic distortion, the circuit's 10-V peak output is produced by a sine wave on the numerator input and 1 V on the denominator input. The second harmonic of the 10-V output is 70 dB below the fundamental.

Appearances are deceiving

The mathematics of multiplication and division makes multiplier circuits appear to have much lower input offset voltages than comparable divider circuits. Multiplying numbers less than one yields a result smaller than either of the original multiplicands. Multiplying the offset voltages at two different inputs, say 0.1 V each, produces an output offset voltage of 0.01 V. In addition, the product is generally divided by 10 (to increase dynamic range), further



3. By implementing the transfer function $V_{out} = V_{num}/V_{den}$, the AD538 multifunction chip handles two-quadrant division. Thus the numerator is capable of handling both positive and negative voltages.

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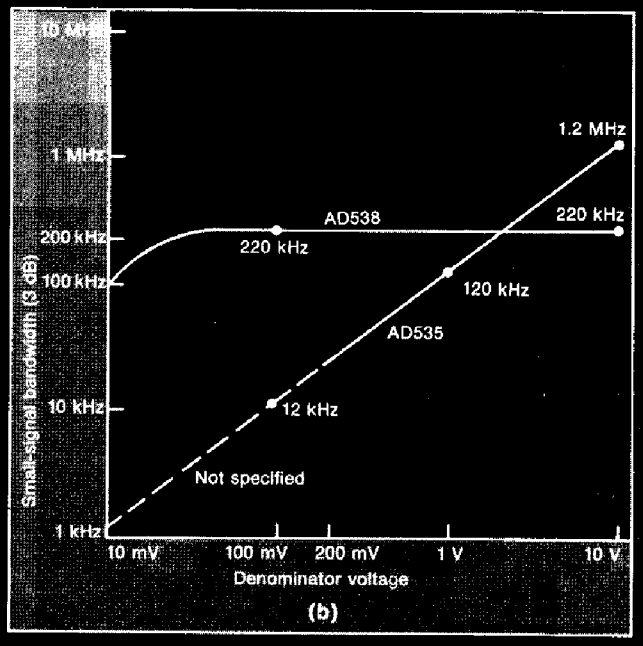
cutting output offset error to 0.001 V. Obviously, in multiplier circuits, output offset voltages matter more than do input offset voltages because the former add directly to the multiplier's output.

Divisive factors

In contrast, analog dividers usually run into difficulties over input offset voltages. The gain of an analog divider must approach infinity as the denominator moves closer to zero: Offset voltages or nonlinearities at the input are amplified by the $V_{scale}/V_{denominator}$ ratio of the divider. As the denominator voltage is reduced, input offset voltages in dividers quickly become intolerable, in turn severely degrading the device's dynamic range.

In multipliers, then, offsets are measured relative to full scale; in dividers, they must be gauged relative to the magnitude of the input signal. For any given



4. The bandwidth and dynamic range of the AD538 in the circuit of Fig. 3 are significantly greater than those of a conventional multiplier-divider IC, the AD535, in the same application.

accuracy, therefore, these offsets limit the minimum denominator voltage level.

The chip overcomes most of its input offset problems by employing high-quality op amps as input stages. These are quite different from the circuits found in the typical analog multiplier, such as the AD535, and the op amps hold offset errors under 100 μV.

A smaller total error

The device's superiority is readily seen by directly comparing total error from each chip for given denominator voltages (Fig. 2). The total error for the 535, configured as a multiplier-divider, is not even specified for denominator voltages below 200 mV. At that point it is, in fact, 5%. Alternatively, the 538's total error is only 2.5% at a denominator voltage of 10 mV—a level at which the typical multiplier-divider is unusable.

The term "total error" represents the sum of three elements: the inherent nonlinearity produced by the internal component errors; the numerator offset error multiplied by the set gain (V_Y/V_X); and the static offset error of the output amplifier. In other words, total error is expressed as:

$$\text{Nonlinearity} + (Z_{OS} \times V_Y/V_X) + V_{OS} \text{ of output amp}$$

where the subscript "OS" indicates offset.

Specifically, the chip's total error equals:

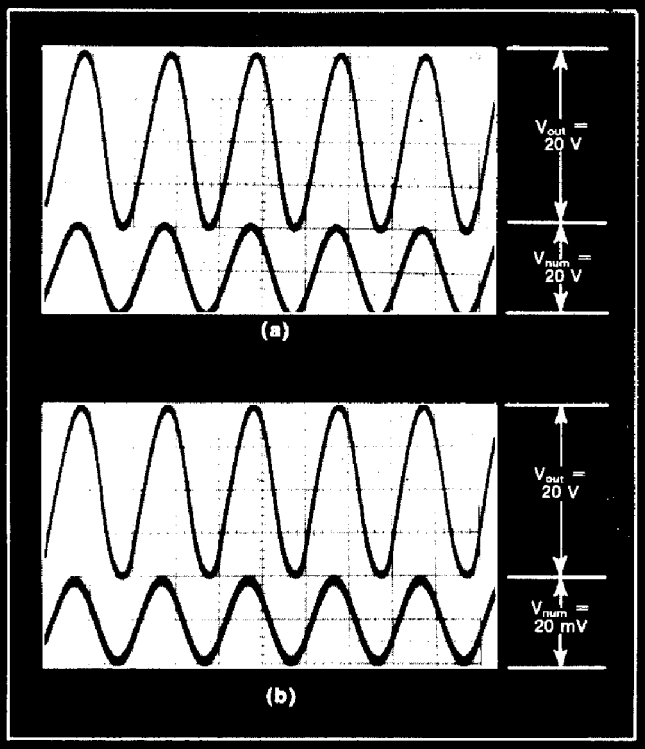
$$\pm 0.5\%\ V_{out} \pm 0.15\ \text{mV}(V_Y/V_X) \pm 0.15\ \text{mV}$$

When V_Y/V_X is small, the nonlinearity error dominates; when that ratio is large, the numerator offset error dominates; and when the output is small (under 10 mV), output offset dominates. Errors are defined in this manner so that the user may minimize total error by nulling out the error dominating a particular input condition.

Another quadrant heard from

Although the one-quadrant multiplier-divider tackles only positive input voltages, the chip can also be set up as a two-quadrant divider capable of handling bipolar numerator signals. That feat is accomplished by offsetting the nominal numerator input at V_Z by a voltage that tracks the denominator input signal V_{den}. The latter is made slightly larger than the former, by a ratio of 35 to 25 (Fig. 3). The ratio is set by feeding the numerator and denominator inputs through external 35-kΩ resistors (R_3,R_4) to the

summing node (current input) of their respective op amps, A_1 and A_2. The offsetting voltage V_{den} is summed with the numerator input, V_{num}, through the internal 25-kΩ resistor at V_Z. That offset changes the divider's transfer function from 10 V (V_Z/V_X) to:



5. In a two-quadrant divider, the chip exhibits the same dynamic response with numerator inputs between 20 V pk-pk (a) and 20 mV pk-pk (b) with denominators of 10 V and 10 mV, respectively.

Table 1. Resistor values for powers less than one

Function	R_B (Ω)	R_C (Ω)	Power (M)
One-fifth root	162	40.2	0.20
One-quarter root	150	49.9	0.25
Cube root	100	49.9	0.33
Square root	100	100.0	0.50

Table 2. Resistor values for powers greater than one

Function	R_A (Ω)	Power (M)
Fifth power	48.7	5.0
Fourth power	64.9	4.0
Analog cube	97.6	3.0
Analog square	196.0	2.0
Arc tangent	931.0	1.21

$$V_{out} = +10\ V(V_{num} + V_{den})/V_{den}$$
$$= +10\ V(1+V_{num}/V_{den})$$
$$= 10\ V + 10\ V(V_{num}/V_{den})$$

As long as the denominator input equals or exceeds the numerator in magnitude, the circuit accepts bipolar voltages (such as sine waves) at the numerator input. However, its output now equals +10 V dc without any numerator voltage applied.

To make the circuit practical, the +10-V output offset is canceled by summing it with the 10-V reference; this is done in the output op amp section through resistors R_1 and R_2. The potentiometer trims the offset, so that there is zero out for zero in, leaving the simple transfer function:

$$V_{out} = 10\ V(V_{num}/V_{den})$$

At a denominator voltage of 100 mV, this log-antilog two-quadrant divider has 20 times the bandwidth of a typical multiplier-divider like the 535 (Fig. 4). These two chips are again compared for given denominator voltages, this time against small-signal bandwidth. The log-antilog device bandwidth is virtually independent of denominator voltage and is faster for all but the highest denominator voltages.

An indication of the dynamic range, precision, and linearity of the two-quadrant divider is readily seen (Fig. 5). In both photographs, the upper waveform is the output of the chip, a 20-V pk-pk 20-kHz sine wave, and the lower waveform is the source of that signal applied to the numerator input. In each case the output is 10 V × V_{num}/V_{den} and shows virtually no difference over a 1000-to-1 change in input signals. Of course V_{den} could have been changing at the time, but the outputs would then be harder to compare.

Getting to the root of the matter

The 538 takes roots in real time with an accuracy that might well appear unbelievable for an analog circuit (Fig. 6). When configured as a square-root (M = ½) circuit, it has a transfer function of:

$$V_{out} = 1\ V\ (V_Z/1\ V)^{1/2}$$

Its scale factor adjustment R_1 and offset trimming resistor R_2 let the curcuit reach an output voltage that is within 0.35% of the ideal over a range of 1 mV to 10 V (80 dB). For an input range of 10 mV to 10 V (60 dB), the output is within ±1 mV of the theoretically correct value. This is equivalent to 13-bit performance referred to the output or 17 to 20 bits referred to the input. Circuit bandwidth is typically

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280 kHz with a 1-V pk-pk sine-wave input.

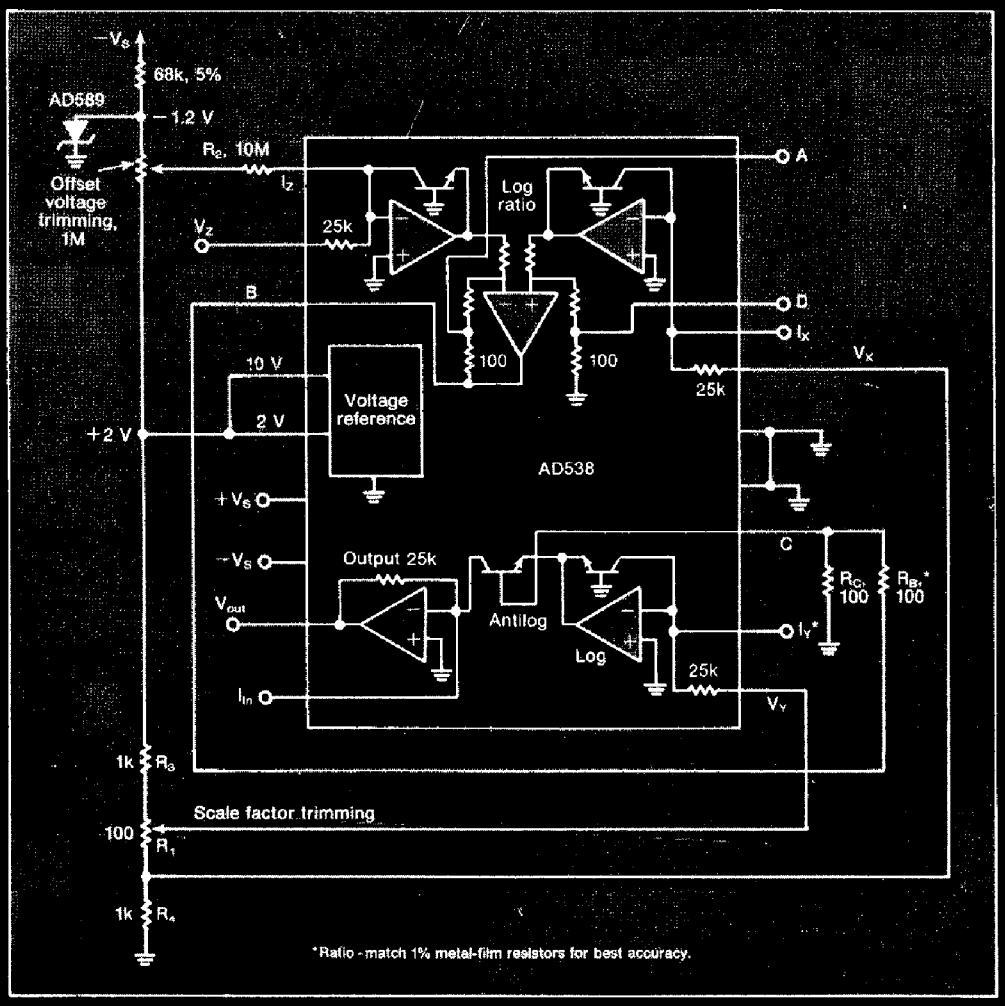
As in the divider circuit, the input signal at V_Z is divided by the level at V_X. Its 1-V scaling is obtained by halving the 2-V reference with resistors R_3 and R_4, applying roughly 1 V to both V_X and V_Y. V_X is actually set low, at 0.95 V, resulting in a V_Y value that is slightly high, providing a ±5% scale factor trimming range. The voltage terms in V_X and V_Y cancel, producing the dimensionless output required to determine a square function.

The square root is extracted by raising the quantity V_Z/V_X to the ½ power with resistors R_B and R_C. For maximum linearity the pair of resistors should be ratio-matched to better than ±1%. Changing the resistor values of R_B and R_C (Table 1) enables cube, quarter, and fifth roots to be determined according to the equation:

$$M = R_C/(R_C+R_B).$$

Finally, to raise the ratio V_Z/V_X to a power greater than one, it is only necessary to change the gain of the log-ratio subtracter op amp, A_3, by connecting a single resistor, R_A, between pins A and D. Varying the values of the resistor (see Table 2) creates M values from one to five according to the equation $R_A = 196/(M-1)$ and allows the arc-tangent function to be computed.

Since resistors of any value may be used, the chip is not limited to integral powers or roots. V_Z/V_X could be raised to the 3.17 power, say. It is only necessary that M stay between ⅕ and 5.



6. Resistors R_B and R_C set the chip to take the square root of the voltage at V_Z according to the transfer function $V_{out} = 1\ V\ (V_Z/1\ V)^{1/2}$.