

Application Note

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*Choosing Components for an
RF Receiver Using Romeo2
(MC33591/2/3/4)*



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Introduction

This application note provides information to help you choose hardware components for an RF receiver using Romeo2.

Romeo2 is a highly integrated superheterodyne receiver dedicated to RF transmission in ISM (Industrial, Scientific, and Medical) bands. It receives data transmitted using OOK (On/Off Keying) or FSK (Frequency Shift Keying) modulation, accepts data rates up to 9.6 kbps, and operates at 315 MHz, 433 MHz, 868 MHz and 915 MHz. It includes a strobe oscillator to reduce power consumption, and a data manager that recovers the clock and serializes the received signal through an SPI port. Some parameters can be software modified, sensitivity can be reduced, and data manager configuration can be changed.

Some optimizations are possible through external components; Romeo2 can be sized precisely to match the application. This application note shows how to change the frequency of operation, to change the RF matching network to accept various antennas, to add some low-pass filtering to improve sensitivity, to optimize AGC speed for any data rate, and to calculate the values of the strobe oscillator components. It also explains the role of each component.

Romeo2 Part Numbers

There are several versions of Romeo2, each with its own part number. Each version offers a different combination of frequency of operation, bandwidth of the internal intermediate frequency filter, and specification of the integrated data manager. The different versions with their part numbers are shown in the following table.

Specific features	MC33591	MC33592	MC33593	MC33594
Bands of operation	315/433 MHz	315/433 MHz	868/915 MHz	315/433 MHz
IF filter bandwidth	500 kHz	300 kHz	500 kHz	500 kHz
Modulation	OOK/FSK	OOK	OOK/FSK	OOK/FSK
Data Manager available for	OOK/FSK	OOK	OOK/FSK	FSK

Calculating External Component Values

Typical Application

A simple RF receiver can be realized with few external components (see [Figure 1](#)).

U1 is Romeo2. The external crystal X1 defines the operating frequency of the internal PLL (phase-lock loop). The loop filter of the PLL is comprised of C20, C25 and R10.

The internal AGC¹ requires an external capacitor C2 that set its time constant.

C3 is a part of the loop filter of an internal AFC² that adjusts the center frequency of the internal IF amplifier³.

C22 forms, with some internal resistors, a low-pass filter. This increases the sensitivity slightly.

C1 and R2 define the frequency of the strobe oscillator that sets the ON-OFF cycling of the receiver.

1. Automatic Gain Control increases the dynamic range of the receiver (the difference between the smallest and the largest signal the receiver can process)

2. Automatic Frequency Control — a system that uses a reference signal to adjust the frequency of a filter or receiver.

3. Intermediate Frequency amplifier in a superheterodyne receiver.

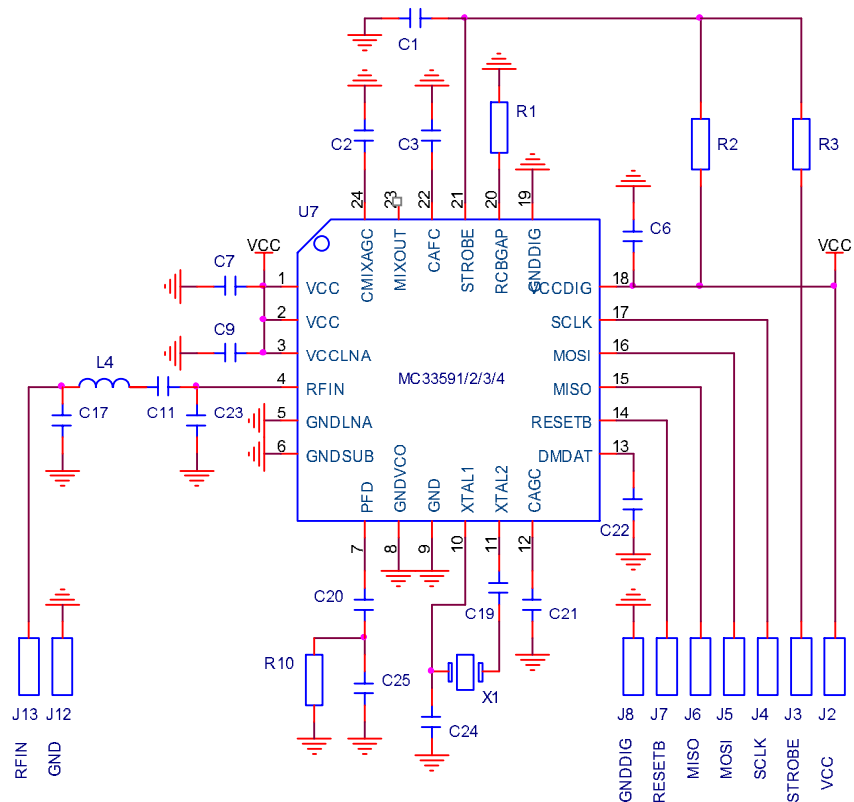


Figure 1. Typical Application using Romeo2

R3 allows the MCU to drive directly the state of the receiver.

C21 is used in OOK for the IF amplifier AGC. In the case of FSK, this capacitor is part of an average low-pass filter that sets the level of the data slicer.

C17, L4, C11, and C23 form a matching network to match the RFIN impedance of Romeo2 to the impedance of the antenna connected to J13.

R1 is used to fix internal biasing.

Power Supply Decoupling Capacitors

C7 and C9 must present a low impedance over a large frequency range. They should be located next to pin 1, 2 and 3 and should have a short track to ground. With $C7 = 100 \text{ nF}$ and $C9 = 100 \text{ pF}$, stable behavior of the front end is guaranteed.

C6 is a decoupling capacitor for the digital part. Its value is not critical and is presently fixed at $C6 = 100 \text{ nF}$.

PLL Loop Filter

R10, C20 and C25 are the external components of the loop filter for the integrated PLL. This filter is in parallel with an internal filter and is not mandatory in the present version of the silicon (designs using devices shipped from Q1 2000 onwards can omit these components). On some critical applications, a slight improvement in EMC performance has been reported when not using this filter. It can be omitted to reduce cost.

Crystal Oscillator

Crystal X1 fixes the oscillator frequency. Its load capacitance is comprised of:

- Capacitor C24 (design value is 10 pF)
- PCB and pin 10 of Romeo2 (about 2 pF)

that is, in total, 12 pF.

If C24 does not fit the value of the load capacitance of the crystal, its value can be increased to a maximum of 20 pF. Values lower than 10 pF are not recommended, as this would increase the sensitivity of the oscillator to parasitic capacitors.

To compute the frequency of X1, first select the good divide ratios (n and m) for the internal clock and the value of the bit CF¹, as shown in the following table.

Frequency Band	n	m	CF	Romeo Reference
315 MHz	8	32	0	MC33591/2/4
433 MHz	11	32	1	MC33591/2/4
868 MHz – 915 MHz	11	64	1	MC33593

Then, compute the frequency of the crystal:

$$F_{ref} = F_{rf} / (m - 0.66 / (1.2346 * n))$$

This gives X1 = 13.58 MHz for F_{rf} = 433.92 MHz.

C19 prevents the small DC voltage between XTAL1 and XTAL2 from being applied to X1, thereby increasing the crystal reliability. Its value is not critical and 10 nF is recommended.

RFIN Matching Network

Any matching network topology is possible, as long as the DC level on the RFIN pin is not affected. C11 acts as an isolating capacitor for this DC level.

The matching network should be designed to match the input impedance of Romeo2 to the required input impedance.

1. See the data sheet for the internal registers of Romeo2

RFIN low signal impedance is equivalent to:

$$Z_{in} = C_{in} // R_{in} = 1.4 \text{ pF} // 1.1 \text{ k}\Omega$$

and, with $F_{RFin} = 433.92 \text{ MHz}$

$$Z_{in} = 59.05 - j.247.9\Omega$$

and, with $Z_o = 50\Omega$

$$\Gamma_{in} = 0.916^{-21.652^\circ}$$

Definitions

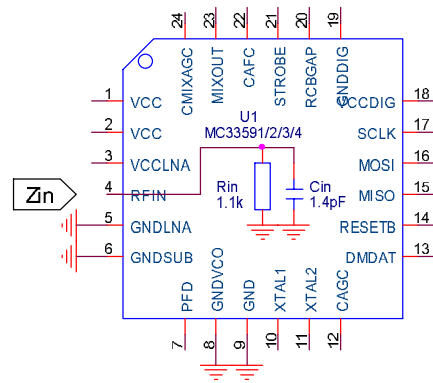
$$\Gamma_{in} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o}$$

$$Z_{in} = C_{in} // R_{in}$$

$$Z_{in} = \frac{R_{in} \cdot Z_{C_{in}}}{R_{in} + Z_{C_{in}}}$$

$$Z_{C_{in}} = \frac{1}{jC_{in}\omega}$$

$$\omega = 2\pi F$$



Γ_{RF}in Data

F (MHz)	Mod	Arg	F(MHz)	Mod	Arg	F(MHz)	Mod	Arg
100	0.913	-5.047	410	0.916	-20.484	720	0.921	-35.205
110	0.913	-5.551	420	0.916	-20.973	730	0.921	-35.663
120	0.913	-6.055	430	0.916	-21.461	740	0.921	-36.120
130	0.913	-6.558	433.92	0.916	-21.652	750	0.921	-36.576
140	0.913	-7.062	440	0.916	-21.948	760	0.921	-37.030
150	0.913	-7.565	450	0.916	-22.434	770	0.922	-37.483
160	0.913	-8.067	460	0.916	-22.920	780	0.922	-37.935
170	0.914	-8.570	470	0.917	-23.404	790	0.922	-38.386
180	0.914	-9.072	480	0.917	-23.888	800	0.922	-38.836
190	0.914	-9.573	490	0.917	-24.371	810	0.923	-39.284
200	0.914	-10.075	500	0.917	-24.853	820	0.923	-39.731
210	0.914	-10.576	510	0.917	-25.334	830	0.923	-40.177
220	0.914	-11.076	520	0.917	-25.814	840	0.923	-40.621
230	0.914	-11.576	530	0.917	-26.293	850	0.923	-41.065
240	0.914	-12.076	540	0.918	-26.771	860	0.924	-41.507
250	0.914	-12.575	550	0.918	-27.249	868.3	0.924	-41.873
260	0.914	-13.074	560	0.918	-27.725	870	0.924	-41.947
270	0.914	-13.572	570	0.918	-28.201	880	0.924	-42.387
280	0.914	-14.070	580	0.918	-28.675	890	0.924	-42.825
290	0.914	-14.567	590	0.918	-29.148	900	0.924	-43.262
300	0.915	-15.063	600	0.919	-29.621	910	0.925	-43.697
310	0.915	-15.559	610	0.919	-30.092	915	0.925	-43.914
320	0.915	-16.055	620	0.919	-30.562	920	0.925	-44.131
315	0.915	-15.807	630	0.919	-31.032	930	0.925	-44.564
330	0.915	-16.550	640	0.919	-31.500	940	0.925	-44.995
340	0.915	-17.044	650	0.919	-31.967	950	0.926	-45.425
350	0.915	-17.537	660	0.920	-32.433	960	0.926	-45.854
360	0.915	-18.030	670	0.920	-32.898	970	0.926	-46.281
370	0.915	-18.523	680	0.920	-33.361	980	0.926	-46.707
380	0.915	-19.014	690	0.920	-33.824	990	0.926	-47.132
390	0.915	-19.505	700	0.920	-34.286	1000	0.927	-47.555
400	0.916	-19.995	710	0.921	-34.746			

Practical Design

Any kind of matching network is possible, as long as it is carefully tuned on the board to correct errors due to parasitic coils or capacitors. It is not recommended to reuse a matching network without retuning it.

Important points:

- The matching network should not alter the DC level of RFIN
- Design the matching network for a loaded Q as low as possible (5 to 10)
- Use high-precision components (better than 5% tolerance), to avoid attenuation over dispersion
- Keep the connections between components short
- Connections to ground should be separate for each component; use a via connection to the lower side used as a ground
- Layout should be in line; avoid loops (coupling between input and output)
- The final value of each component should be found by accurately testing each of them and keeping, each time, the one that gives the highest sensitivity. You do not need a network analyzer; an RF generator will be sufficient.

Two matching networks for Romeo2 at 315 MHz and 433 MHz are shown in [Figure 2](#) and [Figure 3](#).

The tuning of the components should be done in the following order:

1. L1
2. C1
3. C2
4. C3

L1 has more effect on the final result than C1, C2, or C3.

The matching network in [Figure 2](#) is designed for 434 MHz, and the matching network in [Figure 3](#) is for 315 MHz.

For 434 MHz: C17 = 8.2 pF; L4 = 68 nH; C11 = 33 pF; C23 = 1 pF

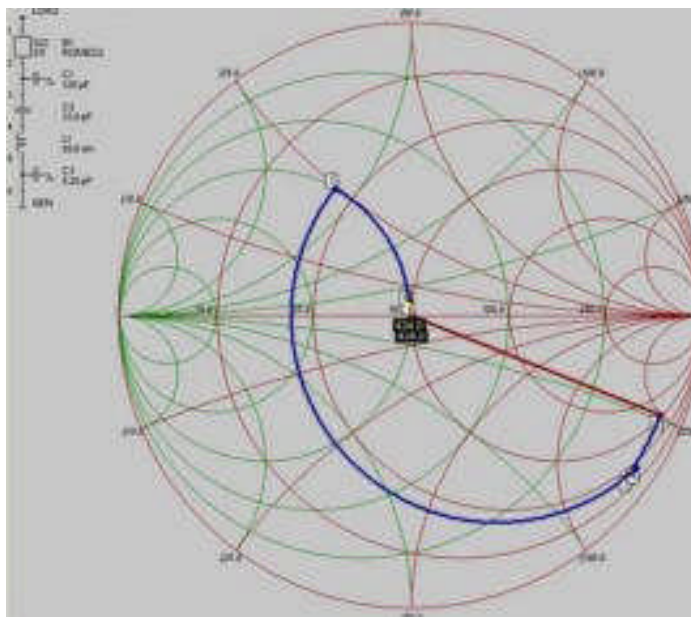


Figure 2. Matching Network Designed for 434 MHz

For 315 MHz: C17 = 10 pF; L4 = 120 nH; C11 = 12 pF; C23 = 1.5 pF

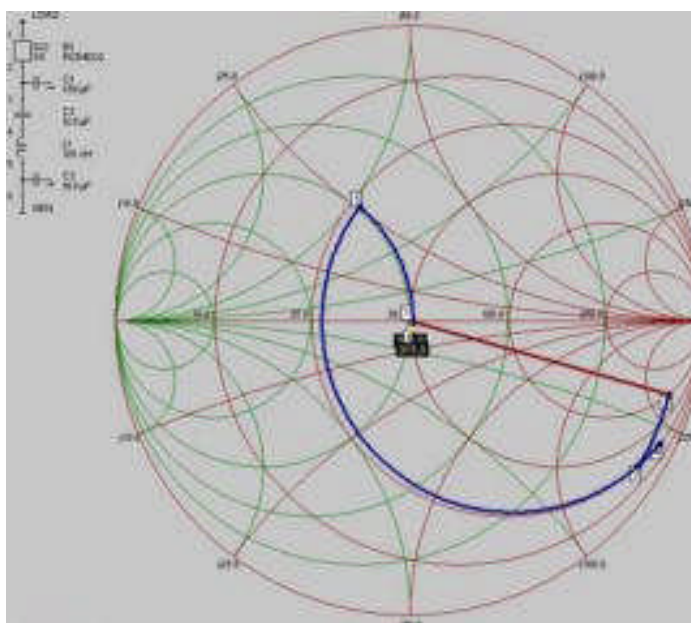


Figure 3. Matching Network Designed for 315 MHz

Additional Base Band Low-pass Filtering

For low data rates, it is possible to connect a capacitor to the DMDAT pin, to increase slightly the signal-to-noise ratio and, thus, the sensitivity of the system.

It is possible to improve the sensitivity to about 1dB at a 1200bps data rate.

For other data rates, C22 can be increased to:

$$C22 = \frac{5.64 \times 10^{-6}}{\text{DataRate}}$$

with DataRate in bits per second.

and C₂₂ in Farads.

Data Rate	C22
1200 bps	4.7 nF
2400 bps	2.2 nF
4800 bps	1 nF
9600 bps	560 pF

Automatic Gain Control in OOK

In OOK mode, C2 and C21 control the speed of the various AGCs. C2 controls the speed of the front end AGC, and C21 controls speed of the IF AGC.

Value	Attack time	Decay time
C2 = 10n F	4 μs (typical)	0.2 ms/dB (typical) – equivalent to 5 dB/ms for the Mixer AGC
C21 = 100 nF	75 μs (typical)	0.4 ms/dB (typical) – equivalent to 2.5 dB/ms for the IF Amplifier AGC

The attack and decay times are proportional to the values of the capacitors.

AGC and Data Rate

To avoid action of the AGC during the low level of the OOK signal that can reduce the sensitivity at low data rate, C21 can be optimized. (C2 has no effect on the sensitivity, as the front end AGC is used only for high level RF signals.)

Thus, the values given above are given for C21 = 100nF and DataRate = 4800 bps Manchester.

For other data rates, C21 can be increased to:

$$C21 = \frac{4.8 \times 10^{-4}}{\text{DataRate}}$$

with DataRate in bits per second

and C_{21} in Farads.

Data Rate	C21
1200 bps	390 nF
9600 bps	100 nF

C21 and Wakeup Time

Any optimization of C_{21} for data rates lower than 4800 bps will lead also to an increase of the wakeup time.

With $C_{21} = 100\text{nF}$, the wakeup time is 1 ms (typical) and 1.8 ms (maximum).

For other values, the wakeup time can be calculated:

$$t_{\text{wakeup.typ}} = C_{21} \cdot 10^4$$

with $t_{\text{wakeup.typ}}$ in seconds.

and C_{21} in Farads.

Data Rate	C21	$t_{\text{wakeup.typ}}$
1200 bps	390 nF	3.9 ms
9600 bps	100 nF	1 ms

FSK Demodulator

In FSK mode, C_{21} is part of an average low-pass filter that sets the level of the data slicer with an internal resistor $R_{\text{int}} = 8\text{k}$.

The value of C_{21} is linked to the data rate of the Manchester coded signal:

$$R_{\text{int}}.C_{21} = \frac{1}{\text{DataRate}}$$

Data Rate	C21
1200 bps	100 nF
9600 bps	12 nF

Internal Bandgap

An external resistor R_1 is used for the internal bandgap. Its value is fixed by design, and should be respected to guarantee the performance of Romeo2.

$R_1 = 180\text{k}$, 1%

Strobe Oscillator

R2 and C1 define the frequency of the internal strobe oscillator when J3 is in high impedance mode (the MCU lets the strobe oscillator run).

The period of the strobe oscillator is:

$$\tau_{strobe} = 0.12 \cdot R2 \cdot C1$$

R2 must be less than 2.2 MΩ, and C1 must be less than 330 nF.

When using the Data Manager, the period of the strobe oscillator and the value of the strobe ratio bits (SR0, SR1) must be selected carefully for Romeo2 to detect the incoming frame during RUN mode (at least eight bits of an ID, plus the wakeup time of Romeo2).

The MCU can control the state of the strobe oscillator (running or not) with R3 (optional), which can be fixed to 1k (not a critical value). This resistor limits the current sourced by the MCU to charge C1, and thus increases its reliability.

Automatic Frequency Control

An internal frequency control system is used to tune the IF filters to 660 kHz. An external capacitor defines the loop characteristics and filters the tuning voltage. Its value is not critical and is fixed by design at 100pF.

Equivalent Pin Schematics

The internal circuits connected to the pins of the device, including the diodes used for ESD protection, are shown in the following tables.

Pin No.	Symbol	Equivalent I/O Schematic
1	VCC	
2	VCC	
3	VCCLNA	

Pin No.	Symbol	Equivalent I/O Schematic
4	RFIN	
5	GND_LNA	
6	GND_SUB	

Pin No.	Symbol	Equivalent I/O Schematic
7	PFD	
8	GNDVCO	
9	GND	

Pin No.	Symbol	Equivalent I/O Schematic
10	XTAL1	
11	XTAL2	

Pin No.	Symbol	Equivalent I/O Schematic
12	CAGC	
13	DMDAT	

Pin No.	Symbol	Equivalent I/O Schematic
14	RESETB	
15	MISO	

Pin No.	Symbol	Equivalent I/O Schematic
16	MOSI	The schematic for Pin 16 (MOSI) shows a signal path starting from a MOSI input block. The signal passes through a 1k resistor, then through a series of two diodes connected to VCC and GND. It then passes through another 1k resistor, followed by a series of two diodes connected to VCC and GND. The signal then passes through an 8k resistor and is connected to a buffer or driver circuit. The circuit is powered by VCC and GND.
17	SCLK	The schematic for Pin 17 (SCLK) is identical to the one for Pin 16 (MOSI). It shows a signal path starting from an SCLK input block, passing through a 1k resistor, then through a series of two diodes connected to VCC and GND. It then passes through another 1k resistor, followed by a series of two diodes connected to VCC and GND. The signal then passes through an 8k resistor and is connected to a buffer or driver circuit. The circuit is powered by VCC and GND.
18	VCCDIG	The schematic for Pin 18 (VCCDIG) shows a signal path starting from a VCCDIG input block. The signal passes through a series of two diodes connected to VCC and GND. The circuit is powered by VCC and GND.

Pin No.	Symbol	Equivalent I/O Schematic
19	GNDDIG	The schematic for Pin 19 (GNDDIG) shows a pull-up resistor connected to VCC and a pull-down resistor connected to GND. The pin is also connected to a digital block GND.
20	RCBGAP	The schematic for Pin 20 (RCBGAP) shows a pull-up resistor connected to VCC and a pull-down resistor connected to GND. The pin is also connected to a 2k5 resistor.
21	STROBE	The schematic for Pin 21 (STROBE) shows a pull-up resistor connected to VCC and a pull-down resistor connected to GND. The pin is also connected to a 3k resistor and a transistor.

Pin No.	Symbol	Equivalent I/O Schematic
22	CAFC	
23	MIXOUT	

Pin No.	Symbol	Equivalent I/O Schematic
24	CMIXAGC	

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