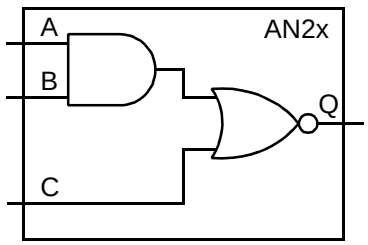
Description

AN2x is a family of AND-NOR circuits consisting of one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	Q
H	H	X	L
X	X	H	L
All other combinations			H

HDL Syntax

Verilog ..... AN2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AN2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AN21	AN22	AN24	AN26
A	1.0	1.0	1.0	2.1
B	1.0	1.0	1.0	2.1
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN21	2.0	TBD	2.1
AN22	3.0	TBD	6.4
AN24	4.0	TBD	7.7
AN26	7.0	TBD	14.6

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

AN21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.15 0.16	0.21 0.22	0.38 0.39	0.54 0.54	0.64 0.63
AN22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.39	0.47 0.50	0.59 0.63	0.74 0.79	0.86 0.91
AN24	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.40	0.49 0.52	0.60 0.63	0.70 0.75	0.81 0.88
AN26	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.40	0.50 0.52	0.59 0.63	0.69 0.73	0.79 0.82

Delay will vary with input conditions. See page 2-17 for interconnect estimates.