Using Terminator Technology in Stratix & Stratix GX Devices

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Introduction

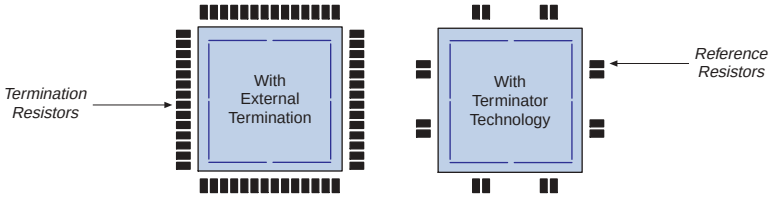
Signal integrity is crucial in high-speed digital designs because of increased system speeds and clock edge rates. Designers must properly terminate single-ended and differential signals to achieve signal integrity. Traditionally, designers use on-board termination resistors to achieve proper signal termination. However, these resistors take up significant board space and can cause signal reflections (stub effects). These reflections normally occur when a termination resistor is too far away from the transmission line it terminates.

Terminator™ technology in Stratix™ and Stratix GX devices helps prevent reflections, improving signal integrity. To address these issues, Stratix and Stratix GX devices have driver impedance matching and on-chip termination circuitry. Terminator technology includes series termination, impedance matching, parallel termination for single-ended I/O standards (e.g., HSTL and SSTL-2), and differential termination.

Termination resistors are adjacent to the buffers on the device, thereby eliminating stub effects. Terminator technology minimizes the need for a cumbersome external resistor network, thereby easing board routing and saving board space. Figure 1 shows a footprint comparison of a device with external termination and with Terminator technology.

This application note covers various Terminator technology types supported by Stratix and Stratix GX devices as well as power management.

Figure 1. Device Footprint Comparison with & without Terminator Technology



How Terminator Technology Works

Two external precision resistors (R_{UP} and R_{DN}) per V_{CCIO} bank are used as reference resistors. R_{UP} is a pull-up resistor connected to V_{CCIO}; R_{DN} is a pull-down resistor connected to GND. Terminator technology monitors the value of the two reference resistors and uses the value to adjust internal termination circuitry to the same impedance. In addition, Terminator technology circuitry compensates for voltage, temperature, and process variation. This circuitry continuously calibrates the internal termination resistors during normal device operation.

Terminator technology supports one type of I/O standard per I/O bank. You can enable or disable on-chip termination within an I/O bank on a pin-by-pin basis. To use different on-chip termination I/O standards on a device, select separate I/O banks. For example, if you want to use on-chip termination for GTL+ (3.3-V V_{CCIO}) and SSTL-3 class II (3.3-V V_{CCIO}), use two separate I/O banks.

Different I/O standards need different V_{CCIO} and V_{REF} voltages. You can simultaneously use some I/O standards with the same V_{CCIO} in an I/O bank. For more information, refer to *AN 201: Using Selectable I/O Standards in Stratix Devices*.

Series Termination Resistor (R_S)

Terminator technology provides an on-chip series termination resistor (R_S) for single-ended voltage-referenced I/O standard such as SSTL-2 and SSTL-3. The series termination value for these I/O standards is 25 Ω; the impedance matching value for these I/O standards is either 25 or 50 Ω. All I/O pins in Stratix and Stratix GX devices support this termination method. Table 1 shows the I/O standards supported for series termination and impedance matching.

Table 1. Supported I/O Standards for Series Termination & Impedance Matching

Feature	Supported I/O Standards	V_{CCIO} (V)
Series Termination	SSTL-3 class I	3.3
	SSTL-3 class II	3.3
	SSTL-2 class I	2.5
	SSTL-2 class II	2.5
Impedance Matching	LVTTL/LVCMOS	3.3
	LVTTL/LVCMOS	2.5
	LVTTL/LVCMOS	1.8

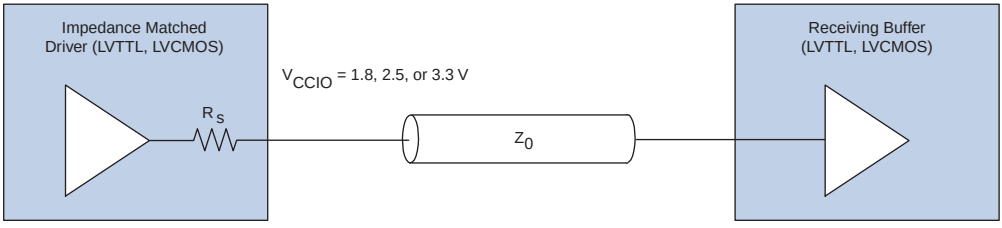
Impedance Matching

The impedance of the output driver is matched with the transmission line impedance. Stratix and Stratix GX output buffers can match output impedance to either 25 or 50 Ω. This impedance matching results in properly terminated signals, improving signal integrity. This feature is supported by all Stratix device I/O pins.

When using impedance matching for an output buffer, variable drive current strength and slow-slew rate features are not available.

Figure 2 shows the on-chip impedance matching resistor for an output driver.

Figure 2. Driver Impedance Matching



Parallel Termination (R_T)

Terminator technology supports on-chip parallel termination for several voltage-referenced I/O standards. To maintain signal integrity and save board space, use Terminator technology resistors instead of external pull-up termination resistors. Parallel termination is supported for SSTL-2, SSTL-3, HSTL (class I and II), GTL, GTL+, and CTT I/O standards. All the I/O pins in the top and bottom I/O banks support parallel termination. Figure 3 shows the parallel termination connections for a Stratix device.

Figure 3. Terminator Technology Parallel Termination

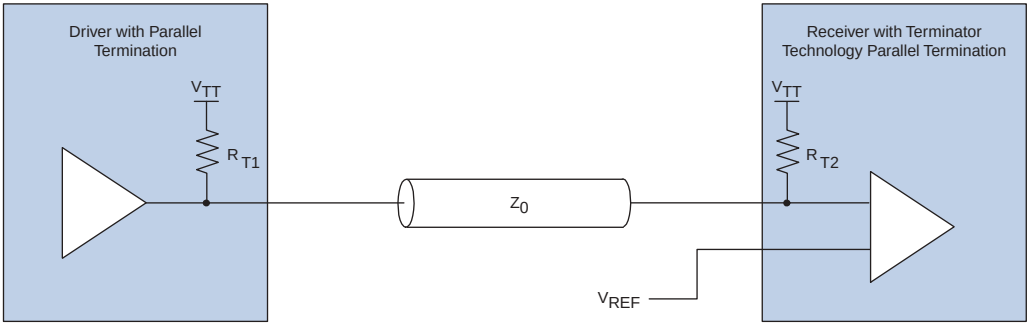


Table 2 shows the supported I/O standards for parallel termination in Stratix and Stratix GX devices.

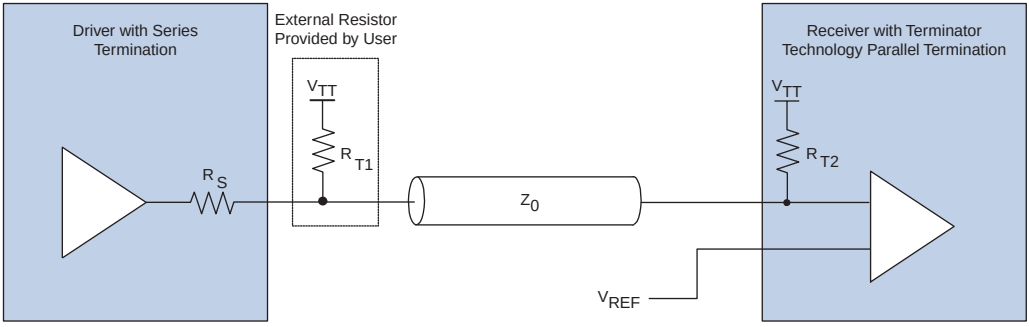
Table 2. Supported I/O Standards for Parallel Termination

Supported I/O Standards	Parallel Termination (R_{T1})	Parallel Termination (R_{T2})	V_{CCIO} (V)
SSTL-3 class I	N/A	50 Ω	3.3
SSTL-3 class II *(1)*	50 Ω	50 Ω	3.3
SSTL-2 class I	N/A	50 Ω	2.5
SSTL-2 class II *(1)*	50 Ω	50 Ω	2.5
HSTL class I	N/A	50 Ω	1.5
HSTL class II	50 Ω	50 Ω	1.5
GTL	50 Ω	50 Ω	3.3
GTL+	50 Ω	50 Ω	3.3
CTT	N/A	50 Ω	3.3

Note to Table 2:

(1) In addition to parallel termination, SSTL-3 and SSTL-2 class II I/O standards require a series termination next to the output buffer. If you are using these I/O standards for the output pins, Altera recommends using the on-chip series termination and an external pull-up resistor to V_{TT} for parallel termination. Figure 4 shows the connection scheme for these particular I/O standards.

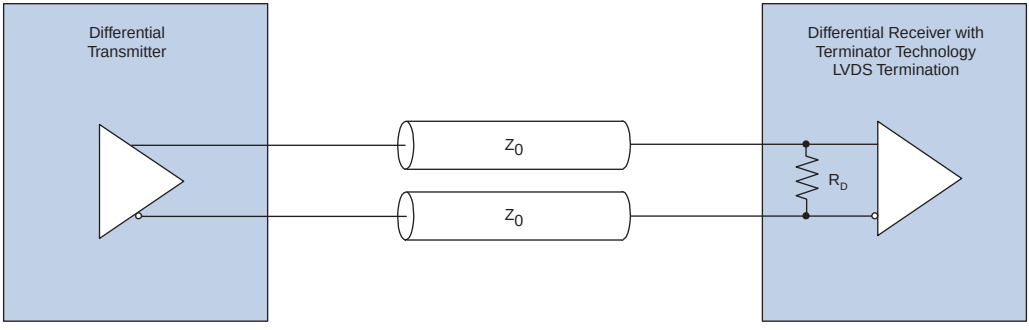
Figure 4. Terminator Technology Series-Parallel Termination



Differential Termination (R_D)

Terminator technology supports on-chip differential termination for source-synchronous LVDS signalling. The differential termination resistors are adjacent to the differential input buffers on the device. This placement eliminates stub effects, improving the signal integrity of the serial link. Using on-chip differential termination resistors also saves board space. Figure 5 shows the differential termination connections for Stratix and Stratix GX devices.

Figure 5. Terminator Technology Differential Termination



Differential termination for Stratix devices is supported for the left and right I/O banks. Differential termination for Stratix GX devices is supported for the left, source-synchronous I/O bank. Some of the clock input pins are in the top and bottom I/O banks, which do not support differential termination. External reference resistors are not required for I/O banks that support differential termination. The value of on-chip differential termination resistors is 100 Ω.

Transceiver Termination

Stratix GX devices feature built-in on-chip termination within the transceiver at both the transmit and receive buffers. This termination improves signal integrity and provides support for the 1.5-V PCML I/O standard.

See *AN 237: Using High-Speed Transceiver Blocks in Stratix GX Devices* for more information on transceiver termination.

Reference Resistors

Connect the two reference resistors (R_{UP} and R_{DN}) to the two dual-purpose reference pins per I/O bank. R_{UP} is a pull-up resistor and is connected to the V_{CCIO} of that I/O bank. R_{DN} is a pull-down resistor and is connected to GND of that I/O bank. Figure 6 below shows the reference resistor connections.

Figure 6. Terminator Reference Resistor Connections

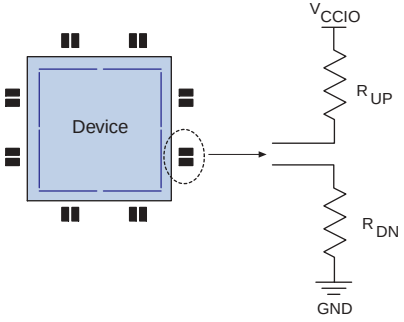


Table 3 shows the external reference resistor values for different types of terminations.

Table 3. External Reference Resistance Values *Note (1)*

Termination Type	Impedance (Ω)	R_{UP}/R_{DN}
Impedance Matching	25	$10 \times Z_0$
	50	$10 \times Z_0$
Series Termination	25	$10 \times Z_0$
Parallel Termination	50	$20 \times Z_0$
Differential Termination	100	Not needed

Note to Table 3:
(1) Z_0 is the target on-chip impedance.

Power Analysis

Terminator technology on-chip termination resistors increase the total current draw of the device. This increase in current draw occurs because the termination circuitry, which is normally external to the device, is now a part of the device. Make sure the device's current consumption in a design does not exceed any device limits. You must ensure that no more than 200 mA (Flip Chip packages) is consumed for any ten consecutive I/O pins (excluding VCC and GND pins). The Altera® Quartus® II software automatically performs these calculations during compilation. If the pin assignments do not comply with these conditions, the Quartus II software generates an error message during design compilation.

Table 4 lists the DC current draw when using on-chip series termination for single-ended I/O standards.

Table 4. DC Current Draw for On-Chip Series Termination

Bank I/O Standard Selected by Terminator Technology	DC Current Draw per Pin for Series Termination (I_{pin} in mA) *(1)*	V_{CCIO} (V)
LVTTL	0	1.8, 2.5, 3.3
LVCMOS	0	1.8, 2.5, 3.3
SSTL-2 class I	10	2.5
SSTL-2 class II	23	2.5
SSTL-3 class I	11	3.3
SSTL-3 class II	24	3.3

Note to Table 4:
(1) I_{pin} is the DC current drawn per pin.

Table 5 lists the DC current draw when using Terminator technology on-chip parallel termination resistors for single-ended inputs or outputs.

Table 5. DC Current Draw for On-Chip Series-Parallel Termination (Input & Output Pins) *Note (1)*

Bank I/O Standard Selected by Terminator Technology	DC Current Draw per Pin for Series & Parallel Termination (I_{pin} in mA) *(2)*			V_{CCIO} (V)
	Output Mode		Input Mode	
	R_S	R_{T1} *(3)*	R_{T2} *(3)*	
GTL	N/A	40	15	3.3
GTL+	N/A	34	14	3.3
SSTL-2 class I	10	N/A	12	2.5
SSTL-2 class II	23	N/A	12	2.5
SSTL-3 class I	11	N/A	15	3.3
SSTL-3 class II	24	N/A	17	3.3
CTT	N/A	N/A *(4)*	18	3.3
HSTL class I	N/A	N/A *(4)*	9	1.5
HSTL class II	N/A	20	10	1.5

Notes to Table 5:

(1) There are no current limitations for 1.8-V I/O standards (thermally-enhanced ball-grid array (BGA) cavity-up packages).

(2) I_{pin} is the DC current drawn per pin.

(3) R_{T1} and R_{T2} are the parallel termination resistors for the voltage-referenced I/O standards. R_{T1} is the parallel termination resistor next to the output buffer and R_{T2} is the parallel termination resistor next to the input buffer. See Figure 3.

(4) The CTT output buffer and HSTL Class I output buffer do not draw any current due to the on-chip termination resistor for single-ended I/O pins, but they will still draw 8 mA as specified in the corresponding JEDEC specifications.

When using bidirectional pins, the total DC current draw by Terminator technology on-chip termination resistors is different than the values listed in Table 5. Table 6 lists the DC current draw values for bidirectional pins.

Table 6. DC Current Draw for On-Chip Series-Parallel Termination (Bidirectional Pins) *Note (1)*

Bank I/O Standard Selected by Terminator Technology	DC Current Draw per Pin for Series & Parallel Termination (I_{pin} in mA) *(2)*			V_{CCIO} (V)
	R_S	R_{T1} *(3)*	R_{T2} *(3)*	
GTL	N/A	40	40	3.3
GTL+	N/A	34	34	3.3
SSTL-3 class I	11	N/A	25	3.3
SSTL-3 class II	24	N/A	37	3.3
SSTL-2 class I	10	N/A	19	2.5
SSTL-2 class II	23	N/A	25	2.5
CTT	N/A	N/A *(4)*	27	3.3
HSTL class I	N/A	N/A *(4)*	16	1.5
HSTL class II	N/A	20	20	1.5

Notes to Table 6:

(1) There are no current limitations for 1.5- and 1.8-V V_{CCIO} I/O standards.

(2) I_{pin} is the DC current drawn per pin.

(3) R_{T1} and R_{T2} are the parallel termination resistors for the voltage referenced I/O standards. R_{T1} is the parallel termination resistor next to output buffer and R_{T2} is the parallel termination resistor next to input buffer.

(4) The CTT output buffer and HSTL class I output buffer do not draw any current due to the on-chip termination resistor for single-ended I/O pins, but they will still draw 8 mA as specified in the corresponding JEDEC specifications.

When you enable Terminator technology for an I/O bank, the external reference resistors for that bank are activated. When enabled, these reference resistors also draw a finite amount of current. The current consumption of these resistors for different I/O standards is shown in the Table 7.

Table 7. R_{UP} & R_{DN} Current Consumption *Note (1)*

Bank I/O Standard Selected by Terminator Technology	R_{UP} & R_{DN} Current Consumption per I/O Bank (I_{ref} in mA) *(2)*		V_{CCIO} (V)
	Series Termination	Parallel Termination	
LVTTL/LVCMOS *(3)*	16	N/A	3.3
LVTTL/LVCMOS *(3)*	10	N/A	2.5
SSTL-2 class I	9	13	2.5
SSTL-2 class II	12	14	2.5
SSTL-3 class I	15	22	3.3
SSTL-3 class II	19	26	3.3
HSTL class I	N/A	5	1.5
HSTL class II	N/A	5	1.5
GTL	N/A	17	3.3
GTL+	N/A	17	3.3
CTT	N/A	24	3.3

Notes to Table 7:

(1) There are no current restrictions for the HSTL class I and class II I/O standards (thermally-enhanced BGA cavity-up packages).

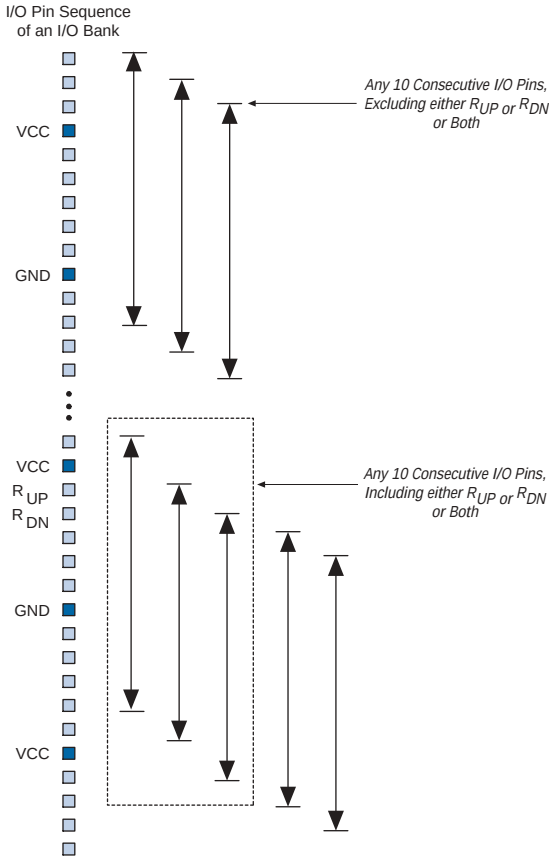
(2) I_{ref} is the current drawn by the Terminator technology control circuitry, including the external reference resistors R_{UP} and R_{DN}, per I/O bank.

(3) These values are the same whether you are using 250- or 500-Ω reference resistors.

Dual-purpose pins for connecting external reference resistors are also included while counting ten consecutive I/O pins. When using Terminator technology, Figure 7 shows a Stratix or Stratix GX device's current draw limitation guidelines.

For complete details on the current draw limits or any other limitations for different I/O standards, refer to *AN 201: Using Selectable I/O Standards in Stratix Devices*.

Figure 7. Current Draw Limitation Guidelines Using Terminator Technology



If the ten consecutive I/O pins exclude either R_{UP} or R_{DN} or both pins, the current draw limitations in thermally enhanced BGA packages cannot exceed 200 mA. Consult Altera Applications for current draw limit for all other packages.

For example, consider a case where the ten consecutive pins are configured as follows (only seven of the ten pins are used in this example):

- Number of SSTL-3 Class I output pins with Terminator technology = 3
- Number of GTL+ output pins without Terminator technology = 4

In this case, the total current draw for these ten consecutive I/O pins would be (see Tables 5 and 6 for values):

(# of SSTL-3 Class I pins with Terminator technology × 11 mA) + (# of GTL+ output pins × 34 mA) = (3 × 11 mA) + (4 × 34 mA) = 169 mA

In the above example, the total current draw for all ten consecutive I/O pins is less than 200 mA.

If the ten consecutive I/O pins also include either R_{UP} or R_{DN} or both pins, the current draw limitation for Stratix devices should be less than (200 mA - I_{ref}), where I_{ref} is the current drawn by either R_{UP} or R_{DN} or both.

For example, consider another case where the ten consecutive pins are configured as follows (nine of the ten pins are used in this example):

- Number of SSTL-3 Class II output pins with Terminator technology = 8
- Number of external reference resistor pins (R_{UP} and R_{DN}) = 1

In this case, the sum total of current draw for these ten consecutive I/O pins would be (see Tables 4 and 7 for values):

(# of SSTL-3 Class II output pins with Terminator technology × 25 mA) + (total current due to the Terminator technology, including external reference resistor pins R_{UP} and R_{DN}) = (8 × 24 mA) + (26 mA) = 218 mA

In the above example, the total current draw for all ten consecutive I/O pins is more than 200 mA. Therefore, this case is not allowed and the Quartus II software generates an error message during design compilation.

Design Tips

The following is a list of design tips:

- Parallel termination is supported only on the top and bottom I/O banks.
- Series termination and impedance matching is supported on all the I/O banks.
- Differential termination is supported only on the left and right I/O banks in Stratix devices and on the left I/O bank in Stratix GX devices.
- Transceiver termination is supported in the Stratix GX transceiver.
- Terminator technology supports one type of on-chip termination I/O standard for a given I/O bank.
- Some features, such as LVTTL variable drive strength and slow slew rate control, cannot be used when impedance matching is enabled.
- Each I/O bank has two dual-purpose reference pins to which two external reference resistors need to be connected when using Terminator technology.
- Each I/O pin can either support series or parallel termination. In the case of SSTL-2 class II and SSTL-3 class II output pins, Altera recommends using on-chip series termination and parallel external pull-up resistors.
- There are no current draw limitations for 1.8-V V_{CCIO} levels (thermally-enhanced BGA cavity up packages).
- Total current draw of ten consecutive I/O pins, including two dual-purpose pins for external reference resistors within these ten I/O pins, should not exceed 200 mA (thermally-enhanced BGA cavity up packages).

Conclusion

Increasing clock speeds and faster edge rates have made board design challenging. Designers must ensure that signal traces on the board are properly terminated to maintain signal integrity. Altera's Stratix and Stratix GX device families with Terminator technology offers impedance matching and on-chip termination resistors for single-ended and differential I/O standards. Terminator technology enables designers to meet signal integrity requirements while simplifying board design, saving time and resources.

Revision History

The information contained in *AN 209: Using Terminator Technology in Stratix & Stratix GX Devices* version 2.0 supersedes information published in previous versions. The following changes were made in *AN 209: Using Terminator Technology in Stratix & Stratix GX Devices* version 2.0

- Added Stratix GX devices throughout the document.
- Added *Note (1)* to Table 3.
- Added *Note (3)* to Table 7.

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