1.0 General Description

AMI Semiconductor's AMIS-720658 (PI6058) contact image sensor (CIS) is a selectable 600 or 300 dot per inch (dpi) resolution linear image sensor, which employs AMI Semiconductor's proprietary CMOS image sensing technology. The sensor contains an on-chip output amplifier, power down circuitry and parallel transfer features that are uniquely combined with the present-day active-pixel-sensor technology. The image sensors are designed to be cascaded end-to-end on a printed circuit board (PCB) and packaged in an image sensing module. Applications for the sensor array include facsimiles, PC scanners, check readers, and office automation equipment.

Figure 1 is a block diagram of the sensor. Each sensor consists of 344 active pixels, their associated multiplexing switches, buffers and an output amplifier circuit with a power down feature. The sensors pixel-pixel spacing is approximately 42.3µm. The size of each sensor without the scribe lines is 14560µm by 335µm.

2.0 Key Features

- 600 and 300dpi selectable resolutions
- 344 or 172 image sensor elements (pixels)
- 42.3µm (600dpi) pixel center-to-center spacing
- On-chip amplifier
- Single 3.3V power supply
- 3.3V input clocks and control signals
- 4.0MHz maximum pixel rate
- Parallel / integrate and transfer
- Power-down circuit
- High sensitivity
- Low power
- Low noise

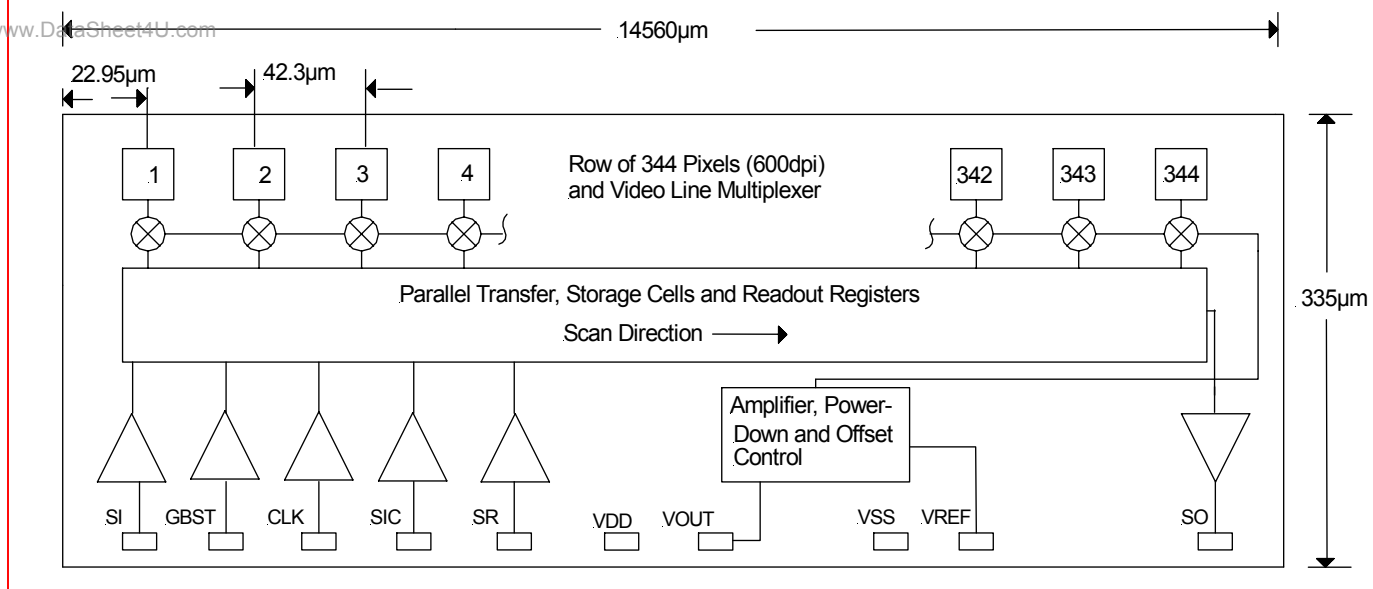


Figure 1: Sensor Block Diagram

3.0 Unique Features

There are six unique features incorporated into the AMIS-720658 which improve the sensor's performance.

3.1 Pixel-to-pixel Offset Cancellation Circuit

The sensor employs a pixel-to-pixel offset cancellation circuit, which reduces the fixed pattern noise (FPN), and amplifier offsets. In addition, this innovative circuit design greatly improves the optical linearity and low noise sensitivity.

3.2 Parallel Integrate, Transfer and Hold

The sensor has a parallel integrate, transfer and hold feature, which allows the sensor to be read out while photon integration is taking place. These features are approached through the use of an integrate-and-hold cell, located at each pixel site. Each pixel's charge is read from its storage site as the sensor's shift register sequentially transfers each pixel's charge onto a common video line.

3.3 Dual Scan Initiation Inputs, GBST and SI

Each sensor has two scan initiation inputs, the global start pulse (GBST) and the start pulse (SI), which are compatible with standard 3.3V CMOS clocks. These clocks help to reduce the sensor-to-sensor transition FPN by initializing and preprocessing all sensors simultaneously before they start their readout scan. The internal shift register starts the scan after GBST is clocked in on the falling edge of the clock input (CLK).

During the first 82 clock cycles following a GBST pulse, all the pixels of all the cascaded sensors cycle through their pre-scan initialization process that reduces FPN and reset noise.

A sequence of cascaded sensors has a unique first sensor and identically behaving subsequent sensors. The start input control (SIC) defines whether a sensor will be the first sensor that self-starts the readout of its pixels or will be a subsequent sensor that waits for the SI before starting the readout of its pixels. With its SIC tied high (Vdd), the first sensor self-starts the readout of its pixels after 82 clock cycles of delay. With their SIC tied low (Ground), all of the subsequent sensors delay their readout of their pixels until after they receive a SI pulse. Furthermore, the first sensor's SI is left unconnected, while the subsequent sensors all have their SI connected to the end-of-scan (SO) of their respective preceding sensor. Just prior to finishing its readout of its pixels, each sensor will send a SO pulse to its respective subsequent sensor so that its respective subsequent sensor will continue the readout of pixels without a pause or gap in readout. The external module-level start pulse (SP) is connected to all of the sensors' GBST inputs.

For example in the 600dpi mode, when the first sensor completes its scan, its SO appears on the rising edge of 416th clock cycle after the entry of GBST and the rising edge of the 11th last pixel, in order to have a continuous pixel readout between sensors in a module. This SO enters as the SI clock of the second and subsequent sensors; hence all subsequent sensors will start their register scan after each of the preceding sensors completes its scan.

3.4 Power Saving

Each sensor incorporates a power-saving feature when multiple sensors are cascaded together to form a linear imaging array. When a particular sensor is selected to be read out, the SIC on each sensor selects a unique feature of powering up that sensor's output amplifier and powering it down when not selected.

3.5 Common Reference Voltage Between Cascaded Sensors

Each sensor has an input bias control (VREF), which serves as an offset voltage reference. Each bias control pad is tied to its own amplifier's reference bias input. In operation, these pads on every sensor are connected together. Each sensor then "shares" the same bias level to maintain a constant bias among all of the sensors.

3.6 Selectable Resolutions of 600dpi and 300dpi

The select resolution input (SR) is connected to high (Vdd) or to low (Ground) to set the sensor to operate in the 600dpi or 300dpi mode, respectively. In the 600dpi mode, all 344 pixels are clocked out, whereas in the 300dpi mode, Pixels 1 and 2 are combined, 3 and 4 are combined and so on up to Pixels 343 and 344 being combined. One half of the pixel amplifiers and one half of the scanning

register are then disabled. As a result, sensitivity in the 300dpi mode will be twice that of the 600dpi mode. The 300dpi readout time will be approximately half of the 600dpi readout time. Unlike a CCD array, both the 300dpi and 600dpi arrays can operate with the same clock frequency.

4.0 Functional Description

4.1 Input / Output Terminals

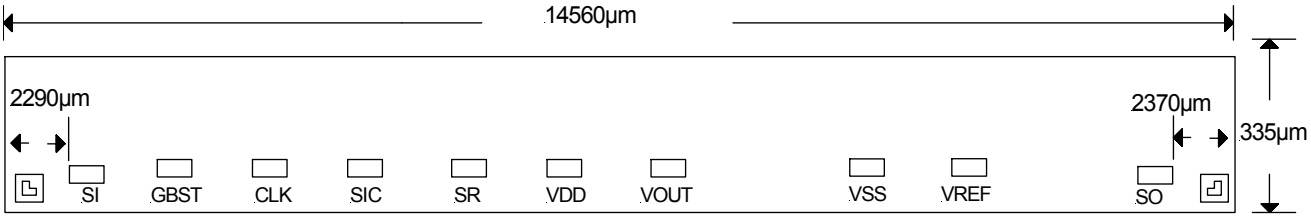
The AMIS-720658 image sensor has ten bond pads that become inter-connected when they are cascaded end-to-end on a PCB and packaged in an image sensing module. Their symbols and functions are listed in Table 1.

Table 1: Input and Output Terminals

Signal	I/O	Description
SI	I	Start pulse: Input to start a line scan (see discussion of the sensors unique features for further details)
GBST	I	Global start pulse: Globally initializes the start inputs of all sensors and starts the scanning process of the first sensor (see discussion of the sensors unique features for further details)
CLK	I	Clock: Clock input for the shift register
SIC	I	Start input control: Input to control the start pulse to the first sensor (see discussion of the sensors unique features for further details)
SR	I	Select resolution: Selects the 600 or 300dpi mode (see discussion of the sensors unique features for further details)
VDD	I	Power supply
VOUT	O	Video output voltage: Output video signal from the chip
VSS	I	Ground
VREF	I	Reference voltage: Externally applied reference input voltage for the amplifier output; sets the output's reset (dark) level
SO	O	End-of-scan pulse: Output from the shift register at the end of a scan

4.2 Bonding Pad Layout Diagram

Figure 2 shows the bonding pad locations for the AMIS-720658 sensor.

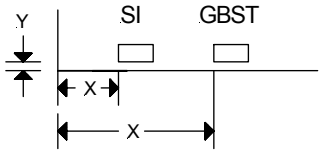


Pad Location Table

Pad	Location	Y	X
SI	Start Pulse	30.0	2290.0
GBST	Global Start Pulse	30.0	2637.0
CLK	Clock	30.0	3649.0
SIC	Start Input Control	30.0	3929.0
SR	Select Resolution	30.0	4243.0
VDD	Power Supply	34.0	4850.0
VOUT	Video Output Voltage	30.0	5135.0
VSS	Ground	34.0	9498.0
VREF	Reference Voltage	30.0	9844.0
SO	End of Scan Pulse	30.0	12190.0

Notes:

1. Definition of X and Y Pad Locations



2. Each pad is 80um x 70um
3. All dimensions are in um
4. Die size does not include the scribe line

Figure 2: AMIS-720658 Bonding Pad Layout

4.3 Wafer Scribe Line

Figure 3 outlines the scribe line dimensions surrounding the sensor die on a wafer.

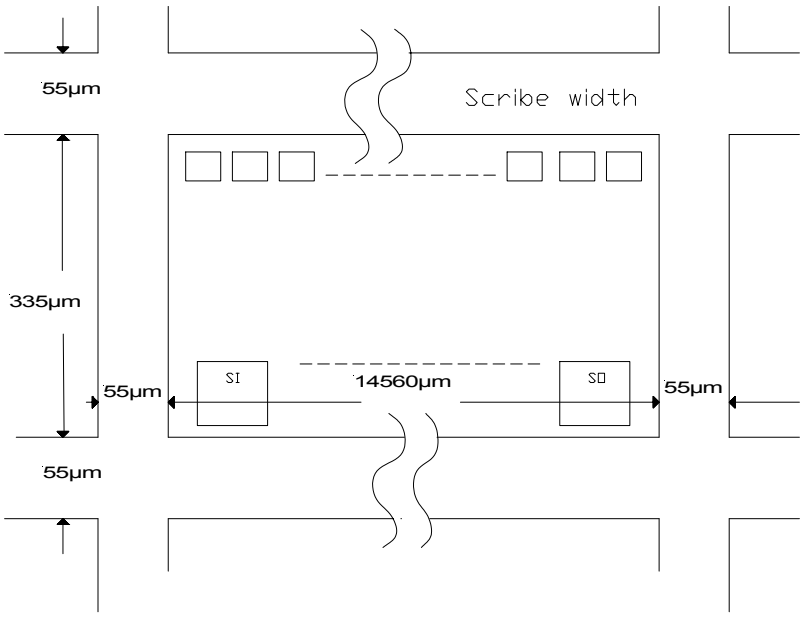


Figure 3: Wafer Scribe Line

5.0 Device Specifications

Table 2 lists the device specifications of the AMIS-720658 sensor operating under the typical values of the recommended operating conditions in table 3; pixel rate of 3.0MHz, temperature of 25°C, Vdd = 3.3V, VREF = 1.2V, integration time of 1.0ms for 300dpi and 2.0ms for 600dpi, no resistive load on Vout and with a capacitive load of 50pf on Vout to ground. The average output voltage Vpavg, which is defined as the voltage difference between the average pixel level in the light and the average pixel level in the dark, will be adjusted to approximately 0.7V, unless stated otherwise. A linear array of uniform green LED's will be used as the light source for measurements requiring illumination, unless otherwise stated.

Table 2: Device Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units
Number of pixels (1) @ 600dpi @ 300dpi		 344 172		 344 172	
Pixel-to-pixel spacing (1) @ 600dpi @ 300dpi		 42.3 84.6		 42.3 84.6	 µm µm
Pixel vertical height		25		25	µm
Dark output voltage level (2)	Vd		1.2		V
Dark output non-uniformity (3)	Ud			100	mV
Photo-response non-uniformity (4)	Up			±15	%
Adjacent photo-response non-uniformity (5)	Upn			±15	%
Sensor-to-sensor photo-response Non-uniformity (6)	Usensor			±10	%
Saturation voltage (7)	VSat	0.95			V
Sensitivity (8) @ 600dpi @ 300dpi	Sv		 750 1500		 V / uJ / cm^2 V / uJ / cm^2
Photo response linearity (9)	PRL	−2.5		+2.5	%
Individual pixel noise (rms) (10) @ 600dpi	P_noise		3.0	10	mV
Image lag (chip average)				2	%
Power supply current	IDD per chip		60	80	mA
Wafer thickness		325	350	375	µm

Notes

1. The SR input is connected to high (Vdd) or to low (ground) to set the sensor to operate in the 600dpi or 300dpi mode, respectively. In the 600dpi mode, all 344 pixels are clocked out, whereas in the 300dpi mode, Pixels 1 and 2 are combined, 3 and 4 are combined and so on up to Pixels 343 and 344 being combined. One half of the pixel amplifiers and one half of the scanning register are then disabled. As a result, sensitivity in the 300dpi mode will be twice that of the 600dpi mode. The 300dpi readout time will be approximately half of the 600dpi readout time.
2. Dark output voltage (Vd). Vd is the average dark output level and is essentially the offset level of the video output in the dark. The dark level is set by the voltage on VREF and which must be applied externally, to a voltage of 1.2V for optimal module operation.
3. Dark output non-uniformity (Ud). Ud = Vdmax – Vdmin, where Vdmax is the maximum pixel output voltage in the dark and Vdmin is the minimum pixel output voltage in the dark.
4. Photo-response non-uniformity (Up). Up = ((Vpmax-Vpavg)/Vpavg) x 100% or ((Vpavg-Vpmin)/Vpavg) x 100%, whichever is the greater, where Vpmax is the maximum pixel output voltage in the light, Vpmin is the minimum pixel output voltage in the light and Vpavg is the average output voltage of all pixels in the light.
5. Adjacent photo-response non-uniformity (Upn). Upn = [Max(Vpn, Vpn+1) - Min(Vpn, Vpn+1)) / Min(Vpn, Vpn+1)) x 100%, where Vpn is the pixel output voltage of pixel n in the light and Vpn+1 is the pixel output voltage of pixel n+1.
6. Sensor-to-sensor photo-response non-uniformity (Usensor). Usensor = (Vpavg – Wavg) / Wavg, where Wavg is the average output of all sensors on the same wafer that pass all other specifications.
7. Saturation voltage (Vsat) is defined as the maximum video output voltage swing measured from the dark level to the saturation level. It is measured by using the module LED light source with the module imaging a uniform white target. The LED light level is increased until the output voltage no longer increases with an increase in the LED brightness. The dark level is set by the voltage on VREF and which must be applied externally, to a voltage of 1.2V for optimal module operation.
8. Sensitivity (Sv) is defined as the slope of the Vpavg vs. Exposure curve.
9. Photo-response linearity (PRL). PRL = ((Vratio – Tratio) / Tratio) x 100% where Vratio = (Vavg2 – Vavg1) / (Vavg3 – Vavg1), Tratio = (Tint2 – Tint1) / (Tint3 – Tint1), Vavg1 is the average output voltage of all pixels under fixed illumination with an integration time of Tint1 selected so that Vavg1 is around 0.1 V, Vavg2 is the average output voltage of all pixels under the same fixed illumination with an integration time of Tint2 selected so that Vavg2 is around 0.4 V, Vavg3 is the average output voltage of all pixels under the same fixed illumination with an integration time of Tint3 selected so that Vavg3 is around 0.7 V.
10. Individual pixel noise in rms (P_noise). The individual pixel noise in rms is defined as the standard deviation of each pixel in the dark. This can also be though of as output referred noise as it is measured at the sensor output.

6.0 Recommended Operating Conditions

Table 3 lists the recommended operating conditions at 25°C.

Table 3: Recommended Operating Conditions at 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply	Vdd	3.1	3.3	3.5	V
Clock input voltage high level (1)	Vih	2.8			V
Clock input voltage low level (1)	Vil			0.5	V
Reference voltage (2)	VREF	1.1	1.2	1.3	V
Clock frequency (3)		0.5	3.0	4.0	MHz
Pixel rate (4)		0.5	3.0	4.0	MHz
Integration time (line scan rate) (5) First die Subsequent die	Tint	 107 86			 µs µs / die
Clock pulse duty cycle (6)			50		%
Resistive load on Vout		5			KΩ
Capacitive load on Vout			50		pF

Notes:

1. Applies to all clocks; GBST, SI and CLK.
2. The dark level is set by the voltage on VREF and which must be applied externally, to a voltage of 1.2V for optimal module operation.
3. Although the device will operate with a pixel rate of less than 500 kHz, it is recommended that the device be operated above 500 kHz to maintain performance characteristics. Operating below 500 kHz may result in leakage current degradation.
4. One pixel is clocked out for every clock cycle.
5. Tint is the integration time of a single sensor and is the time between two start pulses. The minimum integration time is the time it takes to clock out 82 inactive pixels and 344 active pixels for the 600dpi mode, or 82 inactive pixels and 172 active pixels for the 300dpi mode, at a given frequency.

   However, if several sensors are cascaded together in a module then the minimum integration time for the 600dpi mode is the time it takes to clock out 82 inactive pixels and 344 active pixels from the first sensor and 344 pixels from each of all subsequent sensors, at a given frequency.

   Similarly, for cascaded sensors in the 300dpi mode, the minimum integration time is the time it take to clock out 82 inactive pixels and 172 active pixels from the first sensor and 172 pixels from each of all subsequent sensors, at a given frequency.

6. The clock duty cycle is defined as the ratio of the positive duration of the clock to its period.

7.0 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Parameter	Symbols	Max.	Units
Power supply voltage (Vdd)	Vdd	8	V
Clock input voltage high level (Vih) (1)	Vih	Vdd + 0.3	V
Clock input voltage low level (Vil) (1)	Vil	-0.3	V
Operating temperature		-10 to +50	°C
Operating humidity		+10 to +85	RH%
Storage temperature		-25 to +75	°C
Storage humidity		+10 to +90	RH%

Note:

1. Applies to all clocks.

8.0 Timing Requirements

Table 5 lists the timing requirements for the 600 and 300dpi modes, and their associated timing diagrams are shown in Figures 4-10. All measurements were taken at a pixel rate of 3 MHz, integration time of 2ms, Vout of 0.7V, no resistive load on Vout and with a capacitive load of 50pf on Vout to ground.

Table 5: Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Units
Clock (CLK) period	CLKp		330		ns
Clock (CLK) pulse width	CLKpw		165		ns
Clock (CLK) duty cycle			50		%
Data setup time (1)	Tset	20			ns
Data hold time (1)	Thold	25			ns
Clock (CLK) rise time (2)	CLKrt		35		ns
Clock (CLK) fall time (2)	CLKft		30		ns
End-of-scan (SO) rise time (2)	SOrt		50		ns
End-of-scan (SO) fall time (2)	SOft		50		ns
Global start (GBST) rise time (3)	GBSTrt		35		ns
Global start (GBST) fall time (3)	GBSTft		30		ns
Pixel transition time (4)	ptt		155		ns

Notes:

1. The shift register will load on all falling CLK edges, so setup and hold times (Tset, Thold) are needed to prevent the loading of multiple start pulses. This would occur if the GBST remains high during two fallings edges of the CLK signal. See Figure 7.
2. SI starts the register scanning and the first active pixel is read out on the 83rd clock of the CLK signal. However, when multiple sensors are sequentially scanned, as in CIS modules, the SO from the predecessor sensor becomes the SI to the subsequent sensor, hence the SI clock = the SO clock.
3. As discussed under the third unique feature, the GBST starts the initialization process and preprocesses all sensors simultaneously in the first 82 clock cycles before the first pixel is scanned onto the video line from the first sensor.
4. The transition between pixels does not always reach the dark offset level as shown in the timing diagrams, see Vout. The timing diagrams show the transition doing so for illustration purposes; however a stable pixel sampling point does exist for every pixel. The pixel transition time (ptt) shows the time when you cannot sample the pixel.

Figures 4 and 5 show the initialization of the first sensor in relation to its subsequent cascaded sensors. The SIC selects the first sensor to operate with 82 clock cycles of delay by connecting it to Vdd on the first sensor and to Ground for all of the subsequent sensors, hence the first sensor will operate with 82 inactive pixels being clocked out before its first active pixel is clocked out.

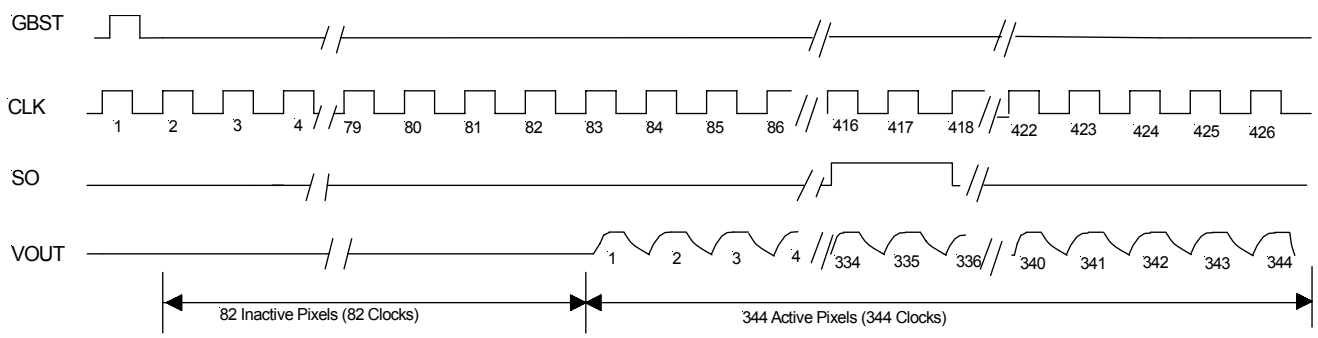


Figure 4: Overall Timing Diagram for the 600dpi Mode

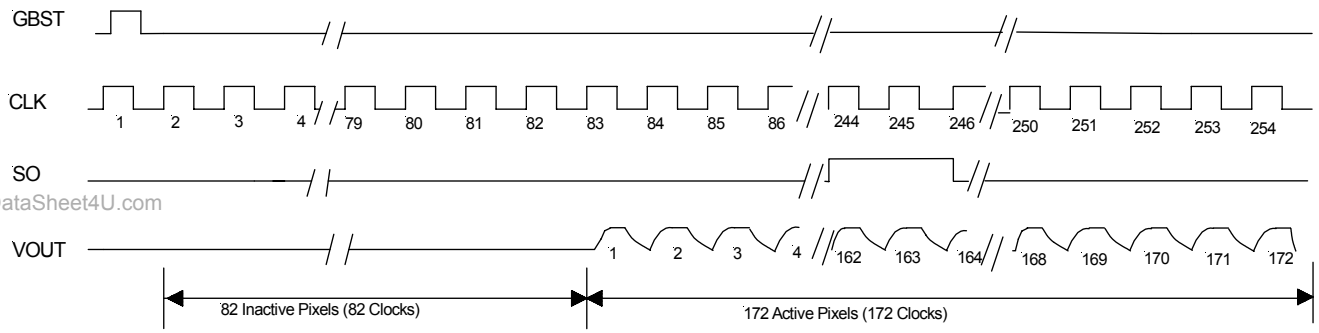


Figure 5: Overall Timing Diagram for the 300dpi Mode

Figures 6 and 7 detail the timing of the CLK, GBST, Vout, and SI/SO signals in further detail, which have the same timing requirements for both the 600 and 300dpi modes. The rise and fall times are listed in Table 5. In Figure 7, note that Pixel 83 is the first active pixel, as the first 82 pixels are dummy pixels.

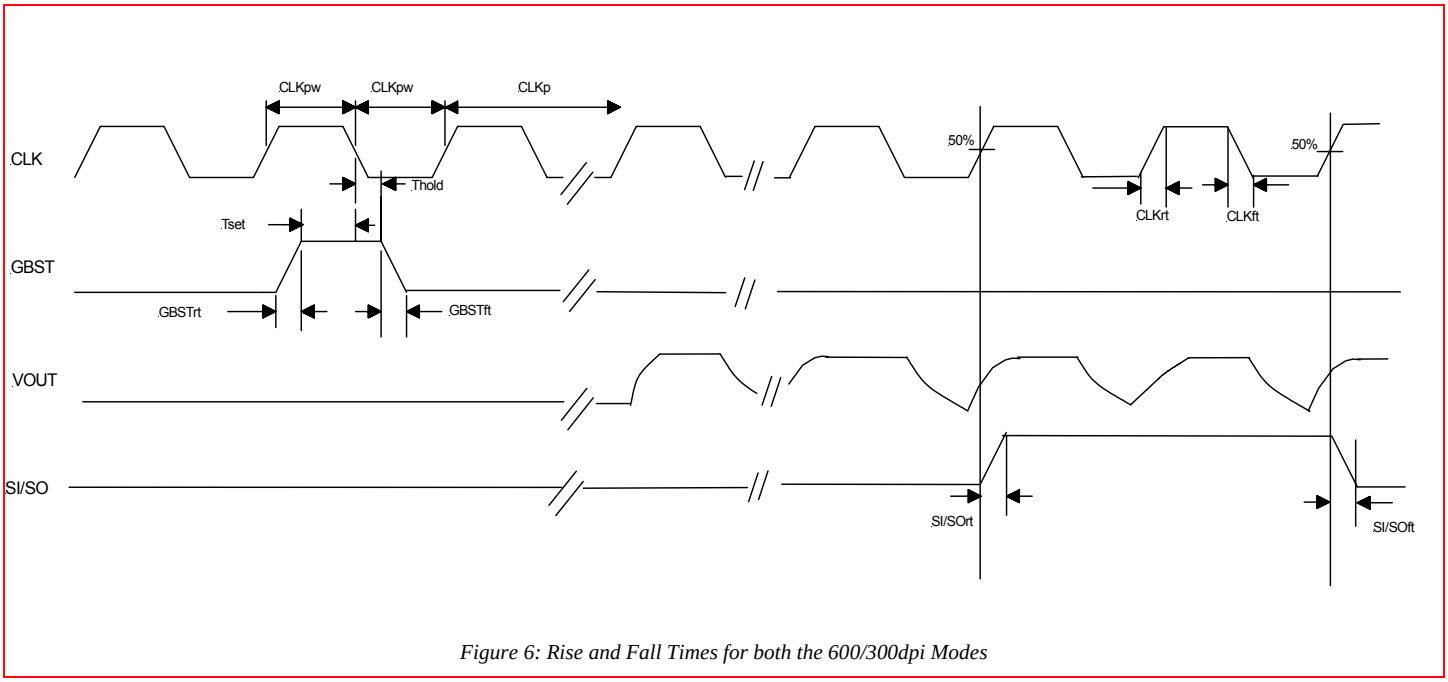


Figure 6: Rise and Fall Times for both the 600/300dpi Modes

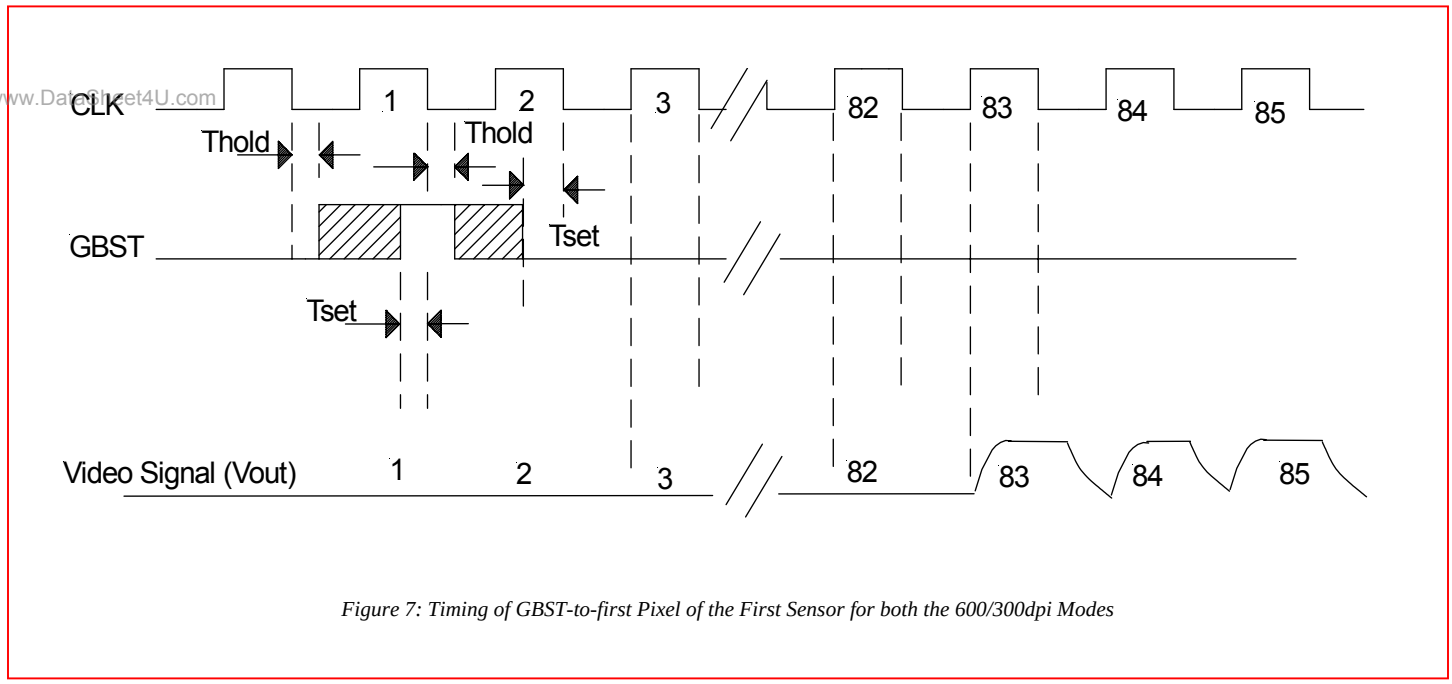


Figure 7: Timing of GBST-to-first Pixel of the First Sensor for both the 600/300dpi Modes

Figure 8 shows the timing of a single pixel. The pixel transition time (ptt) is shown, which is time during which the pixel cannot be sampled.

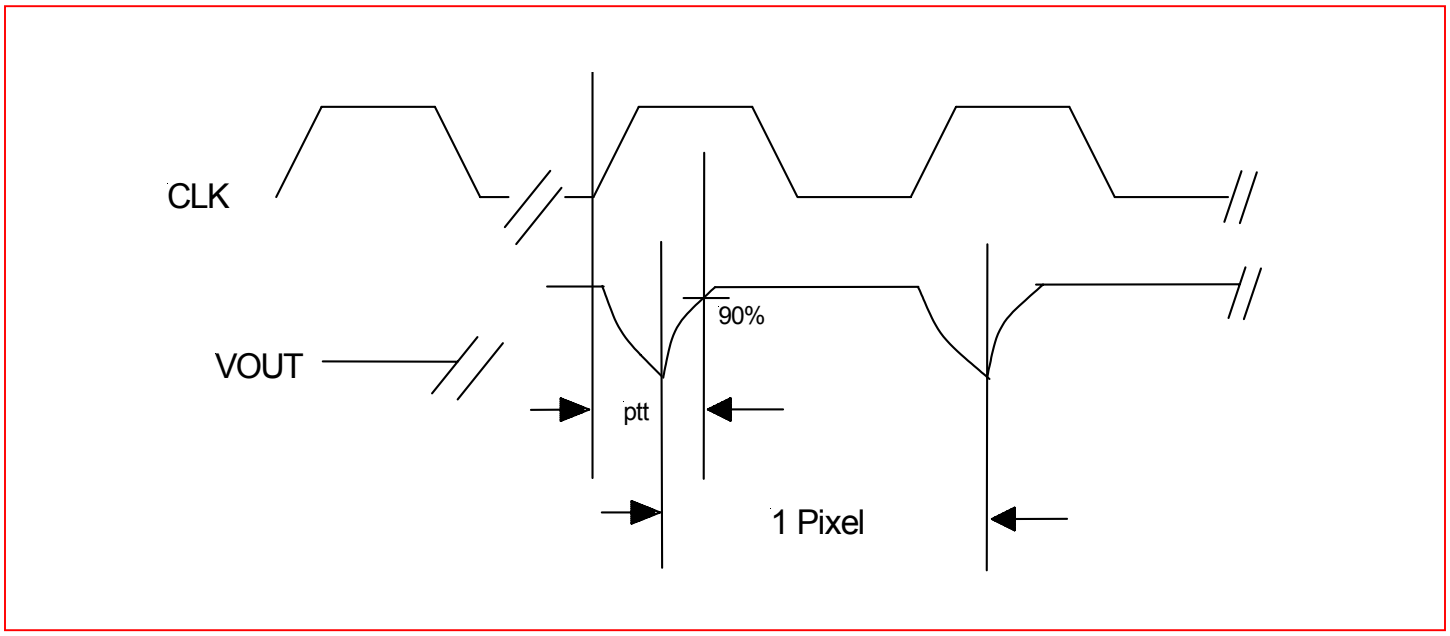


Figure 8: Pixel Timing

Figures 9 and 10 show the timing of the SI/SO, which comes out in line with the 334th pixel for the 600dpi mode and the 162nd pixel for the 300dpi mode. The SO from the first sensor enters as the SI clock of the second and subsequent sensors, hence all subsequent sensors will start their register scan after each of the preceding sensors completes its scan.

The last active pixel of each sensor is the 344th pixel for the 600dpi mode and 172nd pixel for the 300dpi mode.

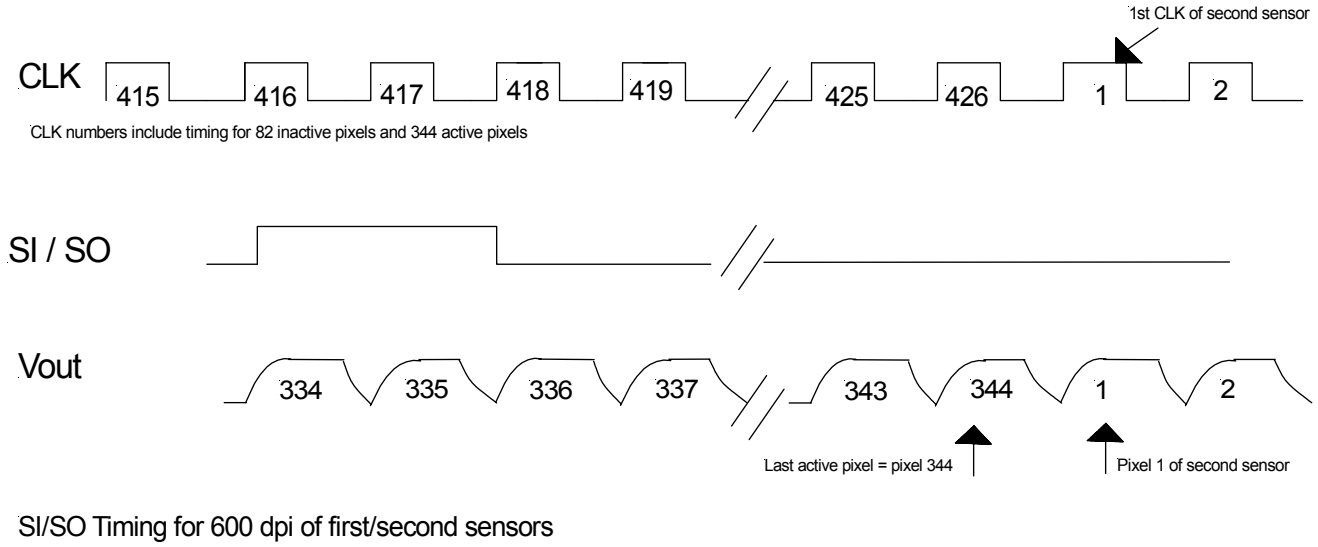


Figure 9: Timing of SI/SO Clock for the 600dpi Mode

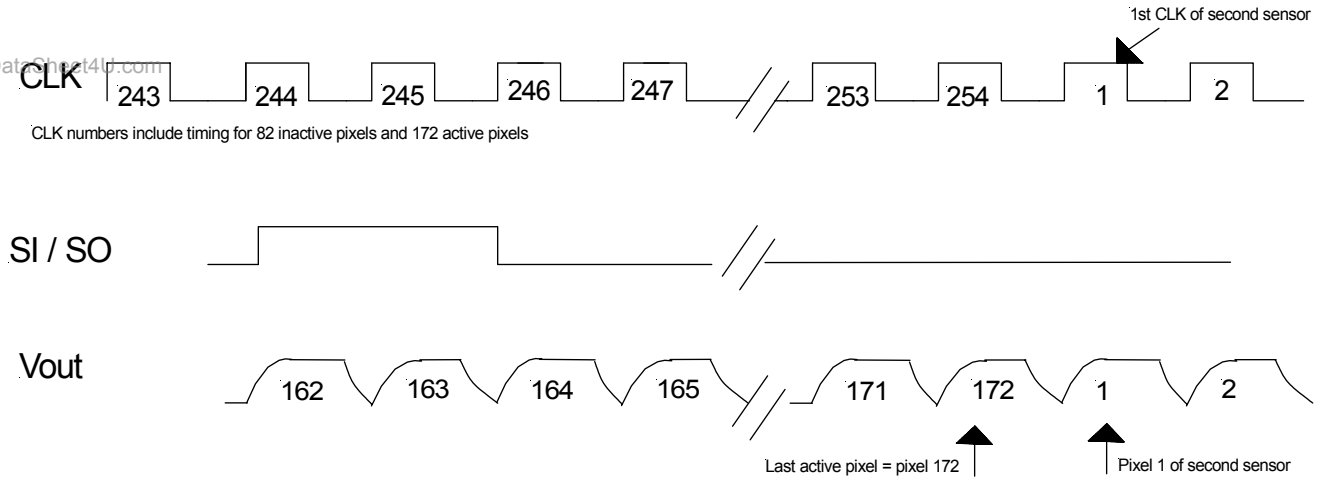


Figure 10: Timing of SI/SO Clock for the 300dpi Mode

9.0 Example of a CIS Module Using Cascaded AMIS-720658 Image Sensors

Figure 11 shows the proposed PCB schematic of the 15 chip CIS module.

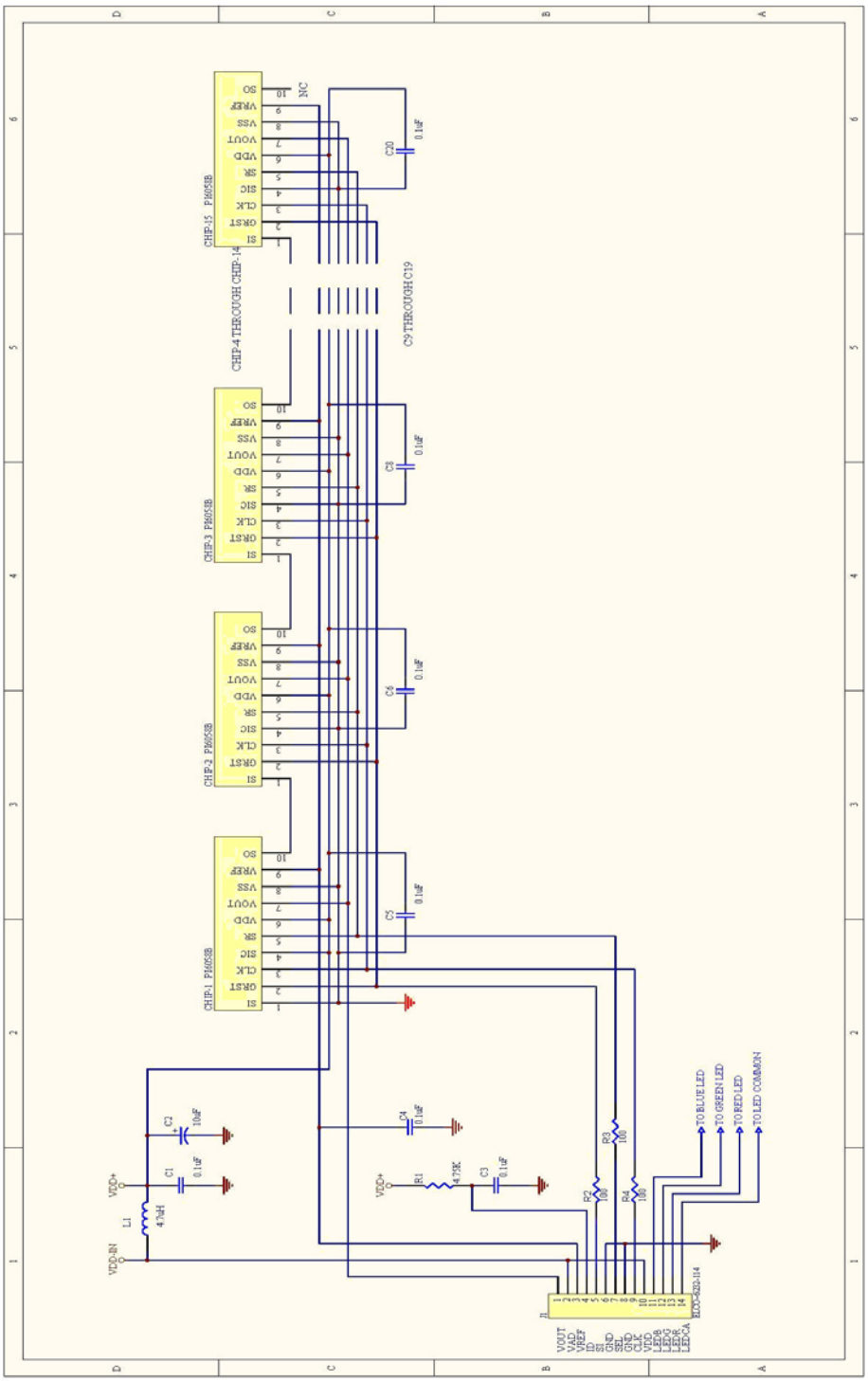


Figure 11: CIS Module with AMIS-720658 Image Sensors

9.1 Parameters to be Confirmed

- Sensitivity

10.0 Company or Product Inquiries

For more information about AMI Semiconductor's image sensors, please send an email to image_sensors@amis.com.

For more information about AMI Semiconductor's products or services visit our Web site at http://www.amis.com.