1.0 General Description

The AMIS-710625-A6 (PI625MC-A6) is a contact imaging sensor (CIS) module, which is composed of 13 AMIS-720639 (PI3039) sensor chips. The AMIS-720639 is a 600dpi solid-state line imaging array, also a product of AMI Semiconductor. This imaging device is fabricated using MOS imaging sensor technology for high-speed performance and high sensitivity. The AMIS-710625-A6 is suitable for scanning A6 size (104mm) documents with 23.62 dots per millimeter (dpm) resolution. Applications include ticket, check and card scanners, a variety of mark readers, and other automation equipment.

2.0 Key Features

- Light source, lens and sensor are integrated into a single module
- 23.62 dots/mm resolution, 104mm scanning length
- Up to 500μs ec/line scanning speed, with 5MHz pixel rate
- Wide dynamic range
- Analog output
- Red 660nm LED light source
- Compact size ≅ 14mm x 19.5mm x 120mm
- Low power
- Light weight

3.0 Functional Description

The AMIS-710625-A6 imaging array consists of 13 sensors that are cascaded to provide 2496 photo-detectors with their associated multiplex switches, and a digital shift register that controls its sequential readout. Mounted in the module is one-to-one graded indexed micro lens array that focuses the scanned documents to image onto its sensing plane. The on-board amplifier processes the video signal to produce a sequential stream of video at the video output pin of the AMIS-710625-A6 module.

Illumination is by means of an integrated LED light source. All components are housed in a small plastic housing which has a cover glass that acts as the focal point for the object being scanned and protects the imaging array, micro lens assembly and LED light source from dust. I/O to the module is the 10-pin connector located on one end of the module.

The cross section of the AMIS-710625-A6 is shown in Figure 1 and its block diagram in Figure 2.

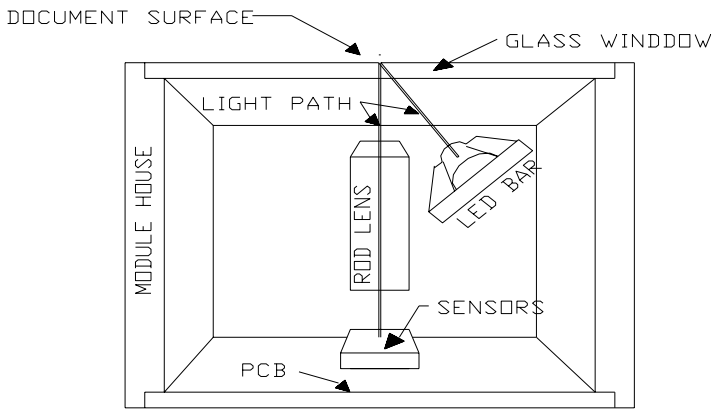

Figure 1: AMIS-710625-A6 Cross Section

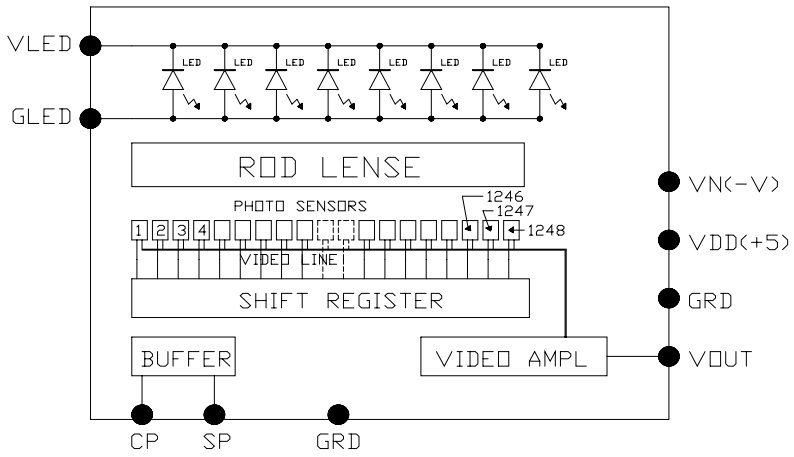

Figure 2: AMIS-710625-A6 Module Block Diagram

4.0 Connector Pin Out Designation

Connector is JAE part number 1L-Z-10P-S125L3-E.

Table 1: Pin Out Configuration

Pin Number	Symbol	Names and Functions
1	Vout	Analog video output
2	Gnd	Ground; 0V
3	Vdd (+5V)	Positive power supply
4	Vn (-5V to –12V)	Negative power supply
5	Gnd	Ground; 0V
6	SP	Shift register start pulse
7	Gnd	Ground; 0V
8	CP	Sampling clock pulse
9	GLED	Ground for the light source; 0V
10	VLED	Supply for the light source

5.0 Maximum Ratings

Table 2: Maximum Ratings

Parameter	Symbols	Max. Rating	Units
Power supply voltage	Vdd	7	V
	Idd	50	mA
	Vn	-15	V
	In	10	mA
	VLED	5.5	V
	ILED	500	mA
Input clock pulse (high level)	Vih	Vdd – 0.5V	V
Input clock pulse (low level)	Vil	-0.5	V

Note: These are the maximum values and are not to be used in a prolonged condition.

6.0 Operating Environment

Table 3: Operating Environment

Parameter	Symbols	Max. Rating	Units
Operating temperature	Top	0 to +50	^{0}C
Operating humidity	Hop	+10 to +85	%
Storage temperature	Tstg	-25 to+75	^{0}C
Storage humidity	Hstg	+5 to +95	%

7.0 Electro-Optical Characteristics

The tabled values are measured at 25°C

Table 4: Electro-Optical Characteristics at 25°C

Parameter	Symbol	Typical	Units	Note
Number of photo detectors		2496	Elements	
Pixel-to-pixel spacing		42.3	µm	
Line scanning rate (1)	Tint	500	µsec	@ 5.0MHz clock frequency
Clock frequency (2)	fclk	5.0	MHz	
Bright output voltage (3)	Video output	1.0 +/-0.1	V	
Bright output non-uniformity (4)	Up	<+/-30	%	
Adjacent pixel non-uniformity (5)	Uadj	<25	%	
Dark non-uniformity (6)	Ud	<100	mV	
Dark output voltage (6)	Vd	<450	mV	
Modulation Transfer function (7)	MTF	>40	%	

Notes:

1. Tint: Line scanning rate or integration time; tint is determined by the interval of two SP.
2. fclk: main clock frequency.
3. Vpavg = ∑ Vp(n)/2496; where n=1, 2, 3...., 2496.
4. Up = [(Vpmax - Vpavg) / Vpavg] x 100% or [(Vpavg - Vpmin) / Vpavg] x 100%, where Vpmax = the maximum V(n) and Vpmin = the minimum V(n).
5. Upadj = MAX[| (Vp(n) - Vp(n+l) | / Vp(n)] x 100%.
   Upadj is the non-uniformity in percent between adjacent pixels, where Vp(n) is the n^{th} pixel in the line scan.
6. Ud = Vdmax – Vdmin.
   Vd = the average dark output level.
   Vdmin is the minimum output on a black document (LED is turned off).
   Vdmax: maximum output voltage of black document (LED is turned off.)
7. MTF = [(Vpmax - Vpmin) / (Vpmax + Vpmin)] x 100 [%]; tested on a 300 lp/inch target.
   Vmax: maximum output voltage at 50lp/in and Vmin: minimum output voltage at 50lp/in, where lp/in is the line pairs per inch.

8.0 Recommended Operating Conditions

The tabled values are measured at 25°C.

Table 5: Recommended Operating Conditions at 25°C

Parameter	Symbol	Min.	Mean	Max.	Units
Power supply	Vdd	4.5	5.0	5.5	V
	Vn.	-4.5	-5	-12	V
	VLED		5		V
	Idd	26	30	34	ma
	Ivn		6.0	10.0	ma
	ILED		450	500	ma
Input voltage at digital high	Vih	Vdd-1.0	Vdd-.5	Vdd	V
Input voltage at digital low	Vil	0		0.8	V
Clock frequency (1)	fclk			5.5	MHz
Clock pulse high duty cycle		25			%
Clock pulse high duration		50			ns
Integration time (1)	Tint	0.25		5.0	ms
Operating temperature	Top		25	50	°C

Note:

1. Electrically, including the image sensors, the circuits will operate above 5.5MHz with tint at 455µs. However the light power is fixed, hence with the shorter integration time, the exposure is reduced. This reduction limits the specification call out to integration time of 500µs at 5.0MHz for 1.0V output.

9.0 Timing Characteristics

The timing characteristics for the I/O clocks are shown in Figure 3. See the timing symbol definitions in Table 6. The listed values are measured at ~25°C.

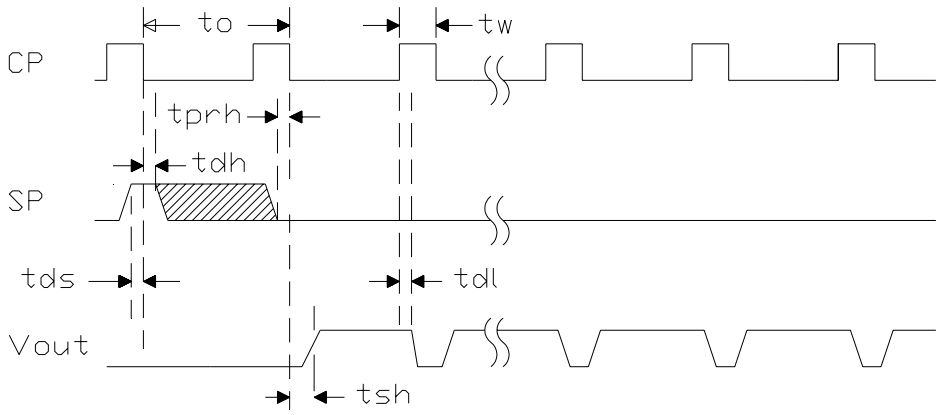

Figure 3: Timing Diagram

Table 6: Timing Symbol Definitions for Figure 3

Parameters	Symbol	Min.	Typ.	Max.	Units
Clock cycle time	to	0.182		10000	µs
Clock pulse width	tw	45			ns
Clock duty cycle		25		75	%
Prohibit crossing time of start pulse	tprh	84			ns
Data setup time	tds	86			ns
Data hold time	tdh	94			ns
Signal delay time	tdl	50			ns
Signal settling time	tsh	98			ns

10.0 AMIS-710625-A6 Module and Its Mechanical Dimensions

This is an overview drawing of the module. A full size drawing is available upon request.

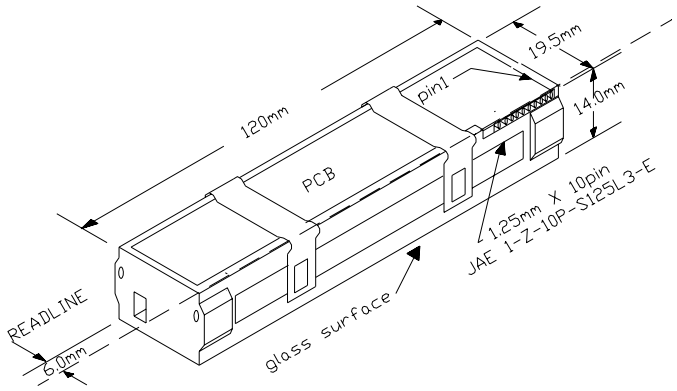

Figure 4: Overall View of the Module Housing

11.0 Company or Product Inquiries

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