1.0 General Description

This data sheet covers the AMIS-710616-AS (PI616MC-AS) specification.

CIS stands for contact image sensor. It is a one-dimension array of photosensitive elements, designed to image documents with a one-to-one magnification ratio. The sensors are sequentially cascaded to form a one dimensional variable-length line array in multiple integral numbers, hence providing the users with desired lengths.

The AMIS-710616-AS is one of these special length line-image arrays. It is configured with a total of eight sub-sections, each section containing a sequential line of five array sensors, with its individual video output line. These eight video outputs are also referred to as tapped outputs. They are all read out in parallel (see Figure 1). The eight sub-sections are sequentially cascaded to form the one-dimensional array. It is fabricated on two printed circuit boards (PCB) referred to as sensor boards. Each sensor board contains four sub-sections. The two sensor boards are cascaded in series to form a complete line image sensor of eight sub-sections with a total read length of ≅ 325mm. Accordingly, each sensor board contains 20 each of AMIS-720639 (PI3039) image sensors, also a product of AMIS. Hence, for both boards there are a total of eight parallel tapped outputs and 40 each of the AMIS-720639 image array sensors. Each chip has 192 photo sensing cells, hence on one board there are 3840 cell sites and a total of 7680 cell sites for both boards. Each cell site is a photo-detector, which possesses its own independent processing circuit. An associated on-chip digital shift register scans and reads the video signal of each photo detector onto a common output video line. In sections of five sensors, these common output video lines are individually brought out to the I/O connectors of the sensor boards. There are two connectors, one on each board, each containing four video outputs. These connectors are connected via a cable to their respective amplifier boards (see Figure 2). The schematic of the AMIS-710616-AS and its PCB mechanical outline drawing are attached to this data sheet.

2.0 Overview

The AMIS-710616-AS has ≈ 324.2mm read width. Its recommended line rate is 192µs/line at a 5.0MHz clock rate, but its minimum can be as low as 160µs/line at its maximum clocking speed of 6.0MHz. Its sensor photo-site density is 23.25elements/mm. See AMI Semiconductor's AMIS-720639 data sheet, which covers the specifications on the imaging array sensor. Operationally, it requires only the power supplies, +5V and –5V and two input clocks, one is the clock (CP), to operate the internal shift registers and the second is the start pulse (SP), to initiate the output scan.

3.0 Scan Outline

Table 3-1: Scanning Outline

Item	Specification	Note
Readable width	324.2mm	
Sensor photo-site density	23.25elements/mm	
Number of total active sensor photo-sites	7680 elements	
Number of photo-sites per tap	960	
Total line read time = read time per section	192µs/line 160µs/line	Typical, tested @ 5.0MHz Clock Minimum, tested @ 6.0MHz Clock
Clock frequency	5.0MHz 6.0MHz	Typical Maximum

4.0 Physical Outline

Table 4-1: Physical Outline

Item	Specification	Note
Image sensors	AMIS-720639	See referenced image sensor data sheet
PCB stiffner board	PCB stiffner board size ≅355.6mm x 41.3mm x 6.35mm	
Sensor PCB	Size ≈165.1mm x 21.4mm x 1.62mm	Two PCBs mounted on the stiffner
Data output	Eight analog video outputs	
Sensor board connectors	Two I/O connectors MOLEX 52610-1590	Used to connect to their respective output amplifiers
Amplifier PCB board	Size ≈ 291.3mm x 76.2mm x 1.6mm	
Amplifier board's four connectors	Two inputs: MOLEX 52207-1950 Two outputs: ERNI-594083	Mounted are eight output amplifiers for each of the video lines from the sensor boards

5.0 Recommended Operating Conditions (25°C)

Table 5-1: Recommended Operating Conditions at 25°C

Item	Symbol	Min.	Typ.	Max.	Units
Power supply	VDD	4.5	5.0	5.5	V
	IDD	135	150	165	ma
	VSS		|-5.0|	|-5.5|	V
	ISS		45	60	ma
Video output levels	Vpavg (1)		3.0		V
Video saturation output	VSATA (2)		5.5		V
Video line saturation output	VSATV (2)		1.2		V
Input voltage at digital high (input clocks, SP and CP)	VIH	VDD-1.0	VDD-.5	VDD+0.3	V
Input voltage at digital low (input clocks SP and CP)	VIL	0		0.8	V
Clock frequency	Freq (3)		5.0	6.0	MHz
Clock pulse high duty cycle	Duty (4)	25		75	%
Clock high duration	TPW(3)(5)	83.3	100		Ns, at 50 percent duty
Integration time	Tint	192µs/line 160µs/line			Typical, tested @ 5.0MHz clock Minimum, tested @ 6.0MHz clock
Operating temperature	Top (6)		25	50	°C

Notes:

(1) Vpavg is a symbol representing the average value of every pixel in the complete line scan. Vp(n) is the pixel amplitude of the nth pixel in a line scan. This measurement is taken with the image array under a uniform light exposure. The typical output is specified with a uniform input light exposure of 0.5µJ/cm^2 from a blue Led light source.

(2) Two saturated video output levels are specified. One is at the video signal's output amplifier, VSATA, and the other is at the input of the amplifier. In almost all applications, because the integration time is usually too short, there is not enough exposure time to saturate the array sensors. Accordingly, each output amplifier is fixed with a gain of ≅ 4.5.

(3) Freq is generally fixed for any application for the following reasons: One is the exposure time. With a given light power, the exposure time of the sensor can be related to the clock frequency. The second is the shape of the video output pulse. Because the output video is in pulse charge packets, the signals are processed on the output video line of the sensors. Hence, the signal shape depends greatly upon the amplifier configurations. Please refer to the referenced AMIS-720639 data sheet. It has some brief outline application notes. Under Note 6 on Page 6, there is a discussion about video pulse shapes. On Page 8, 9 and 10 there are discussions on the three types of signal output stages.

(4) Duty is the ratio of the clock's pulse width over its pulse period. Because the video pixel output resets during the clock pulse's high period and because the reset requires a finite resetting time, it is recommended to operate the clock duty cycle within the following limits. See the referenced data sheet in Note 3, above. Noting that the larger the duty, the less the signal amplitude, while too short of a clock pulse will not provide enough video reset time and leaves residual charges, the recommended duty is 25 percent for frequencies less than 5MHz and 50 percent for frequencies greater than 5MHz.

(5) Tint is determined by the time interval between two start pulses, (SP). Hence, if the SP is generated from a clock count down circuit, it will be directly proportional to the clock frequency and it will be synchronous with the clock frequency. The longest integration time is determined by the degree of leakage current degradation that can be tolerated by the system. A 10ms maximum is a typical rule-of-thumb. An experienced CIS user can use his discretion and determine the desired tolerance level for the given system.

(6) Top is a conservative engineering estimate. It is based on measurements of similar CIS modules and simple bench top tests, using heat guns and freeze sprays. These will be re-measured during the pilot production under the standard QA practices that are under the control of ISO 9000.

6.0 Electro-Optical Characteristics (25°C)

Table 6-1: Electro-Optical Characteristics at 25°C

Parameter	Symbol	Parameter	Units	Note
Number of active photo detectors		7680	Elements	
Pixel-to-pixel spacing		43.25	µm	
Line scanning rate	Tint (1)	192	µs/line	@ 5.0MHz clock frequency (see Note 1)
Clock frequency	Freq (2)	6.0	MHz	Maximum clock frequency (see Note 2)
Red responsivity	ExpR(3)	70	V/µJ/cm2	See Note 3 for definition
Green responsivity	ExpG(3)	55	V/µJ/cm2	See Note 3 for definition
Blue responsivity	ExpB(3)	35	V/µJ/cm2	See Note 3 for definition
Bright output voltage	Vpavg (4)	3.0	V	Green light
Bright output non-uniformity	Up (5)	<7	%	Depends on optical system (see Note 5)
Adjacent pixel non-uniformity	Uadj (6)	<10	%	
Bright output Non-uniformity total	Uptotal (7)	<10	%	Depends on the optical system (see Note 5)
Dark non-uniformity	Ud (8)	<25	mV	
Dark video offset	Vd (9)	-2.0	Volts	
Random noise	RNL (10)	<11.8 <3.0	p-p mV rms mV	
Modulation transfer function	MTF (11)	>70	%	Sensor only (see Note 11)

Notes:
Since this is a prototype module, the following Notes 4, 5, 6, 7, and 8, are on data based on engineering scope measurements. The data will be re-measured during pilot production using all the standard QA practices under the control of ISO 9000 regulations. Furthermore, they will be taken on fully computerized test systems. If required, these prototype data may be revised.

(1) Tint is the line-scan rate or integration time. It is determined by the time interval between two SPs. If the SP is generated from a clock count down circuit, it will be directly proportional to clock frequency and it will be synchronous with the clock frequency. The longest integration time is determined by the degree of leakage current degradation that can be tolerated by the system. A 10ms maximum is a typical rule-of-thumb. An experienced CIS user can use his discretion to determine the desired tolerance level for the given system.

(2) Freq is the clock frequency, which is also equal to the signal data rate. It is generally fixed for many applications for following reasons: One is the exposure time. With a given light power, the exposure time of the sensor depends on the integration time and in most applications it uses clock count down circuits to generate the SP, shift register start pulse. The second is the shape of the video output pulse. Because the output is in pulse packets of video charges, the signals are processed on the output video line of the sensors. The signal shape depends greatly upon the amplifier configurations. Please refer to the referenced AMIS-720639 data sheet. It has some brief outline application notes. Under Note 6 on Page 6, there is a discussion on video pulse shapes. On Page 8, 9 and 10 there are discussions on the three types of signal output stages.

(3) The responsivity is the ratio of video signal in volts, divided by the unit exposure (V/micro-Joules/cm ^{2}). This exposure was measured with the output level adjusted to 1.27V. The spread of the measured exposure R-RSP, G-RSP and B-RSP can be used to compute the user's desired signal voltage level.

(4) Vpmax = maximum pixel value of Vp(n); Vpmin = minimum pixel value of Vp(n); Vpavg = Σ Vp(n)/7680; where Vp(n) is the nth pixel in a line scan with the module scanning a uniform white target. Vp values are measured with a uniform exposure.

(5) Bright output Non-uniformity: Up(+) = [(Vpmax - Vpavg) / Vpavg] x 100% or Up(-)= [(Vpavg - Vpmin) / Vpavg] x 100%, whichever polarity with the highest value is selected. Two further notes: One is that the AMIS-710616-AS has no requirement for an optical system, or a light system. The second is that the non-uniformity is dominated by the LED light bar's non-uniformity so only the sensor non-uniformity is specified. The normal standard CIS modules are enclosed in a self-contained module with a complete optical and LED lighting system. So the light system, usually the LED bar, is included in making the measurement of the optical characteristics. This fixes the optical geometry for the module and the light source. The module's optical characteristics are simply measured with the module placed on a uniform reflecting target with a known reflection density. However, the AMIS-710616-AS is not enclosed with its optical and light source system. Therefore, Up is measured with uniform light source, which directly illuminates the image sensors' photosite.

(6) Adjacent Pixel Non-uniformity: Upadj = MAX[| (Vp(n) - Vp(n+l) | / Vp(n)] x 100%. Upadj is non-uniformity in percentage of Vpavg. It is the maximum difference amplitude between two neighboring pixels.

(7) Bright output total non-uniformity: Uptotal = [Vpmax -Vpmin]/Vpavg

(8) Dark non-uniformity: Ud = Vdmax – Vdmin: It is measured over the full length of the array with the light source off and the sensors placed in the dark. Vdmax is the maximum pixel value of the video pixel with the exposure off. Vdmin is the minimum pixel value of the video pixel with the exposure off. The references for these levels are the dark level, VDL.

(9) Dark output voltage, VDL is the level between the out video pixel dark level and the ground.

(10) Random noise, RNL, is measured using two methods; one is to take the measurement tangentially on the scope. This measures an approximate peak-to-peak, p-p, random thermal noise. The other method is in terms of rms. It is estimated by using Gaussian statistical methods. One pixel is selected out of a line scan and its peak values are recorded for multiple line scans. These random peak values are used to estimate the rms values.

(11) Modulation transfer function depends on the optical system. Since this system relies on the users optical system, it was not measured. Referring back to Note 5, measurements on Up, all notes that reference the optical measurements apply to MTF measurements as well. Using a conservative engineering estimate, the sensor's MTF is in excess of 70 percent at the optical Nyquest frequency.

7.0 Electrical Timing Characteristics

7.1 Clock Amplitude and Duty Characteristics

Table 7-1: Clock Amplitude and Duty Characteristics (Ta =25°C)

Item	Symbol	Condition	Specification			Units
			Min.	Typ.	Max.	
Clock input voltage	VIH (1)	For values see the notes		See Note (1) for values		
	VIL (1)					
Clock input current	IIH (1)			See Note (1) for values		
	IIL (1)					
Clock frequency	Freq (2)		0.100	5.0	6.0	MHz
Line read time	Tint (3)		160	192	1000	µs
Clock pulse duty cycle	Ratio = tw/ to (4)		25	50	75	%

Notes:

(1) These CP and SP values are compatible with CMOS 74HCXX series logic devices.
(2) Freq is not only the clock frequency, but is also equal to the pixel sample rate. See not 2 under Table 6.1.
(3) Tint is the line scan read time, which depends on the interval between the SP entries. See Note 1 under Table 6.1. The longest integration time is determined by the degree of leakage current degradation that can be tolerated by the system. A 10ms maximum is a typical rule-of-thumb. An experienced CIS user can use his discretion to determine the desired tolerance level for the given system.
(4) The definition for the symbols used in the ratio is defined in Section 7.2.

7.2 Clock Timing Characteristics

This table defines the symbols used in the timing diagram (Figure 3). It is for a single video section, however it applies to all eight video sections. Accordingly, the system-timing diagram is a composition of this timing diagram repeated eight times, with all waveforms in parallel, so electrically the system produces pixels from all eight video sections simultaneously.

Table 7-2: Clock Timing Characteristics

Item	Symbol	Min.	Typ.	Max.	Units
Clock cycle time(2)	to	0.1666	0.200	10	µs
Clock pulse width(2)	tw		0.100		ns
Clock duty cycle(2)	duty	25	50	75	%
Prohibit crossing time of SP	tprh	30			ns
Data setup time	tds	30			ns
Data hold time	tdh	25			ns
Signal delay time	tdl			75	ns
Signal sample time	tsmp(3)	125			ns
Signal fall time	tsigf			75	ns
Recommended SP generation	Tonoff(4)				

Notes:

(1) This applies to the whole chart. All of the symbol definitions in Table 7-2 are used in Figure 3. For the complete system, there are only two clocks, CP and SP and their logic levels are compatible with CMOS 74HCXX series logic devices.
(2) See the notes on clock periods (the inverse of freq) and their duty cycles under Table 5-1 Notes 3 and 4.
(3) See AMIS-720639 data sheet Page 6, Table 6A, Note 6.
(4) This is the recommended method for SP generation because the shift register loads only on the falling edge.

8.0 Maximum Ratings

Table 8-1: Maximum Ratings (Not to be Used for Continuous Operation)

Item	Symbol	Specification	Note
DC supply voltage	VDD	7V	
Input voltage	VIN	0 to VDD +0.3	SP & CP
Ambient temperature (1)	TA (PCB surface)	0 to 70°C (see note below) -10° to +75°C (see note below)	Operational storage
Ambient humidity (1)	HA	0 to 80% (see note below)	Non-condensing
Maximum operating case temperature (1)	PCB temperature	70°C (see note below)	

Note:

(1) All the referenced parameters are conservative engineering estimates based on a few of the prototypes' PCB. They are based on measurements of similar CIS modules and/or simple bench top tests using heat guns and freeze sprays. However, these parameters will be re-measured during the pilot production using standard QA practices, which are under the control of ISO 9000 regulations.

9.0 I/O Connector Pin Configuration

There are two I/0 connectors on the stiffener plate with the two sensor boards. They are MOLEX 52610-1590. They serve to connect the sensor boards to the amplifier boards (see the outline drawing of the system, Figure 2). Two 15 conductor strip lines serve as the interfacing harness. It is depicted with harnesses coming from under the stiffener plate, crossing to the top of the amplifier board and connecting to the two input connectors MOLEX 52207-1950. The final connectors are the two ERNI-594083s. They are the system I/Os.

Only one of the two connectors on the stiffener board is specified because both connectors have identical pin-out definitions. There are eight video taps, four from each sensor board and they are sequential re-numbered. The first sensor board video outputs are, 1, 2, 3 and 4. The second sensor board's videos are 5, 6, 7 and 8.

9.1 Two MOLEX 52610-I590 and its Mate to Amplifier Boards MOLEX 52207-1590

Table 9-1: Sensor Board Connectors and Input Connectors for Amplifier Board Pin-outs

Pin Numbers	Pin Names	Symbols	I/0	Names and Functions
1	Clock pulse	CP	I	
2	Start pulse	SP	I	
3	Ground	GRD	I	Ground; 0V
4	Power supply	VDD	I	Positive power supply
5	Ground	GRD	I	Ground; 0V
6	Ground	GRD	I	Ground; 0V
7	Ground	GRD	I	Ground; 0V
8	Video output	VSEC1	O	Tapped 1 video output, Section 1 on Board 1; it is Section 5 on Board 2
9	Analog Ground	AGRD	I	Analog video return line, ground; 0V
10	Video output	VSEC2	O	Tapped 2 video output, Section 2 on Board 1; it is Section 6 on Board 2
11	Analog Ground	AGRD	I	Analog video return line, ground; 0V
12	Video output	VSEC3	O	Tapped 3 video output, Section 3 on Board 1; it is Section 7 on Board 2
13	Analog Ground	AGRD	I	Analog video return line, ground; 0V
14	Video output	VSEC4	O	Tapped 4 video output, Section 4 on Board 1; it is Section 8 on Board 2
5	Analog Ground	AGRD	I	Analog video return line, ground; 0V

9.2 Amplifier Board Output Connectors, ERNI594083

There are four connectors on the amplifier board. Two are inputs, which are described above, and two are outputs, which are described below. There is only one table shown for both connectors. They are both identical in their connections except that one is for the outputs of Sensor Board 1 and the other is for the outputs of Sensor Board 2. Accordingly, each of the video outputs after amplification for both sensor boards are labeled, VOUT1, VOUT2, VOUT3 and VOUT4. Videos from Sensor Board 1, VSEC1's corresponding output is VOUT1, VSEC2's corresponding output is VOUT2, VSEC3's corresponding output is VOUT3 and VSEC4's corresponding output is VOUT4. Then the videos from Sensor Board 2 will have their corresponding outputs on the second connector VOUT1, VOUT2, VOUT3 and VOUT4, except their outputs VOUT5, VOUT6, VOUT7 and VOUT8 because those video signals originate from Section 5, Section 6, Section 7 and Section 8 of Sensor Board 2.

Table 9-2: Amplifier Board Output Connectors, ERNI-594083

Pin Numbers	Description Row A	Description Row B	Description Row C
1	VDD	VDD	AGND
2	VDD	VDD	VOUT1
3	No connect	No connect	AGND
4	Ground	Ground	AGND
5	SP	GND	AGND
6	No connect	GND	VOUT2
7	No connect	GND	AGND
8	No connect	GND	AGND
9	CLK	GND	AGND
10	GND	GND	VOUT3
11	No connect	GND	AGND
12	No connect	GND	AGND
13	No connect	GND	AGND
14	GND	GND	VOUT4
15	No connect	No connect	AGND
16	VSS	VSS	AGND

Note: The functional description for the symbols used in Table 9-2 are the same as described for the input connector. The two new symbols VSS and CLK are as follows: VSS is negative supply input. CLK is CP.

The locations of Pin 1 on all the connectors are facing the same end (see Figure 2).

10.0 Block Diagrams - Figures 1, 2 and 3

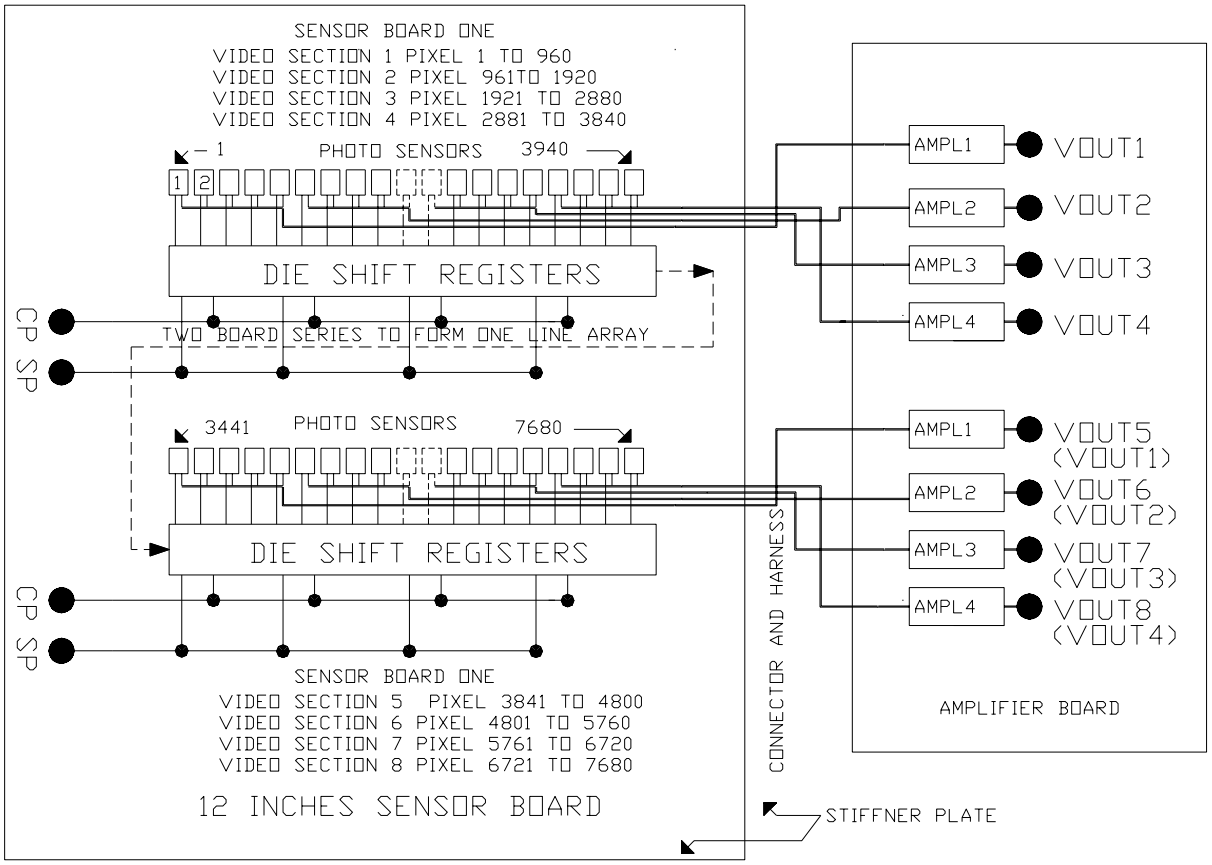

Figure 1: Simplified Circuit Block Diagram

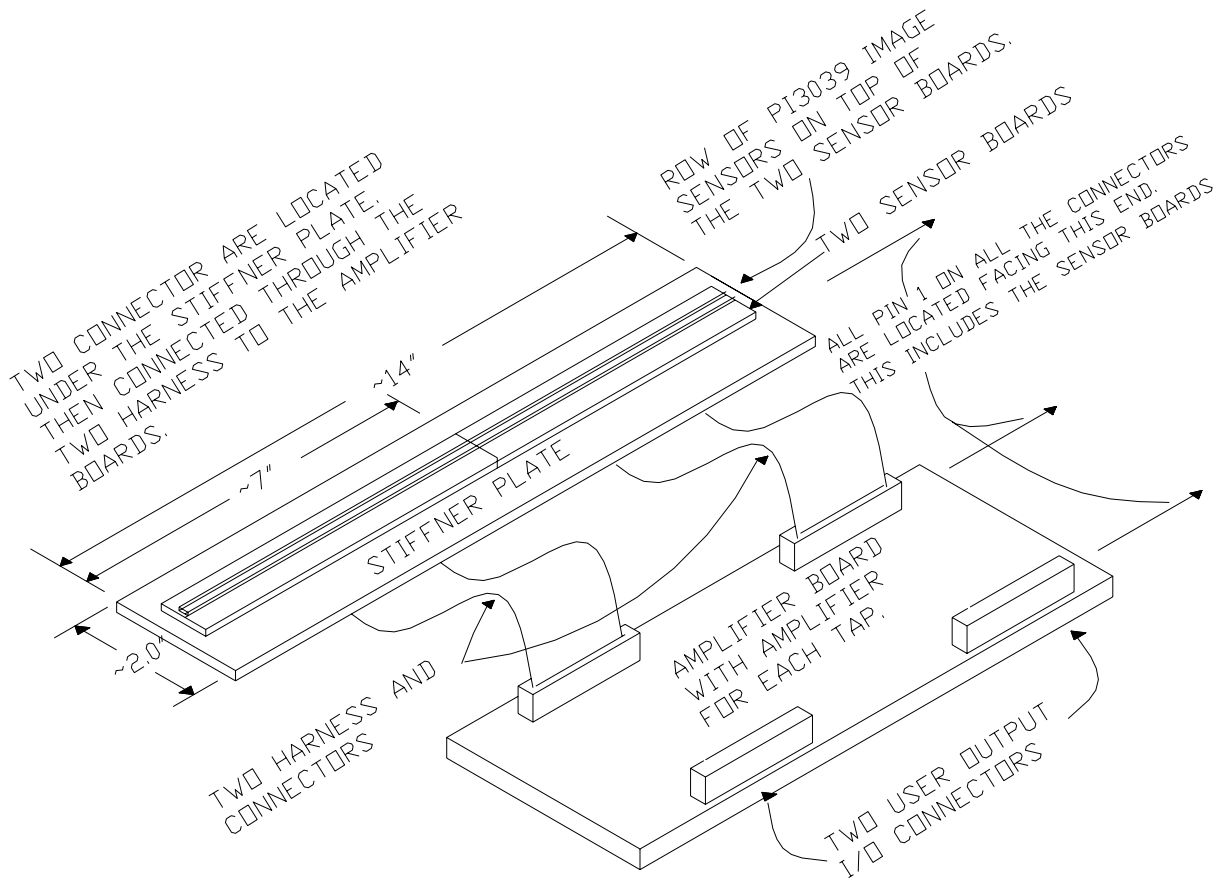

Figure 2: System Configuration Block Diagram

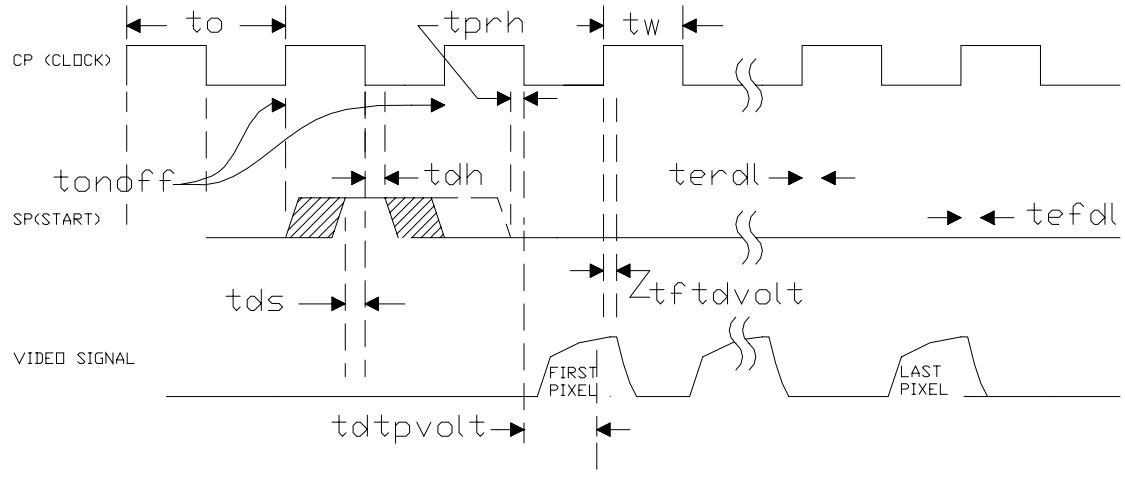

Figure 3: Timing Diagram

11.0 Schematic Diagram

Two reference schematic diagrams are attached to this document (Figure 4 and Figure 5). Only one schematic, CKT 1, Schematic (Figure 1), is required to represent both the Sensor Board 1 and 2 because the circuits are identical. The second one is for the amplifier board and it contains all eight of the amplifiers on one schematic. The circuit description of its structure and operation has been briefly discussed in Section 1 of this document. Its operation follows from the discussion of the simplified block diagram. There are only two input control clocks for the circuits, CP and SP. SP starts the shift register scanning while CP clocks the register and produces the video pixels at its same rate. The clocks are entered through the I/O connectors on both sensor boards. They are both externally buffered with the 74HC00 hexes and applied to the inputs of the image sensors. On each of the two-image array sensor boards there are four sequential video sections. Each video section contains a row of five sequential image array sensors, AMIS-720639. These are all clocks in parallel with CP. The four sections on both boards are clocked with SP in parallel, to initiate all eight video sections and simultaneously begin the eight sequential readouts. All eight lines, four in each sensor board, have reset switches, BU4S66, which parallel resets the video pixel charges after they are readout. These pixels, read out in parallel, are applied to their respective output amplifiers on the amplifier board.

The second schematic, CKT 2, Amplifier Board Schematic (Figure 5), is the amplifier board. There are eight amplifiers for processing the output videos from both sensor boards. The amplifier board receives the inputs from the sensor board output connector, J1, through two harnesses. They are connected into the input I/O connectors, J1 and J2, of the amplifier board. Since there are two sensor boards using the same schematic representation, the connector on Sensor Board 1, J1, becomes J2 for the second board. They are physically differentiated and marked as J1 and J2 on the stiffener board. Since all eight sections process their video signals through identical amplifiers, only one amplifier circuit is discussed. The AD8051 is an operational amplifier, which is configured into a non-inverting buffer amplifier with a gain of $\cong 4.5$. It is used to isolate the video line from its external circuits. The isolated video line then serves as a storage capacitance for the pixels outputs. The pixel charges are read out onto the video line capacitance and integrated. This integrated pixel charge, converted to a voltage pulse, is amplified and produced at the output I/O. The reset switch on the video line, which is located on the sensor board schematic, resets the pixel signal charge prior to the readout of following pixel.

11.1 Schematic Drawings; CKT 1 and CKT 2

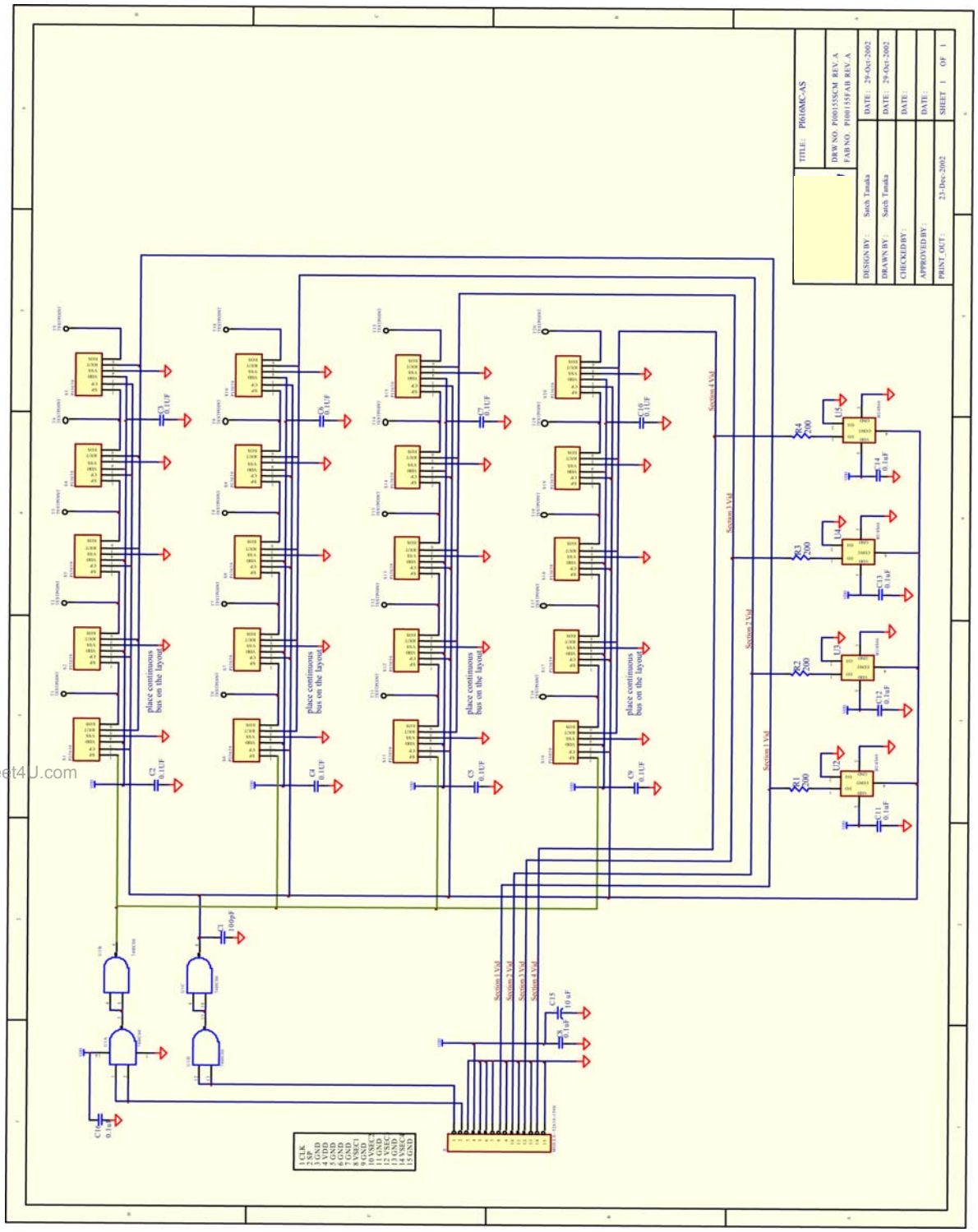

Figure 4: CKT 1 - Sensor Board Schematic

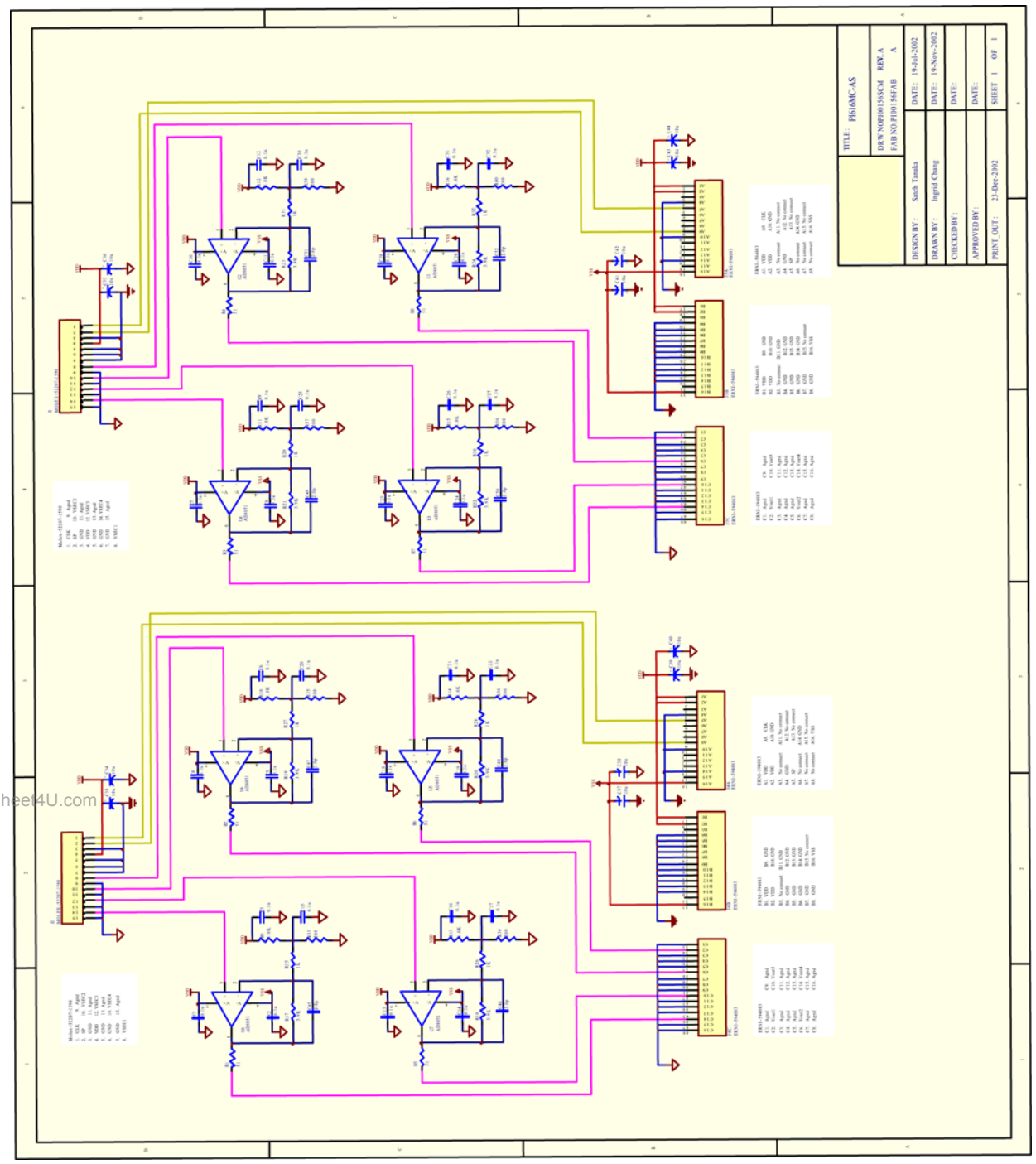

Figure 5: CKT 2 - Amplifier Board Schematic

12.0 Drawing on Mechanical Structure

Attached are six mechanical drawings. The first drawing (Figure 6) shows an outline drawing of the complete CIS system, consisting of the stiffener plate, the interconnecting harness and the amplifier board. There are two connector pin configuration tables, one is for the two sensor boards and the input for the amplifier board and the other is for the two output connectors on the amplifier boards. These two tables show the pin numbering and names for the six connectors that are seen in the drawing. For detailed descriptions of the interconnections and their functions, see section 9.0.

The second drawing (Figure 7) shows the view of the stiffener board. The stiffener board is a ¼" aluminum backing plate on which the two image sensor boards are mounted. The schematic drawing provides the dimensions of the plate, its access holes for the two-sensor board's connectors, along with all of the required dimensions.

The third drawing (Figure 8) shows a view of the two sensor boards mounted on the stiffener board. It shows the direction of the scan, its first pixel location and its video read line location. It provides the dimensions on the connector height, the thickness of PCB board and its component height.

The fourth drawing (Figure 9), is a backside view of the stiffener plate. It shows the location of the connectors and its pin order and direction.

The fifth drawing (Figure 10) shows a view of the PCB outline. The three views of the board provide the outline dimensions, its length, its width and its thickness. It also depicts the mounting holes and their dimensions and locations.

The six drawing (Figure 11), shows a view of the PCB with its connectors.

12.1 Mechanical Drawings; Drawing 1, 2, 3, 4, 5 and 6

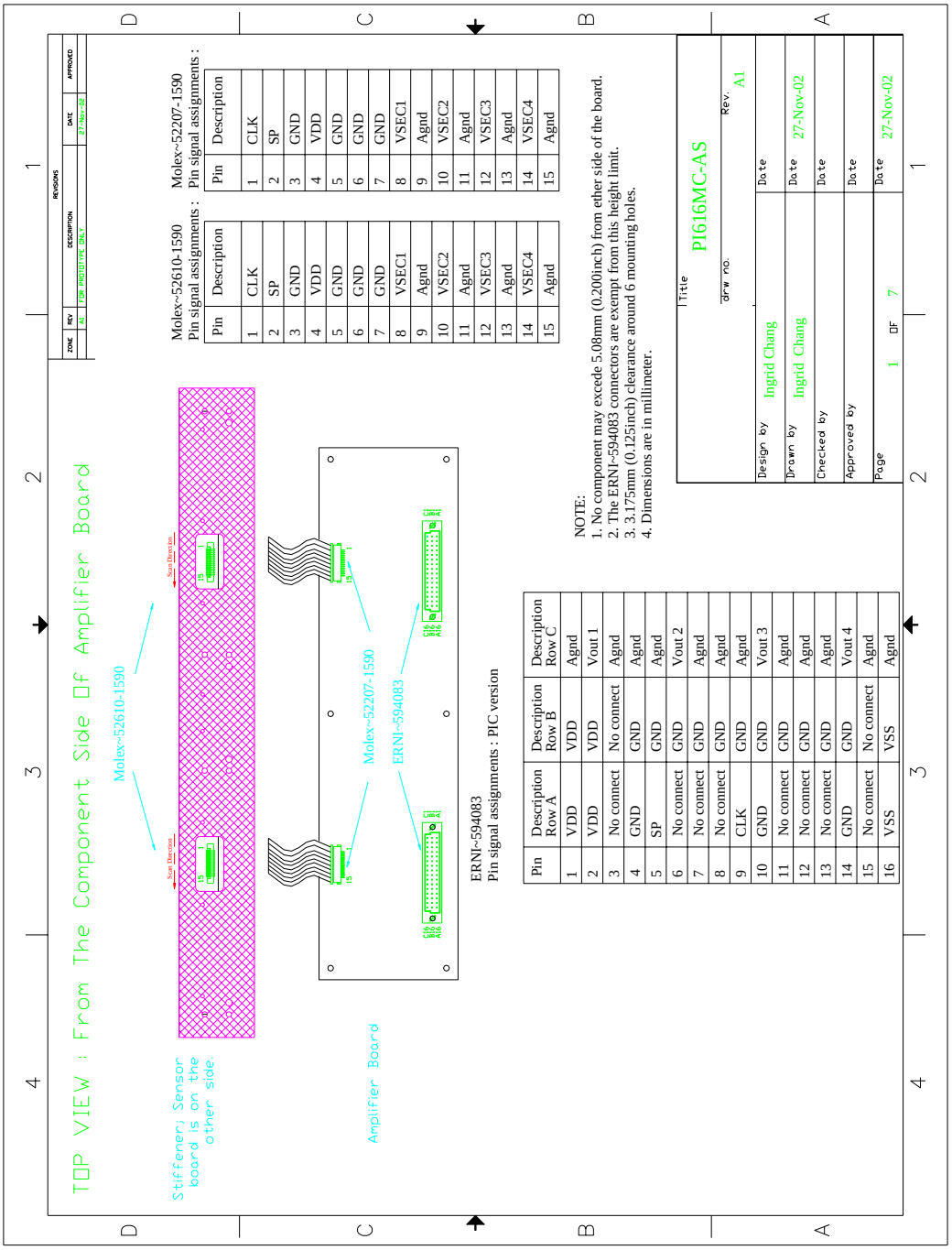

Figure 6: Drawing 1 -Top Assemble Outline

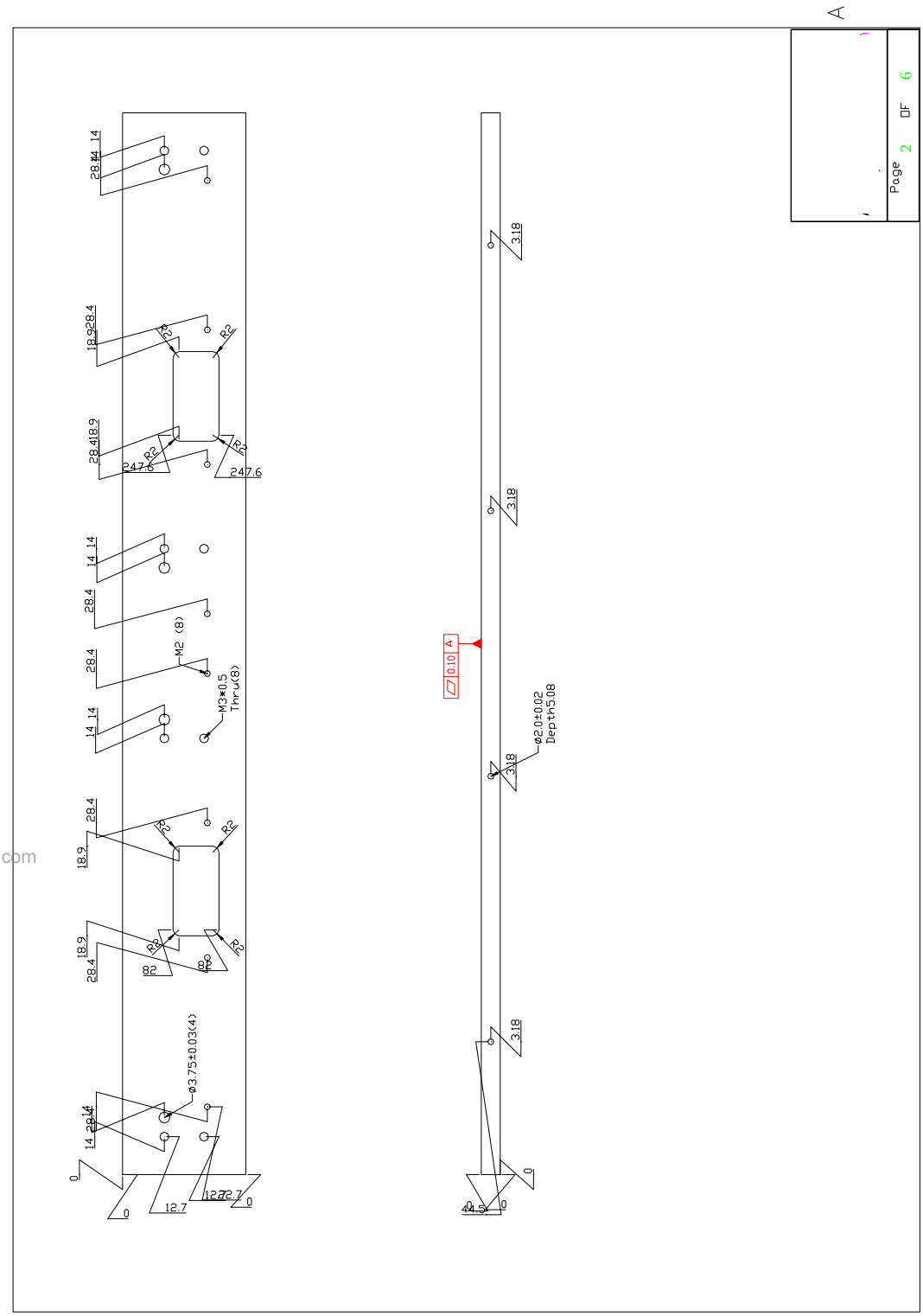

Figure 7: Drawing 2 - Stiffner Plate

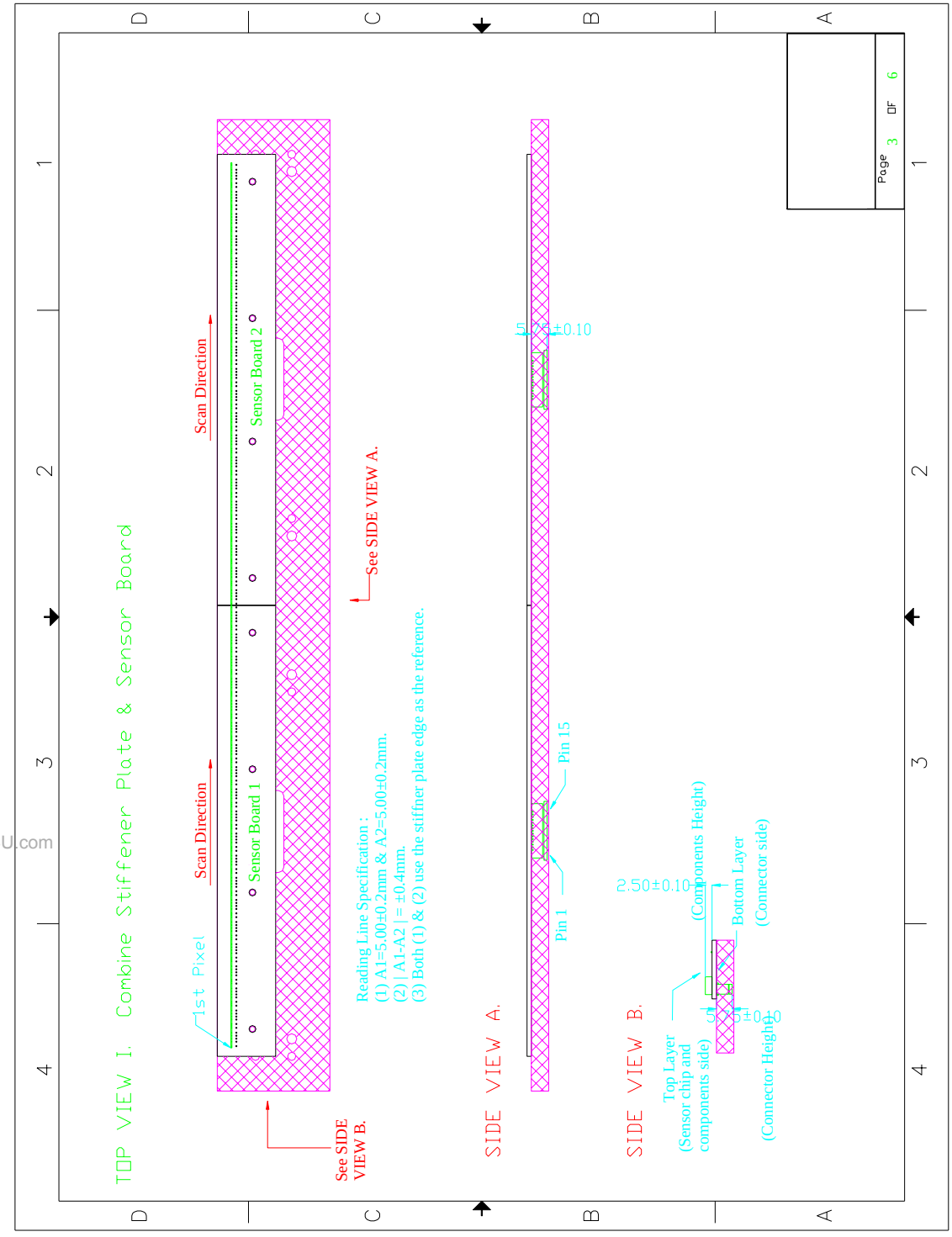

Figure 8: Drawing 3 - Two Sensor Board

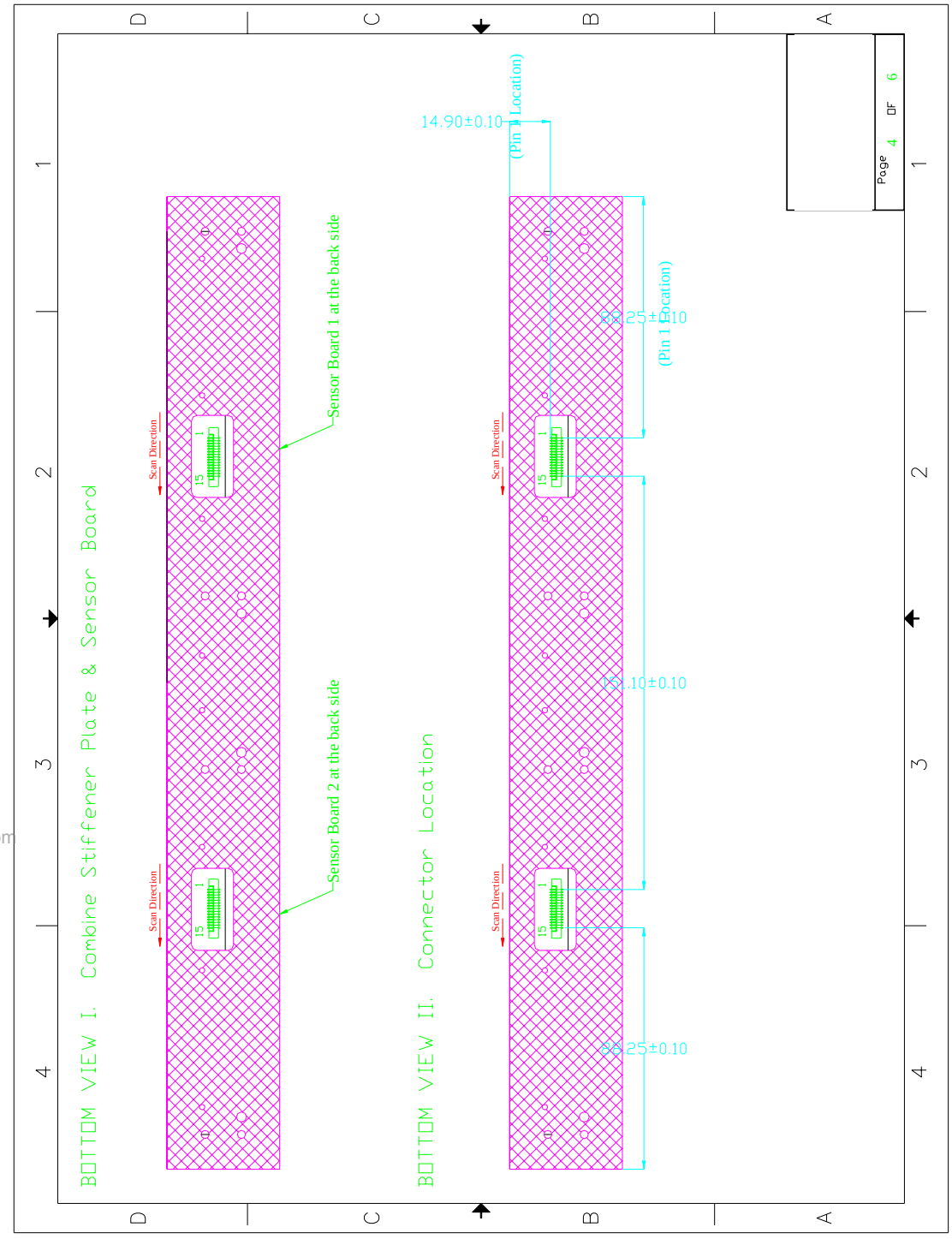

Figure 9: Drawing 4 - Connectors on Stiffner

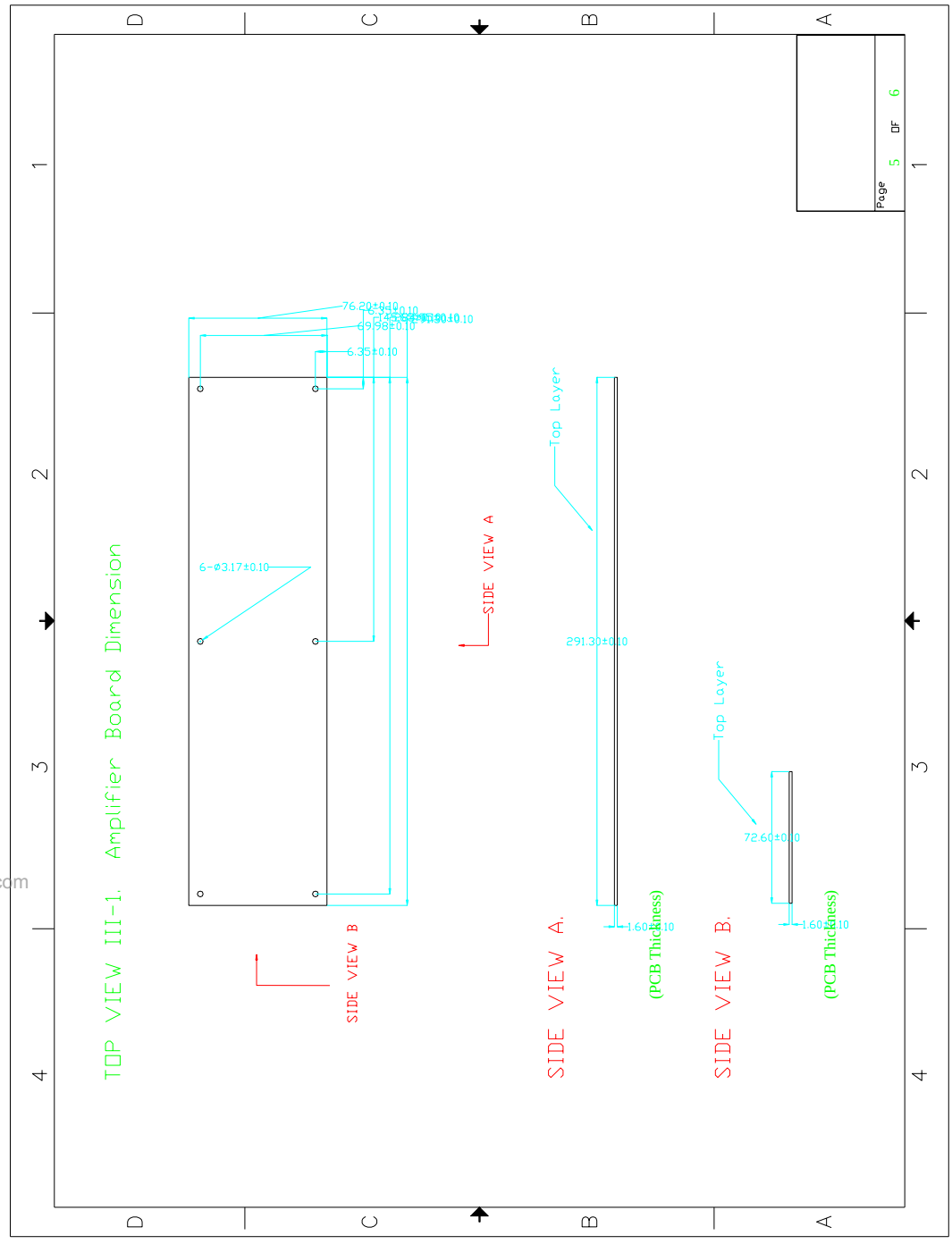

Figure 10: Drawing 5 - Amplifier Board

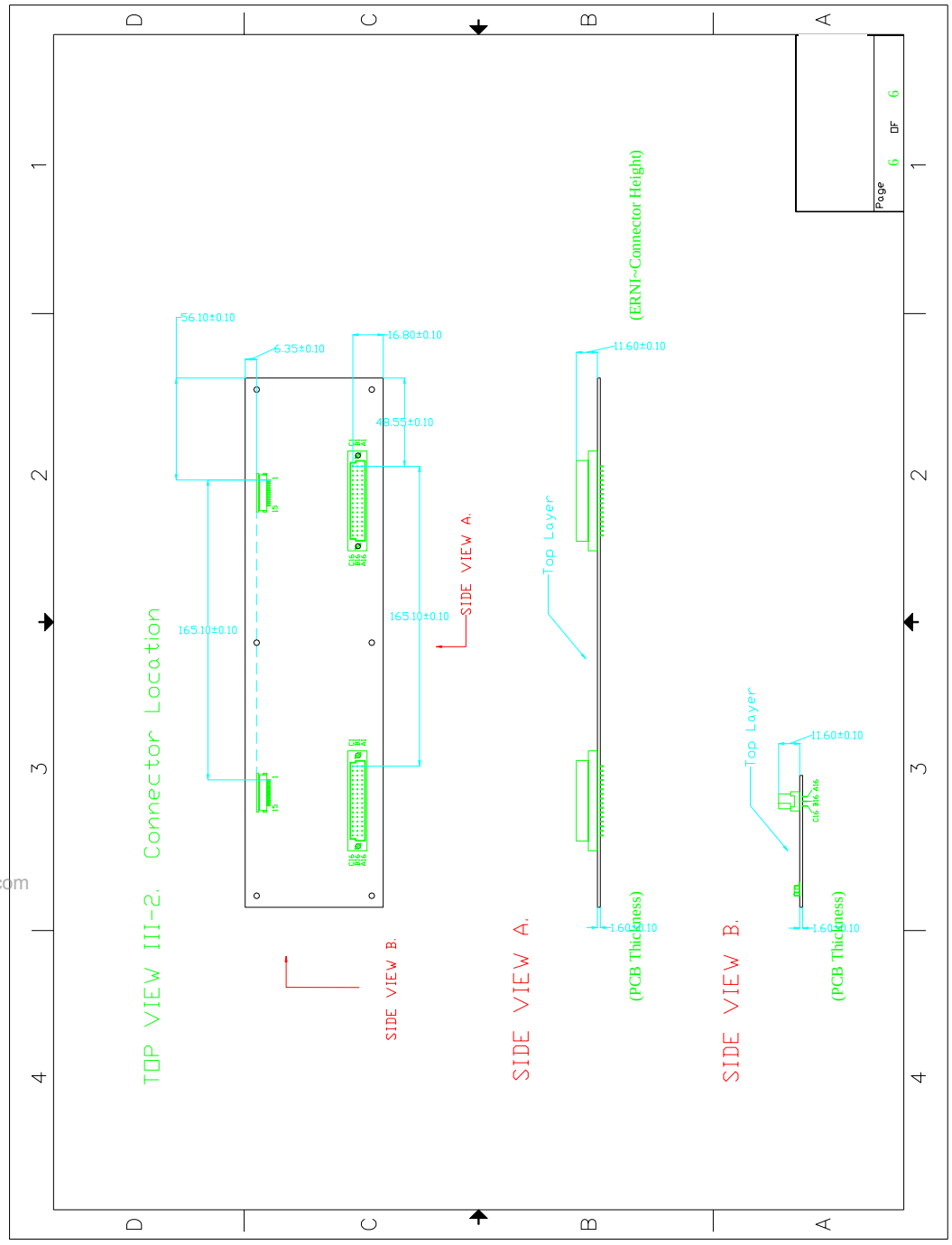

Figure 11: Drawing 6 - Amplifier Board with Connectors

13.0 Company or Product Inquiries

For more information about AMI Semiconductor, our technology and our product, visit our Web site at: http://www.amis.com

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