# AMIS-52150

# Low-power Transceiver with Clock and Data Recovery

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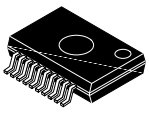

SSOP−20
CASE TBD

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

### Introduction

The AMIS−52150 is a cost-effective, ultra-low power single-chip wireless transceiver. It combines the proven Amplitude Shift Key/On-Off Key (ASK/OOK) modulation technology of the AMIS−52050 with data clock recovery.

Based on key features, such as dual independent receive channels, Quick Start crystal oscillator, Sniff Mode signal acquisition, and data clock recovery, the AMIS−52150 is ideally suited for a wide range of applications, including point-to-point wireless data links, cost-optimized wireless monitor solutions, and very low power remote wireless sensors, among others.

### Key Features

- Data Clock Recovery
- Auto Slicing of Data
- Very Low-power Single-chip Transceiver
- Minimal External Components
- Low-power RC Oscillator
- Quick Start Crystal Oscillator
- Ultra-low Power RF Sniff Mode, with Wake-up on RSSI
- Internal Trim Functions Reduce External Component Requirements
- $I^2C$ Control Interface
- Serial TX/RX Data Port
- Clock Generation for an External Microprocessor
- Wake-up on RSSI
- Antenna Diversity Dual Receiver
- Internal VCO/PLL Tuning Varactor
- Wake-up Interrupt to External Controller
- These Devices are Pb-Free and are RoHS Compliant

### Technical Features

- Operating Frequency Range:
  - Quick Start, from 350 MHz to 448 MHz
  - Non-quick Start, from 300 MHz to 768 MHz
- TX Output Power: +12 dBm
- RX Sensitivity:
  - Sniff Mode: −93 dBm Minimum
  - Receive: −117 dBm Minimum @ 1 kbps, with CDR
- Data Rate:
  - 1−8 kbps with Manchester Coding
  - 1−16 kbps with NRZ Data
- Power Requirements:
  - Receive: 7.5 mA (Continuous)
  - Transmit: 25 mA @ Full Power (50% Duty-cycle)
  - Sniff Mode: 75 μA (One Percent Duty-cycle)
  - Standby: 500 nA (RC Oscillator Running)
- Operating Voltage: 2.3 V to 3.6 V
- Modulation: ASK/OOK
- Xtal Start Time: 15 μs (Quick Start)
- Sniff Mode Polling: 0.5 ms to 16 s (0.5 ms or 64 ms Steps)
- PLL Lock Time: < 50 μs
- Selectable Data Filter: Up to 20 kHz
- Internal Trim Functions:
  - TX Power (−3 to +12 dBm)
  - Antenna Impedance Matching (Two Independent Channels)
  - Xtal, for Frequency and Quick Start
  - RC Oscillator Frequency
  - Sniff Mode, for Data Threshold
  - Data slice
- Clock and Data Recovery (Reduced Data Jitter)
- $I^2C$ Interface: Control Bus
- Serial Interface: Data Input/Output
- Low Frequency IF
- Internal IF Filtering
- Package: 20-lead, 209 mm SSOP

## FUNCTIONAL BLOCK DIAGRAM

The AMIS−52150 is a dual-channel receiver and a transmitter in a single, small outline package (Figure 1). The receiver provides for two independent receive channels with the signals combined in the data detection circuit. Summing the signals allows the two channels to be used for antenna diversity optimization, without the need for complex protocols to select the strongest channel. The AMIS−52150 can be programmed to be a single channel or a dual-channel receiver, respectively. There exist internal trim functions for the RF receiver frequency, for tuning each input port, for setting the internal filters to match the data rate, and for setting the threshold level for acquiring an incoming signal, respectively. The receiver converts the received RF signal to a low frequency IF. An RSSI circuit determines the strength of the received signal. A level detector samples the RSSI signal level and compares that level to the slice threshold to recover the data. The slice threshold can be either set to a fixed level, or alternately, the transceiver can be configured to automatically set the threshold level based on the incoming data.

The transmitter is a high efficiency power amplifier (PA) that is turned On or Off by the serial data. The output power level is adjustable. The frequency of the RF output can be tuned with an internal crystal trim function, in order to conform to component and manufacturing tolerances. In addition, the design of the transceiver is based on a number of unique features.

The AMIS−52150 can be placed in a very low power state, with the crystal oscillator being Off while the low power RC oscillator maintains the chip operation. In this low power state, the AMIS−52150 remains in the sleep mode until either the wake-up timer or an external microcontroller wake up the device, respectively. The receiver can be also configured for operation in Sniff Mode, where by the device is programmed to wake up at regular intervals to sniff for received RF signals, returning to the sleep mode if a signal is not detected. The AMIS−52150 contains a Quick Start circuit as well, which results in full operation of the crystal oscillator in an extremely short time, in turn leading to much lower power consumption as compared to other transceiver products available in the market. In the AMIS−52150, a programmable PLL is used to synchronize the data clock to the received data. This feature enables reducing much of the jitter in the data signal.

These functions will be described in more detail later in the document.

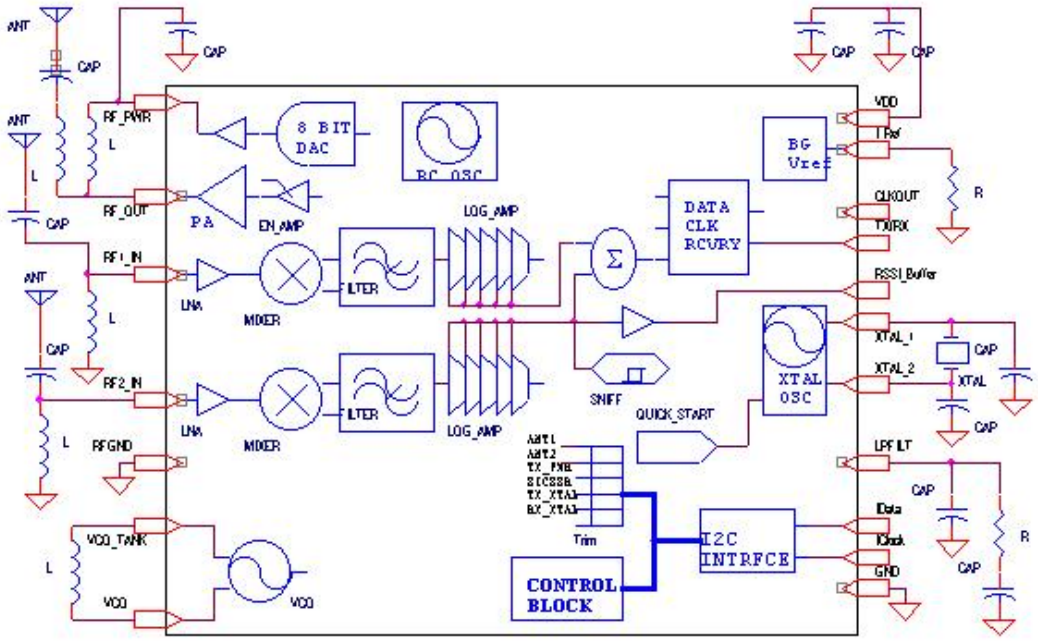


**Figure 1. AMIS−52150 Block Diagram**

## OPERATING AND MAXIMUM SPECIFICATIONS

**Table 1. OPERATING CONDITIONS**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply | 2.3 | 3 | 3.6 | V |
| $V_{SS}$ | Ground | – | 0.0 | 0.1 | V |
| Temp | Temperature Range | 0 | +25 | +50 | °C |

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Positive Supply | – | +4 | V |
| $RF_{in}$ | Max RF Input RX1/RX2 | – | +10 | dBm |
| $V_{SS}$ | Ground | 0.0 | 0.1 | V |
| $V_{in}$ | Logical I/P Voltage | −0.3 | $V_{DD}$ + 0.3 | V |
| $T_{strg}$ | Storage Temperature | −40 | +120 | °C |

| Idd (Supply Current) | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Transmitting | 20 | 25 | mA | 50% Duty Cycle |
| Receiving | 7.5 | 10 | mA | |
| Sniff Mode | 75 | – | μA | 1% Sniff Cycle |
| Off | – | 500 | nA | RC OSC Off |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. ELECTRICAL CHARACTERISTICS**

| Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| **Digital Inputs** | | | | | |
| $V_{ih}$ | 0.7 × $V_{DD}$ | – | – | V | |
| $V_{il}$ | – | – | 0.3 × $V_{DD}$ | V | |
| $I_{ih}$ | – | – | +1.0 | μA | |
| $I_{il}$ | −1.0 | – | – | μA | |
| $I^2C$ Internal Pull-up | – | 15 | 20 | kΩ | |
| **Digital Outputs** | | | | | |
| $V_{oh}$ | 0.8 × $V_{DD}$ | – | – | V | |
| $V_{ol}$ | – | – | 0.4 | V | |
| $I_{oh}$ | – | – | −1.0 | mA | |
| $I_{ol}$ | +1.0 | – | – | mA | |
| $I^2C$ Internal Pull-up | – | 15 | 20 | kΩ | |
| **Analog TX** | | | | | |
| Frequency Range | 402 | 403.5 | 405 | MHz | Targeted |
| | 300 | – | 768 | | Non-quick Start |
| | 350 | – | 448 | | Quick Start |
| Modulation | 1 | – | 8 | kbps | Manchester-coded Data |
| | 1 | – | 16 | kbps | NRZ Data |
| Max. Output Power | 11 | 12 | 13 | dBm | |
| On/Off Ratio | – | 70 | – | dB | Transmit |
| VCO Gain | – | 75 | – | MHz/V | Kvco |

**Table 3. ELECTRICAL CHARACTERISTICS** (continued)

| Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| **Analog TX** | | | | | |
| PLL Phase Noise | – | −95 | – | dBc/Hz | 10 kHz |
| | – | −97 | – | dBc/Hz | 100 kHz |
| Harmonics | – | −35 | – | dBc | With Typical Matching Components |
| Crystal Freq. Spurs | – | −50 | – | dBc | 50 kHz PLL Loop Bandwidth |
| Time TX to RX | – | – | 1 | ms | |
| **Analog RX** | | | | | |
| Frequency Range | 402 | 403.5 | 405 | MHz | Targeted |
| | 300 | – | 768 | MHz | Non-quick Start |
| | 350 | – | 448 | MHz | Quick Start |
| Modulation | 1 | – | 8 | kbps | Manchester-coded Data |
| | 1 | – | 16 | kbps | NRZ Data |
| RF Input | −117 | – | −10 | dBm | |
| Noise Figure | – | 4.5 | – | | |
| RF Detect Time | 100 | – | – | μs | In Sniff Mode |
| Time RX to TX | – | – | 1 | ms | |

## PIN DEFINITIONS

This section describes the pins of the AMIS−52150 package.

**Table 4. PIN DESCRIPTION**

| Pin# | Name | Type | Comments |
|---|---|---|---|
| 1 | RX1 RF | RF | Receive RF Input 1 |
| 2 | RX2 RF | RF | Receive RF Input 2 |
| 3 | VCO2 | Analog | Voltage Controlled Oscillator 2 |
| 4 | VCO1 | Analog | Voltage Controlled Oscillator 1 |
| 5 | LPFILT | Analog | Loop Filter |
| 6 | RSSI/Bandgap Out | Analog | Analog RSSI Output or Bandgap Output |
| 7 | NC | | No Electrical Connection |
| 8 | CREF | Analog | Current Bias Precision Resistor |
| 9 | GND | Analog | Analog/Digital Ground |
| 10 | CLKOUT | Digital | RC, XTAL, or Data Clock Output |
| 11 | X1 | Analog | Xtal Input |
| 12 | X2 | Analog | Xtal Output |
| 13 | IIC Data | Digital | IIC Interface Data I/O |
| 14 | NC | | No Electrical Connection |
| 15 | IIC Clock | Digital | IIC Interface Clock |
| 16 | TX/RX DATA | Digital | Data Transmit, Data Receive or Recovered Data |
| 17 | VDD | Analog | Positive Power Supply |
| 18 | RFPWR | Analog | Regulated Voltage<br>Output for RF Transmitter Circuitry |
| 19 | RFOUT RF | RF | Transmit RF Output |
| 20 | RFGND | Analog | RF Ground |

## PIN DESCRIPTIONS

### RX1, Rx2, RF Input Pins

RX1 and RX2 are the RF antenna inputs to the AMIS−52150. The internal circuit designs are identical between these inputs. For the AMIS−52150 receiver inputs, RX1 and RX2, external components are required in order to match the low noise amplifier (LNA) to external devices such as antennas. The external components must provide a DC voltage path to the RF ground. Figure 2 suggests an external circuit for the receiver inputs at 403 MHz. Each circuit's input impedance can be trimmed internally to compensate for manufacturing and external component tolerances. The circuits employ an LNA, internal filters, a low frequency, intermediate frequency (IF), and a received signal strength indication (RSSI) circuit to recover the ASK/OOK modulated data. The signals in the two input channels are "summed" before the data recovery circuit.

The functions of the receive circuits are controlled by writing to the registers shown in Table 5.

**Table 5. RECEIVER CONTROL REGISTER DESCRIPTION**

| RX1 or RX2 Receiver Register Control | | | | |
|---|---|---|---|---|
| **Register (HEX)** | **Name** | **Bits** | **States** | **Comments** |
| 0x00 | ANT1 Trim | All | | Inverse Relationship Register Value to Internal Capacitance |
| 0x01 | ANT2 Trim | All | | Inverse Relationship Register Value to Internal Capacitance |
| 0x0c | ANT1 Enable | 0 | 0 | Antenna Port is Off |
| | | | 1 | Antenna Port is On |
| | ANT2 Enable | 1 | 0 | Antenna Port is Off |
| | | | 1 | Antenna Port is On |

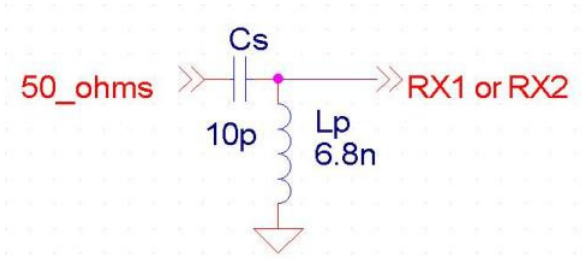


**Figure 2. Typical Input Impedance Match to 50 Ω (402 MHz)**

### VCO1, VCO2, Voltage Controlled Oscillator Pins

The VCO1 and VCO2 pins connect a parallel combination of a capacitor and an inductor to the AMIS−52150 internal voltage controlled oscillator (VCO). The external LC (parallel inductor and capacitor) circuit sets the frequency of the internal VCO. The VCO frequency must be set to twice the value of the desired TX or RX frequency. Typical components for the tuning of the VCO at 402 MHz are shown in Figure 3. The range of the VCO frequency is from 600 MHz to 1536 MHz.

The voltage on these pins can be used to determine proper operation of the PLL/VCO circuits.

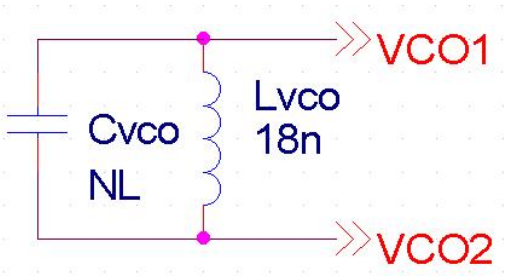


**Figure 3. Typical Components for VCO Tuning at 402 MHz**

**Table 6. VCO CONTROL REGISTERS**

| VCO/PLL Control Registers | | | | |
|---|---|---|---|---|
| **Register (HEX)** | **Name** | **Bits** | **States** | **Comments** |
| 0x06 | Charge Pump | 0, 1 | 00 | 20 μA |
| | | | 01 | 25 μA |
| | | | 10 | 50 μA* |
| | | | 11 | 100 μA |
| | VCO Current | 2, 3, 4 | 000 | 180 μA |
| | | | 001 | 220 μA |
| | | | 010 | 260 μA |
| | | | 011 | 300 μA |
| | | | 100 | 340 μA* |
| | | | 101 | 380 μA |
| | | | 110 | 420 μA |
| | | | 111 | 460 μA |
| | PLL Divider | 7 | 0 | Divider is 64 |
| | | | 1 | Divider is 128 |

* Denotes the normal value.

### LPFILT, Loop Filter Pin

The LPFILT pin connects the AMIS−52150 internal phase lock loop (PLL) frequency synthesizer to an external loop filter (Figure 4). An external loop filter allows the system designer to optimize the operation of the AMIS−52150 in order to meet the requirements for a specific end application.

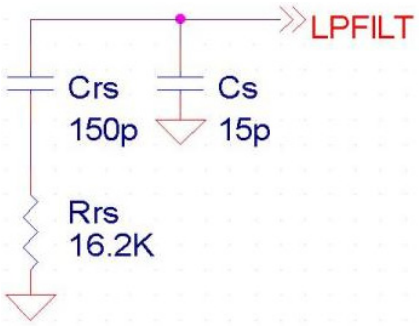


**Figure 4. Typical Loop Filter**

### RSSI/BG, Analog Output Pin

The RSSI/BG pin is used to output either the signal from the RSSI circuits, or to output the voltage from the bandgap voltage reference or a bypass capacitor node, respectively. The RSSI output is a true analog representation of the received signal level. The pin can also be programmed to output the voltage of the bandgap voltage reference. When using the AMIS−52150 in the clock and data recovery mode, a capacitor needs to be connected from the RSSI/BG pin to ground. A typical value for this capacitor is 2.2 nF. Additional information on the CDR function can be found later in this document. Table 7 presents the registers that control the function of the RSSI/BG pin.

**Table 7. RSSVBG PIN CONTROL REGISTERS**

| RSSI Pin Definition Control Registers | | | | |
|---|---|---|---|---|
| **Register (HEX)** | **Name** | **Bits** | **States** | **Comments** |
| 0x0e | Bandgap on RSSI | 3 | 0 | Normal Operation |
| | | | 1 | BG Output on RSSI* |
| 0x1e | RSSI Ext Amp | 4 | 0 | Tri-stated |
| | | | 1 | RSSI Signal |

* Note that device needs to be in RX, TX or crystal-on mode for bandgap voltage to be present on pin.

### CREF, Current Reference Bias Pin

A resistor must be connected to the CREF pin to provide a current bias to the internal bandgap voltage reference circuit. It is critical that this resistor value is 33.2 kΩ (with one percent or better tolerance) to achieve proper operation of the bandgap voltage reference.

### GND, Ground Pin

The GND pin is the ground connection for the digital and analog circuits.

### CLKOUT, Internal Clock Output Pin

The CLKOUT pin is an output for the RC oscillator, crystal oscillator signal or the recovered data clock, respectively. The crystal oscillator signal output can be divided by 2, 3 or 4. The pin can also be programmed to output the signal from the recovered data clock function. For more information about the clock and data recovery (CDR) function of the AMIS−52150, refer to the section of this document on clock and data recovery.

The CLKOUT pin function control registers are shown in Table 8.

**Table 8. OSCILLATOR OUTPUT CONTROL REGISTERS**

| CLKOUT Pin Definition Control Registers | | | | |
|---|---|---|---|---|
| **Register (HEX)** | **Name** | **Bits** | **States** | **Comments** |
| 0x0c | CLKOUT Enable | 7 | 0 | CLKOUT is Enabled |
| | | | 1 | CLKOUT is Disabled |
| 0x0d | CLKOUT Select | 4, 5 | 00 | Automatic Control |
| | | | 01 | RC OSC |
| | | | 10 | Xtal |
| | | | 11 | Off |
| 0x0e | XTAL Divide | 0, 1 | 00 | Divide by 4 |
| | | | 01 | Divide by 3 |
| | | | 10 | Divide by 2 |
| | | | 11 | Divide by 1 |

### X1, X2, External Crystal Reference Pins

X1 and X2 pins connect a parallel resonance oscillator crystal to the AMIS−52150 internal oscillator circuit. The external crystal should meet the requirements as listed in Table 9. However, the two load capacitors should be sized slightly smaller than the recommended value for the crystal, because of the added capacitance due to the internal trim circuit. The crystal parameters are shown in Table 9.

**Table 9. EXTERNAL CRYSTAL PARAMETERS**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Crystal Frequency | 12.56 | – | 12.65 | MHz | Targeted |
| | 9.375 | – | 24.0 | | Non-quick Start |
| | 10.9 | – | 14.0 | | Quick Start |
| Crystal ESR | – | – | 70 | Ω | |
| Crystal Tolerance | – | 10 | – | ppm | |
| Load Capacitance | Load Capacitors should be Smaller than Recommended for the Crystal to allow for Frequency Tuning | | | | |

### $I^2C$DATA, $I^2C$CLK, $I^2C$ Control Interface Bus Pins

The AMIS−52150 implements an $I^2C$ serial 8-bit bi-directional interface with the pins $I^2C$DATA and $I^2C$CLK. The device implements the protocol for a slave device. The clock for the interface is generated by the external master device. The interface will support the normal (0 – 100 kbits/second) or the fast (0 – 400 kbits/second) data modes. The interface conforms to the Phillips specification for the $I^2C$ bus standard. The pins have internal pull-up resistors. See Table 10 and Table 11 for some parameters of this interface.

In addition, Table 12 shows the details of register that controls the $I^2C$ address increment function.

**Table 10. INTERNAL $I^2C$ PULL-UP RESISTORS**

| Pin | Function | Typ | Unit |
|---|---|---|---|
| $I^2C$DATA | Internal Pull-up R | 15 | kΩ |
| $I^2C$CLK | Internal Pull-up R | 15 | kΩ |

**Table 11. I²C BUS DEVICE ADDRESSING**

| Device | Address (Bin) | HEX | Function |
|---|---|---|---|
| AMIS−52150 | 01101000 | 68 | Device Write |
| AMIS−52150 | 01101001 | 69 | Device Read |

**Table 12. I²C CONTROL REGISTER**

| Register (HEX) | Name | Bits | States | Comments |
|---|---|---|---|---|
| 0x0c | I²C Address Increment | 2 | 0 | Increment after Write |
| | | | 1 | Do Not Increment |

The I²CDATA and I²CCLK lines are also used to signal to an external controller certain internal activities of the transceiver. The receiver is activated upon detection of RF energy during Sniff Mode operation. The wake-up timer can also be configured to wake-up the device in order to alert an external controller to perform specific tasks, as defined by the system designer.

### TX/RX, Data Input/Output Pin

The transmit/receive (TX/RX) pin can be programmed to be either an input for RF transmissions, or an output for RF reception, or the output of the RC oscillator signal, or the output of the recovered data from the CDR circuits, respectively.

In transmit mode, this pin is the digital data input to the AMIS−52150 RF transmit circuit. The digital data results in the On and Off cycling of the output power amplifier (PA). The AMIS−52150 does not perform any protocol conversion on the data bit stream; it is simply a serial bit stream. The state of the TX/RX pin either turns the output amplifier On (enabling RF transmission) or turns the output amplifier Off (disabling RF transmission). The TX/RX input can be inverted which causes the state control of the RF output amplifier to be inverted as well.

In receive mode, this pin is the digital data output from the AMIS−52150 receivers. The received data is recovered as a high/low (digital ones and zeros) serial bit stream; the AMIS−52150 does not modify the received data protocol. The data output state due to the presence of energy in the receiver can be programmed to be either a high level or a low level at the TX/RX pin. An external controller is needed to decode the information in the recovered data bit stream.

When programmed to be an oscillator output, the TX/RX pin outputs the signal from the RC oscillator. This signal can be used to monitor the frequency of the RC oscillator in order to trim the frequency to the desired value.

The TX/RX pin can be programmed to output the recovered data obtained from the clock and data recovery circuits. In this case, the device must be programmed in the CDR mode. More information on CDR will be provided in a later section of this data sheet.

The functions of the TX/RX port are controlled by the values of the register settings, as shown in Table 13.

**Table 13. TX/RX PIN DEFINITION CONTROL REGISTERS**

| Register (HEX) | Name | Bits | States | Comments |
|---|---|---|---|---|
| 0x0e | RC OSC on TX/RX | 2 | 0 | RX/TX Normal |
| | | | 1 | RC OSC Output |
| 0x1e | TX/RX Invert | 5 | 0 | Normal Levels |
| | | | 1 | Inverted |

### VDD, Supply Voltage Pin

The VDD pin is the power supply pin for the AMIS−52150. The voltage on this pin is typically 3.0 V. Please refer to the section “Operating and Maximum Specifications” of this document for the VDD operating conditions.

### RFPWR, DC Voltage Output Pin

In the AMIS−52150, a regulated DC voltage is generated and outputted at the RFPWR pin. This voltage should be fed through a DC connection to the RFOUT pin in order to power the output stage of the RF PA. The voltage level is adjusted based on the value of the register setting, as shown in Table 14.

**Table 14. TX VOLTAGE CONTROL REGISTER**

| RFPWR Voltage Control Register | | | |
|---|---|---|---|
| **Register (HEX)** | **Name** | **Bits** | **Comments** |
| 0x02 | RFPWR Trim | All | 0xff is Highest Power |

### RFOUT, RF Output Signal Pin

In the AMIS−52150, a high efficiency non-linear output driver is used to produce the high power RF signal. This driver must be connected through a DC connection to the RFPWR pin. External components are required to match the output to a 50 Ω load, or to an external antenna, respectively.

Figure 5 shows a typical matching circuit for the RFOUT pin.

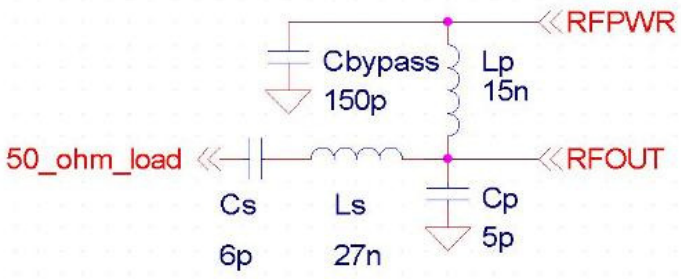


**Figure 5. Typical RFOUT Output Impedance Match to 50 Ω (402 MHz)**

## CIRCUIT FUNCTIONAL DESCRIPTION

The functions of the AMIS−52150 are presented in this section. These functions are:

- Receiver
- Transmitter
- Sniff Mode
- Quick Start
- Data Detection
- Data and Clock Recovery
- Application Wake-up
- $I^2C$ Interface
- Registers
- Power-on-Reset/Brown-out
- Alternative Wake-up

### Receiver

RF signals often suffer from reflections along the path of propagation. These reflected signals arrive at the receiver antenna with different phases or time delays. The different phases of the reflected signals cause the signal strength at the receiver to vary. This variation can be large enough to cause the receiver to miss information. The AMIS−52150 sums the signals from the dual receiver channels within the data detection circuits. This reduces the effect of multi-path reflections. Proper operation requires a) trimming aimed at minimizing the frequency tolerances, b) tuning of the oscillator frequency, c) selection of the data rate filters, and d) setting of a signal threshold, as shown in Table 15.

Table 16 lists some characteristic parameters for the receivers. Figure 6 shows a typical received data waveform.

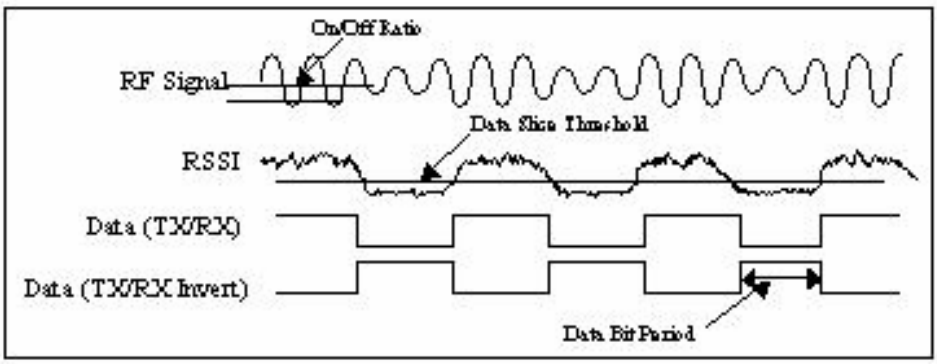


**Figure 6. Received Waveform**

**Table 15. RECEIVER CONTROL REGISTERS**

| RX1 or RX2 Receiver Register Control | | | | |
|---|---|---|---|---|
| **Register (HEX)** | **Name** | **Bits** | **States** | **Comments** |
| 0x00 | ANT1 Trim | All | | Inverse Relationship Register Value to Internal Capacitance |
| 0x01 | ANT2 Trim | All | | Inverse Relationship Register Value to Internal Capacitance |
| 0x05 | RX XTAL Tune | All | | |
| 0x0a | Data Threshold | All | | Reference Level for Detecting Data Logic State |
| 0x0c | ANT1 Enable | 0 | 0 | Antenna Port is Off |
| | | | 1 | Antenna Port is On |
| | ANT2 Enable | 1 | 0 | Antenna Port is Off |
| | | | 1 | Antenna Port is On |
| | RX Enable | 3 | 0 | Receiver is Off |
| | | | 1 | Receiver is On |
| 0x0f | Data Filter | 4, 5, 6 | 000 | 1.1 kHz |
| | | | 001 | 2.3 kHz |
| | | | 010 | 5.2 kHz |
| | | | 011 | 10.4 kHz |
| | | | 100 | 1.18 kHz |
| | | | 101 | 2.57 kHz |
| | | | 110 | 7.0 kHz |
| | | | 111 | 20.45 kHz |
| 0x1e | TX/RX Invert | 5 | 0 | Normal Levels |
| | | | 1 | Inverted |

**Table 16. RF INPUT ELECTRICAL CHARACTERISTICS**

| Specification | Settings | Conditions | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Input Resistance | | | 2 | – | kΩ | |
| Input Capacitance | Trim 0x00 | Min. Tune | 3 | – | pF | |
| | Trim 0xff | Max. Tune | 6 | – | pF | |
| Sensitivity | | 1 kbps | −117 | – | dBm | w/CDR |
| Frequency | | | 403.5 | – | MHz | Target Frequency |
| Max. Input | | | – | −10 | dBm | |
| IP3 | | | +8 | – | dBm | |
| IP2 | | | +66 | – | dBm | |

### Transmitter

The RF transmitter is a non-linear open drain device. It requires a DC signal path to RFPWR, which is the output of the internal power supply to the transmitter. The transmitter is switched On and Off with the serial transmit data stream. To achieve the desired output waveform, a tuned external resonant circuit is required. This resonant circuit should be designed to achieve the desired output frequency. This circuit includes a parallel LC tank (Lp and Cp) tuned to 402 MHz (including internal capacitance), as well as a series LC (Ls and Cs) to produce a 403 MHz output. The transmitter output is also to be filtered in order to reduce the harmonics to acceptable levels. It is further required that the transmitter output power level is programmed, that the transmit frequency is tuned and that the data rate is selected, respectively (Table 17).

Table 18 lists some characteristic parameters for the transmitter, while a typical transmitter output waveform is shown in Figure 7.

**Table 17. TRANSMITTER CONTROL REGISTERS**

| TX/RX Definition Control Registers | | | | |
|---|---|---|---|---|
| **Register (HEX)** | **Name** | **Bits** | **States** | **Comments** |
| 0x02 | TX Power | All | | |
| 0x04 | TX XTAL Trim | All | | |
| 0x0c | TX Enable | 4 | 0 | Transmitter is Off |
| | | | 1 | Transmitter is On |
| 0x0f | Data Filter | 4, 5, 6 | 000 | 1.1 kHz |
| | | | 001 | 2.3 kHz |
| | | | 010 | 5.2 kHz |
| | | | 011 | 10.4 kHz |
| | | | 100 | 1.18 kHz |
| | | | 101 | 2.57 kHz |
| | | | 110 | 7.0 kHz |
| | | | 111 | 20.45 kHz |
| 0x1e | TX/RX Invert | 5 | 0 | Normal Levels |
| | | | 1 | Inverted |

**Table 18. OUTPUT IMPEDANCE CHARACTERISTICS**

| Specification | Settings | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Impedance | | Resistance | – | 22 | – | Ω |
| | | Capacitance | – | 3 | – | pF |
| Output Power | RFPWR 0x00 | | – | −26 | – | dBm |
| | RFPWR 0xff | | 11 | 12 | 13 | |
| Harmonics | | Ext. Circuit | – | −35 | – | dBm |
| Frequency Range | | Target | 402 | – | 405 | MHz |
| | | Quick Start | 350 | – | 448 | |
| | | Full Range | 300 | – | 768 | |
| Modulation | | | | ASK/OOK | | |
| On/Off Ratio | TX Output | | – | 70 | – | dBm |

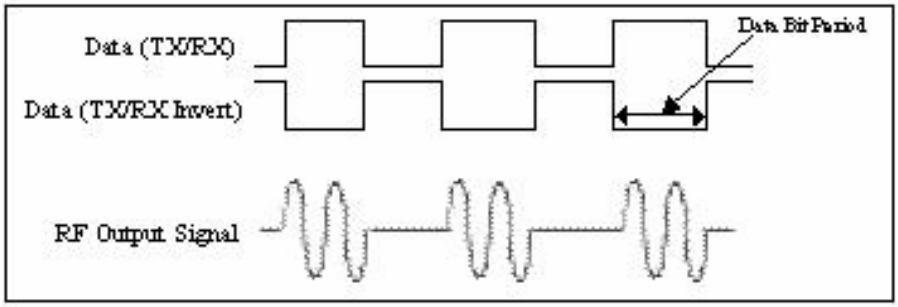


**Figure 7. Transmit Waveforms**

### Sniff Mode

Applications based on low power consumption require Sniff Mode operation of the AMIS−52150. This mode turns off the receiver and the crystal oscillator during programmable, regular time intervals. At the end of each time interval, the receiver wakes up and sniffs for the incoming RF energy. If energy is detected, the receiver transitions to the full receive mode and starts data recovery from the RF carrier. If energy is not detected, the receiver

returns to the low power or “sleep” state. Sniff Mode operation is programmable; the “sleep” time as well as multiple delay sequences can be fully programmed. Table 19 lists the Sniff Mode control registers.

Typical timing waveforms for operation in Sniff Mode are shown in Figure 8 and Figure 9.

**Table 19. SNIFF FUNCTION CONTROL REGISTERS**

| Control Registers Associated with the Sniff Function | | | | |
|---|---|---|---|---|
| **Register (HEX)** | **Name** | **Bits** | **States** | **Comments** |
| 0x0b | SNIFF Threshold | All | | Reference Level for Detected RF |
| 0x0c | Wake on RSSI | 5 | 0 | Do Not Wake on RSSI |
| | | | 1 | Wake on RSSI > Threshold |
| 0x0d | SNIFF TIMER RES | 3 | 0 | Resolution is Set to 0.5 mS per Step |
| | | | 1 | Resolution is Set to 64 mS per Step |
| 0x13 | DATA FILTER | All | | Delay from RX Wakeup to Data Sampled |
| 0x16 | IRQ DELAY | All | | Time $I^2C$ and TX/RX are Active to Indicate a Wakeup |
| 0x18 | RSSI DELAY | All | | Delay from Wakeup to RSSI Being Checked |
| 0x19 | SNIFF TIMER | All | | Time that Receiver is Off in Sniff Mode |
| 0x1a | OFFSET DWELL | All | | Time Allowing Receiver to Power Up (Typically > 40 μS) |
| 0x1b | DATA FILTER PRE-DIVIDER | All | | Delay from Data Detection to Pre-clock Output |

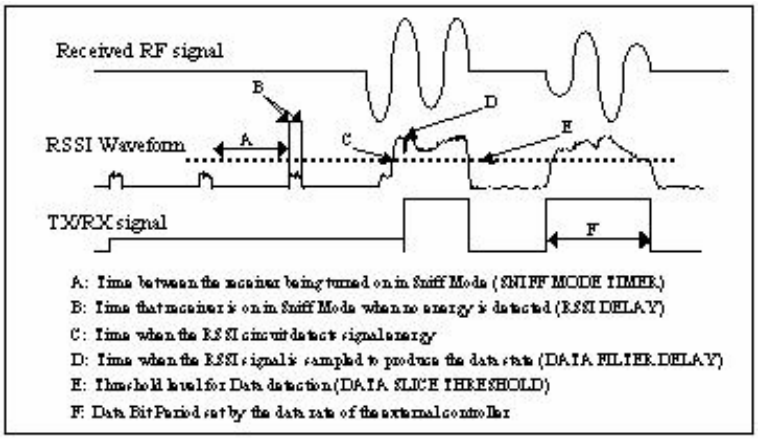


**Figure 8. Receiver Data Acquisition in Sniff Mode**

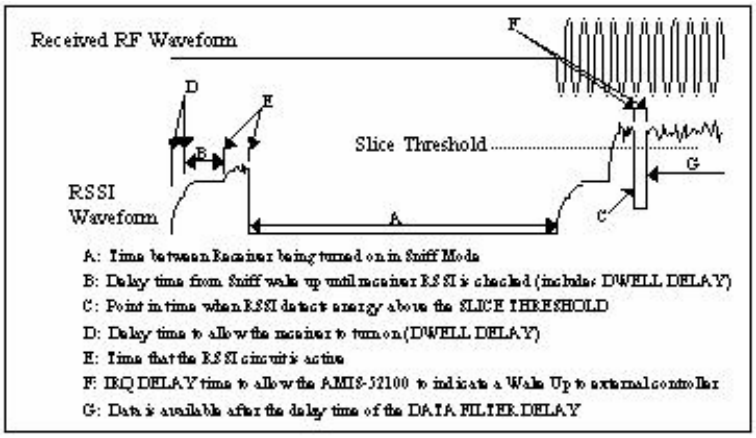


**Figure 9. Sniff Timing at RF Energy Detection**

### Quick Start

There are two oscillators in the AMIS−52150, a low power 10 kHz RC oscillator and a crystal oscillator, respectively.

The RC oscillator is used to keep the AMIS−52150 running in the ultra-low power mode. This oscillator is used to generate the clock signals for the Sniff Mode timers as well as the wake-up timers. Figure 10 shows a block diagram of the clocks in the AMIS−52150. The crystal oscillator provides the reference frequency which is used to generate the RF frequencies for transmission and receiving of data. It is also the reference for all the timing functions in the AMIS−52150. The RC oscillator is in turn used to produce a “kicker” signal when the Quick Start function of the crystal oscillator is needed.

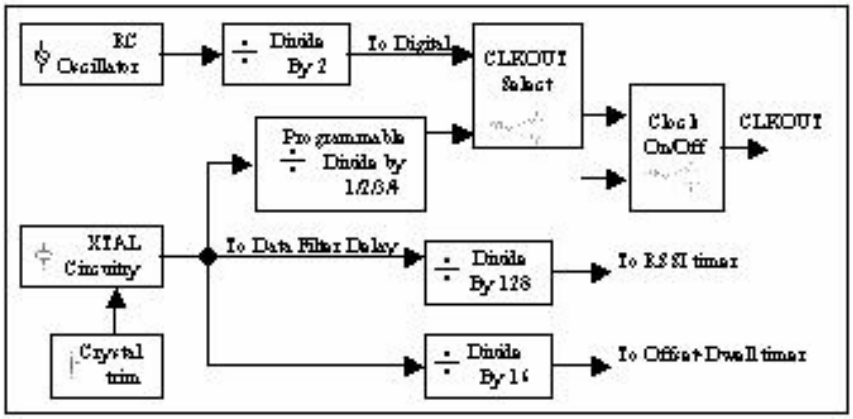


**Figure 10. Internal Clocks**

A “kicker” circuit stimulates the crystal oscillator circuit with oscillations close to the final frequency. This significantly reduces the time it takes for the oscillator to reach and lock to the final frequency. The Quick Start function is necessary for operation in Sniff Mode. Table 20 lists the Quick Start control registers.

**Table 20. QUICK START CONTROL REGISTERS**

| Register (HEX) | Name | Bits | States | Comments |
|---|---|---|---|---|
| 0x03 | Kick Trim | All | | Trim the Internal RC OSC to Form a Kick-start to the XTAL Oscillator |
| 0x0e | Kick Config1 | 4 | 0 | Common Mode Clamp Disabled (Startup) |
| | | | 1 | Common Mode Clamp Enabled (Normal) |
| | Kick Config2 | 5 | 0 | Normal Operation |
| | | | 1 | Continuous Kick On |

### Data Detection

The RSSI circuit creates an analog voltage waveform (18 mV/dB) that follows the signal strength of the RF signal. The data slice circuit then samples that waveform to create the digitized data. The slice circuit in the AMIS−52150 can be programmed to operate in one of three modes; DAC mode, Average mode or Peak mode. The DAC mode compares a fixed slice threshold value to the level in the slice output. The digital data state is determined by the level of the slice output being above or below that fixed threshold. Figure 11 shows a typical waveform for the DAC mode, while Table 21 shows the control registers for the auto slice modes.

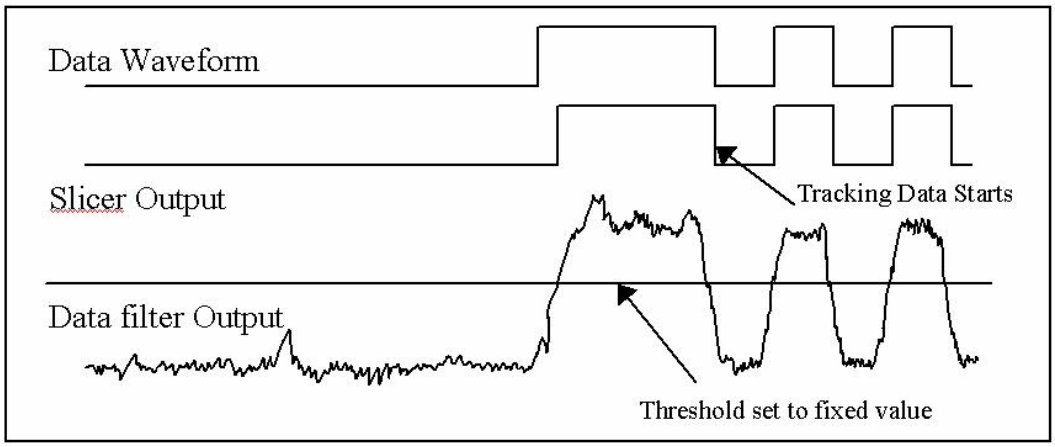


**Figure 11. DAC Slice Mode Waveform**

In the Average mode, the threshold value is generated automatically. This threshold value is then compared to the output of the slice circuit to re-create the digital data. The slice circuit along with an external capacitor are used to generate a charging time constant which is equal to charging to 95 percent of a bit level in two bit time periods. The data protocol should add a header to the data to allow the slice circuit to determine the average level. Figure 12 shows a typical waveform for the Average mode. Table 21 shows the control registers for the auto slice modes.

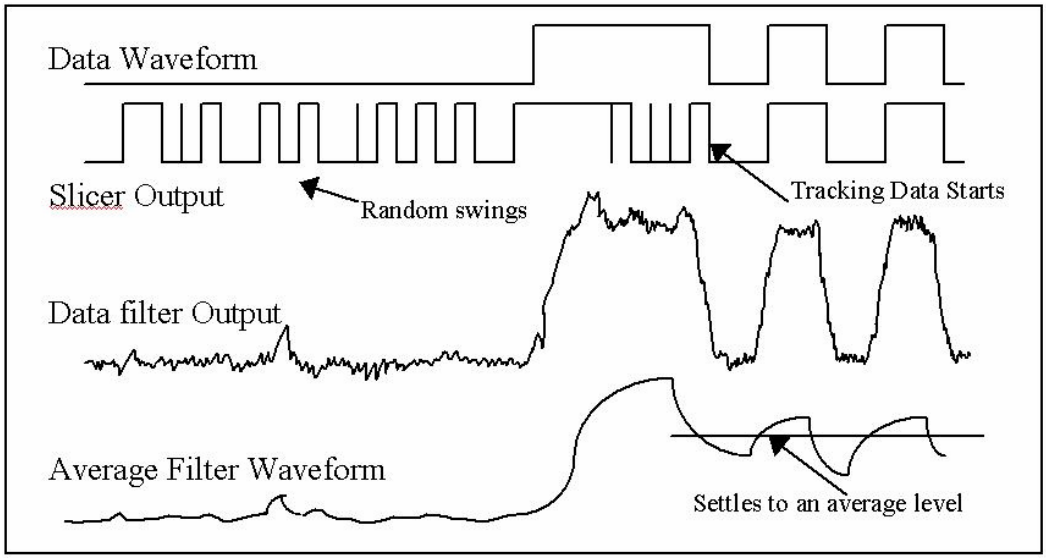


**Figure 12. Average Slice Mode Waveform**

In the Peak mode, a threshold value is generated automatically as well. This threshold value is then compared to the output of the slice circuit to re-create the digital data. The operation of the slice circuit is based on an external capacitor with an internal peak detector, in order to arrive at the peak value of the data waveform. The threshold value is set 6 dB below this peak value. The capacitor value should be selected so that the peak detector does not discharge during periods of continuous zeros, while being small enough to allow the peak detector to reach the peak value quickly. Figure 13 shows a typical waveform for the Peak mode.

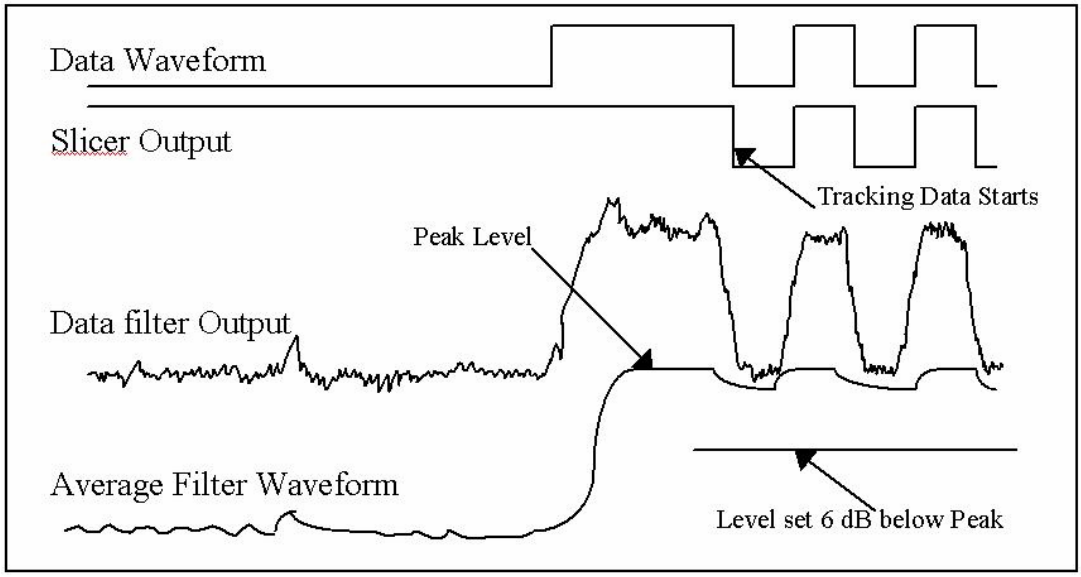


**Figure 13. Peak Slice Mode Waveform**

**Table 21. AUTO SLICE CONTROL REGISTERS**

| Register (HEX) | Name | Bits | States | Comments |
|---|---|---|---|---|
| 0x0a | DATA SLICE THRESHOLD | All | | Set a Fixed Reference Level for the Slice Output to be Compared to in the DAC Mode |
| 0x0f | HYSTERESIS | 0, 1 | 00 | 0 mV Hysteresis Used in the Threshold Circuit |
| | | | 01 | 20 mV Hysteresis Used in the Threshold Circuit |
| | | | 10 | 50 mV Hysteresis Used in the Threshold Circuit |
| | | | 11 | 100 mV Hysteresis Used in the Threshold Circuit |
| | AUTOSLICE | 2, 3 | 00 | DAC Mode Used for Data Detection (DEFAULT) |
| | | | 01 | Average Mode Used for Data Detection |
| | | | 10 | Peak Mode Used for Data Detection |
| | | | 11 | DAC Mode Used for Data Detection |

### Data and Clock Recovery

Data recovered in a noisy environment or from a weak RF signal is usually jittery. The AMIS−52150 can remove much of that data jitter by recovering a synchronous clock signal from the incoming data. The device can be set to achieve auto slice data detection. The clock and data recovery circuits can be programmed to generate a data clock for synchronously clocking the data output from the transceiver, removing much of the jitter in this process. The AMIS−52150 has an internal PLL that must be programmed to the frequency of the data by setting the values in the FWORD register and setting the coefficients of the filter. If these values are close to the data rate, the device will recover the data clock from the incoming detected data. The CDR circuit can also be set to a given tolerance with respect to the frequency difference between the target data rate and the actual data rate, in order to improve the performance of the CDR function. The CDR circuit can also be configured to reset after a programmed number of data time periods if no data is received. This “stop and check” function allows the CDR circuit to re-acquire the clock data when new data is received, maintaining better clock to data synchronization.

Table 22 lists the registers associated with the data and clock recovery function.

**Table 22. DATA AND CLOCK RECOVERY CONTROL REGISTERS**

| Data and Clock Recovery Associated Registers | | | | |
|---|---|---|---|---|
| **Register (HEX)** | **Name** | **Bits** | **States** | **Comments** |
| 0x07 | FWORD LSB | All | | Sets the Initial Internal Clock Frequency for the Clock and Data Recovery Circuits |
| 0x08 | FWORD | All | | |
| 0x09 | FWORD MSB | All | | |
| 0x0d | DATA MUX | 6 | 0 | TX/RX Normal Signals |
| | | | 1 | Recovered Data on TX/RX |
| | CLKMUX | 7 | 0 | Normal CLKOUT Signals |
| | | | 1 | Recovered CLOCK Output on CLKOUT |
| 0x10 | $K_0$ | 0, 1, 2 | 000 | Filter Coefficient Gain is 1 |
| | | | 001 | Filter Coefficient Gain is 2 |
| | | | 010 | Filter Coefficient Gain is 4 |
| | | | 011 | Filter Coefficient Gain is 8 |
| | | | 100 | Filter Coefficient Gain is 16 |
| | | | 101 | Filter Coefficient Gain is 32 |
| | | | 110 | Filter Coefficient Gain is 64 |
| | | | 111 | Filter Coefficient Gain is 128 |
| | $K_1$ | 4, 5, 6 | 000 | Filter Coefficient Gain is 1 |
| | | | 001 | Filter Coefficient Gain is 2 |
| | | | 010 | Filter Coefficient Gain is 4 |
| | | | 011 | Filter Coefficient Gain is 8 |
| | | | 100 | Filter Coefficient Gain is 16 |
| | | | 101 | Filter Coefficient Gain is 32 |
| | | | 110 | Filter Coefficient Gain is 64 |
| | | | 111 | Filter Coefficient Gain is 128 |
| 0x11 | $K_2$ | 0, 1, 2 | 000 | Filter Coefficient Gain is 0.125 |
| | | | 001 | Filter Coefficient Gain is 0.250 |
| | | | 010 | Filter Coefficient Gain is 0.500 |
| | | | 011 | Filter Coefficient Gain is 1.000 |
| | | | 100 | Filter Coefficient Gain is 2 |
| | | | 101 | Filter Coefficient Gain is 4 |
| | | | 110 | Filter Coefficient Gain is 8 |
| | | | 111 | Filter Coefficient Gain is 16 |
| | FsDIV | 4, 5, 6 | 000 | Sample Frequency Divider is 2 |
| | | | 001 | Sample Frequency Divider is 4 |
| | | | 010 | Sample Frequency Divider is 8 |
| | | | 011 | Sample Frequency Divider is 16 |
| | | | 100 | Sample Frequency Divider is 20 |
| | | | 101 | Sample Frequency Divider is 32 |
| | | | 110 | Sample Frequency Divider is 40 |
| | | | 111 | Sample Frequency Divider is 48 |

**Table 22. DATA AND CLOCK RECOVERY CONTROL REGISTERS** (continued)

| Register (HEX) | Name | Bits | States | Comments |
|---|---|---|---|---|
| 0x12 | STOP CHECK | 0, 1 | 00 | Stop Check Bits: Disabled |
| | | | 01 | Stop Check Bits: 2 |
| | | | 10 | Stop Check Bits: 4 |
| | | | 11 | Stop Check Bits: 8 |
| | LOOPCLAMP | 2, 3 | 00 | Loop Clamp Value is: ±BaudClk/8 |
| | | | 01 | Loop Clamp Value is: ±BaudClk/16 |
| | | | 10 | Loop Clamp Value is: ±BaudClk/32 |
| | | | 11 | Loop Clamp Value is: ±BaudClk/64 |
| | FREERUN | 4 | 0 | Phase Alignment Enabled |
| | | | 1 | Phase Alignment Disabled |
| | CDR RESET | 5 | 0 | CDR Reset Disabled |
| | | | 1 | CDR Reset Enabled |
| | AUTO/MANUAL RESET | 6 | 0 | POR Reset (Auto) |
| | | | 1 | CDR Reset Enabled (Manual) |
| | SAMPLE WINDOW | 7 | 00 | Sampling Starts with Bit Start Edge |
| | | | 00 | Sampling Centered around Bit Center |

The clock and data recovery function is dependent on the receiver's ability to recover the data from the incoming RF signal. There exists a technique to test the clock and data recovery function without having to set up the receiver to receive data. This is a test mode that allows an input data stream (square wave at 1/2 the data rate) on the RSSI pin, with the recovered clock data appearing on the CLKOUT pin and the recovered data appearing on the TX/RX pin, respectively. Once the AMIS−52150 is configured for clock and data recovery, the register shown in Table 23 can be used to define the test mode operation.

**Table 23. CLOCK AND DATA RECOVERY TEST MODE**

| Clock and Data Recovery Test Control Register | | | |
|---|---|---|---|
| **Register (HEX)** | **Binary Code** | **HEX Code** | **Comments** |
| 0x1d | 00001110 | 0x0e | Normal RSSI Digital Input |
| | 00001111 | 0x0f | CDR Start Bit Digital Input to RSSI |

### Wake-up Function

Ultra-low power applications can take advantage of the wake-up function of the AMIS−52150. The AMIS−52150 can be placed in a low power or "sleep" state until an interrupt based on the programmable wake-up timer is generated. This wakes up the transceiver, which then flags the external microcontroller to perform the required application-specific operations. The wake-up interrupt is also generated based on detection of RF energy (Sniff Mode). Communication with the microcontroller takes place via the $I^2C$ bus. In addition, when the AMIS−52150 is in the "sleep" state, the wake-up signal can be generated by the microcontroller. Table 24 lists the registers associated with the wake-up function.

**Table 24. APPLICATION WAKE-UP CONTROL REGISTERS**

| Register (HEX) | Name | Bits | Comments |
|---|---|---|---|
| 0x14 | AW TIMER DIV | All | Divides the RC Oscillator to Form a Clock for the AW |
| 0x15 | AW TIMER | All | Number of AW Clock Periods before a AW Wake-up |
| 0x17 | PRE/POST AW DELAY | All | Number of CLKOUT Clock Periods before the TX/RX Pin Goes Low for a AW Cycle |

### I²C Interface

The I²C is a two pin bi-directional serial interface communication bus, with a data line and a clock line, respectively. Serial data on the data pin is clocked into or out of the AMIS−52150 by the clock pin. The AMIS−52150 is implemented as a slave device, which means that the external controller is the master device. The clock signal for all transmissions between the master (controller) and the slave (AMIS−52150) is generated by the controller. The serial communication bit rate can be as high as 400 kbps. A communication link is initiated based on a start sequence. Bi-directional communication continues as long as the master and slave acknowledge the write or read sequences, and is terminated with a stop sequence. This is illustrated in Figure 14, Figure 15 and Figure 16, respectively.

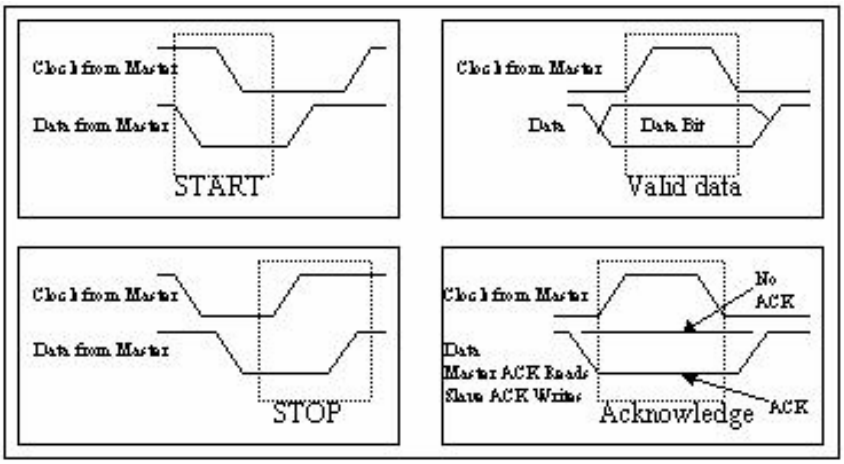


**Figure 14. I²C Valid Control Waveforms**

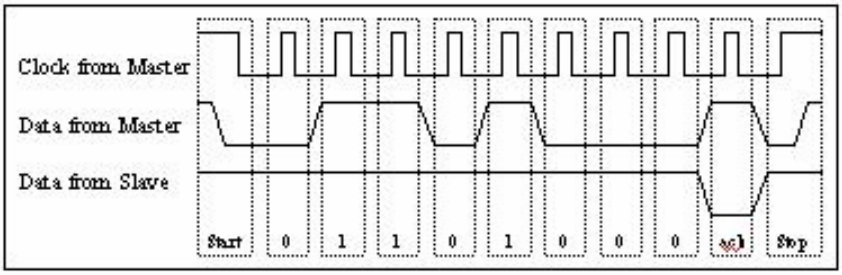


**Figure 15. I²C Protocol in a Write 68 (Hex) or a Data Write Request**

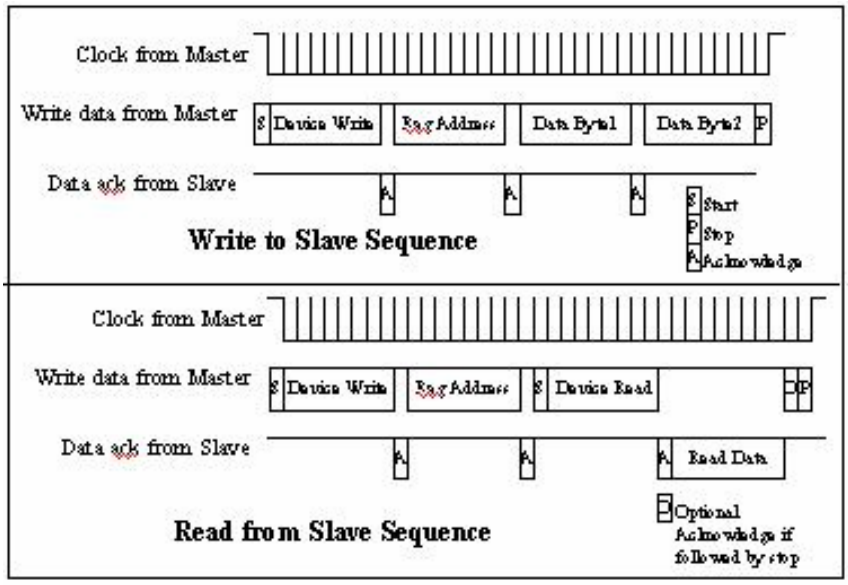


**Figure 16. I²C Write and Read Protocol**

### Registers

The AMIS−52150 is comprised of 31 registers.

### Power-on-Reset/Brown-out Detection

The POR/brown-out detection circuit ensures that the AMIS−52150 will be in a reset state when VDD drops below a certain threshold voltage, and remains in this state until VDD rises above another threshold voltage. The characteristics of the POR circuit are shown in Figure 17.

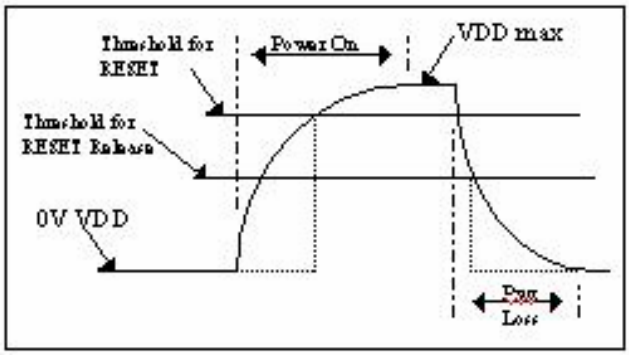


**Figure 17. Power-on-Reset Characteristics**

### Alternative Wake-up Functions

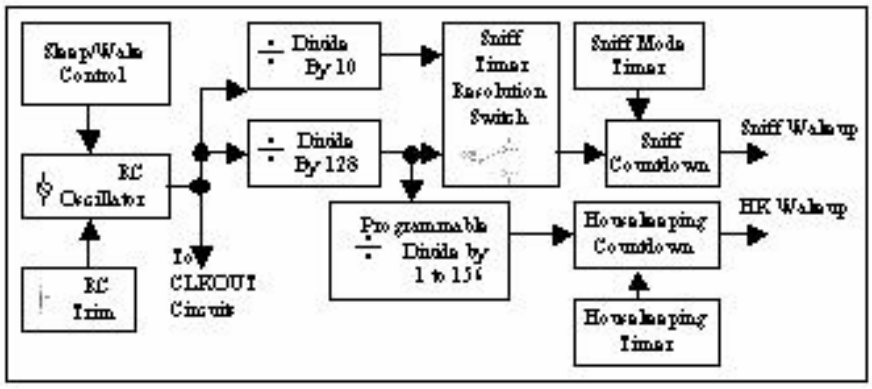


**Figure 18. Wake-up Circuits**

The AMIS−52150 will wake up from the low power mode upon a) reception of RF energy, b) an interrupt generated by the wake-up timer, or c) an interrupt generated by the external controller. In this low power mode, the RF circuits, the crystal oscillator, and the CLKOUT circuits are shut off, and only the RC oscillator and the wake-up divider circuitry are active. Once the AMIS−52150 receiver detects RF energy and wakes up, the RX/TX pin is set “low” while the $I^2C$DATA and $I^2C$CLK pins can remain “high”. In addition, when the wake-up timer wakes up the AMIS−52150 to in turn flag the external controller, the TX/RX and $I^2C$DATA pins are set “low” while the $I^2C$CLK pin can remain “high”. The external controller can also signal the AMIS−52150 to wake up by setting both the $I^2C$DATA and $I^2C$CLK lines low. These functions are shown in Table 25.

**Table 25. WAKE-UP TRUTH TABLE**

| Wake-up Source | TX/RX | $I^2C$ DATA | $I^2C$CLK | CLKOUT | Comments |
|---|---|---|---|---|---|
| SNIFF | 0 | 1 | 1 | XTAL Out | Wake on RF Energy Detect |
| HK Cycle | 0 | 0 | 1 | RC Oscillator | Wake due to HK Timer Timeout |
| External | 1 | 0 | 0 | Don’t Care | Wake due to External Controller |

**Table 26. ORDERING INFORMATION**

| Part Number | Package Type | Temperature Range | Shipping† |
|---|---|---|---|
| AMIS−52150−XTD | 20-pin SSOP<br>(209 mil, Shrink Small Outline Package) | 0°C to 50°C | Tube/Tray |
| AMIS−52150−XTP | 20-pin SSOP<br>(209 mil, Shrink Small Outline Package) | 0°C to 50°C | Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**TBD**



**PUBLICATION ORDERING INFORMATION**

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