1.0 General Description

The AMIS-39100 is a general purpose IC with eight integrated high side (HS) output drivers. The device is designed to control the power of virtually any type of load in a 12V automotive environment, such as transistor gates, relays, LEDs etc.

Each of the output drivers of the AMIS-39100 is able to drive up to 275mA continuously when connected to an inductive load of 300mH. Even higher driver output currents can be obtained as long as the total current of the device is limited. The integrated charge-pump of the AMIS-39100, which uses only one low cost external capacitor, avoids thermal runaways even if the battery voltage is low. The HS drivers withstand short to ground (even when AMIS-39100 has lost its ground connection), short to the battery and has over-current limitation. In case of a potential hazardous situation, the drivers are switched off and the diagnostic state of the HS drivers can be read out via serial peripheral interface (SPI). In case of a short to ground, the output driver is deactivated after a de-bounce time.

The AMIS-39100 can be connected to a 3.3V or 5V microcontroller by means of a SPI interface. This SPI interface is used to control each of the output drivers individually (on or off) and to read the status of each individual output driver (read-back of possible error conditions). This allows the detection of error situations for each driver individually. Furthermore, the SPI interface can be used to read-back the status of the built-in thermal shutdown protection. The AMIS-39100 has a low-power mode and excellent handling and system ESD characteristics.

2.0 Key Features

- Eight HS drivers
- Up to 830mA continuous current per driver pair (resistive load)
- Charge pump with one external capacitor
- Serial peripheral interface (SPI)
- Short circuit protection
- Diagnostic features
- Power-down mode
- Internal thermal shutdown
- 3.3V and 5V microcontroller compliant
- Excellent system ESD
- Automotive compliant
- SO28 package with low R_{thja}

3.0 Typical Applications

- Automotive dashboard
- Automotive load management
- Actuator control
- LED driver applications
- Relays and solenoids
- Industrial process control

4.0 Ordering Information

Product Name	Package	Temperature Range
AMIS39100AGA	PSOP 300-28 (JEDEC MS-013)	-40°C…105°C

5.0 Block Diagram

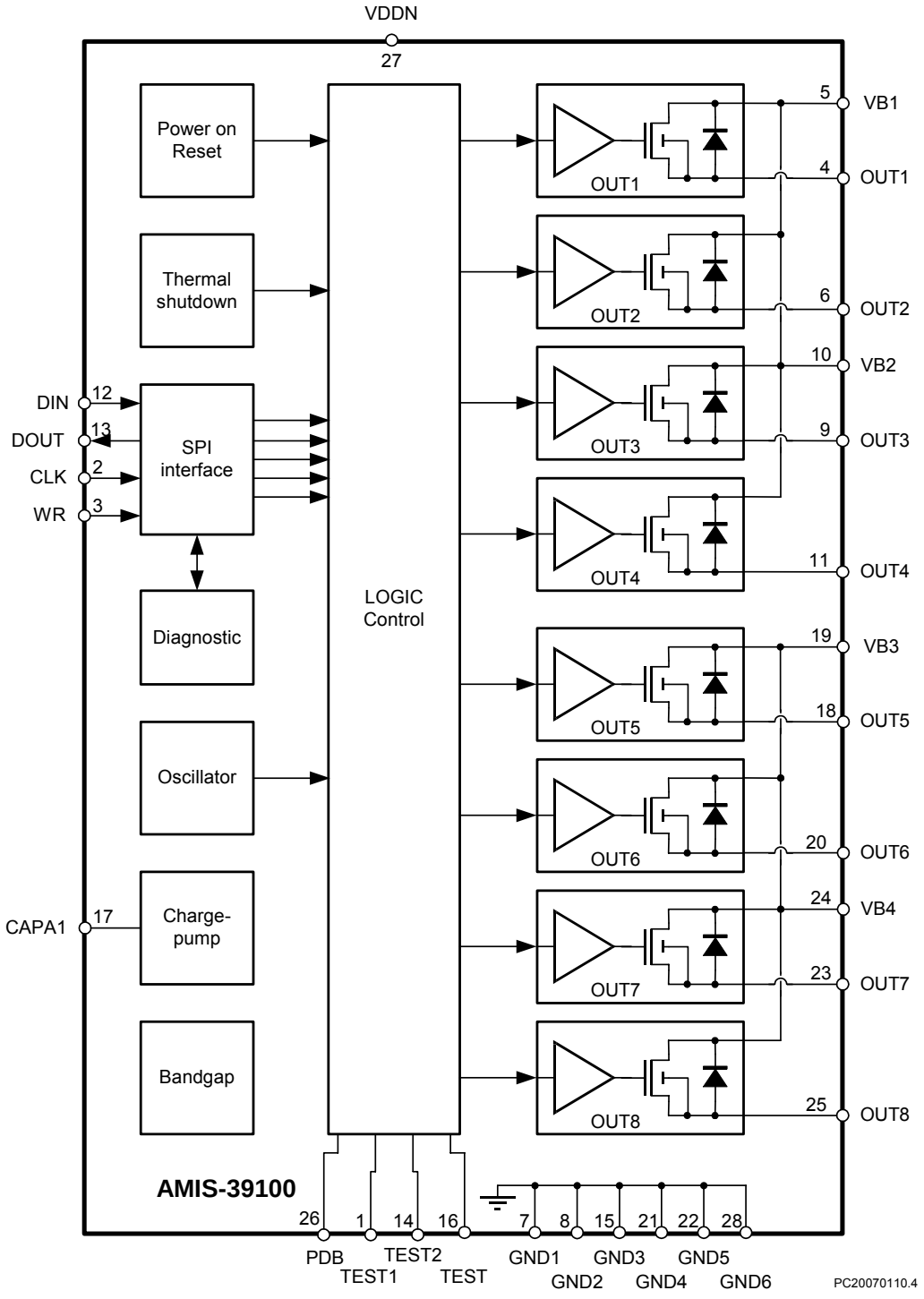

Figure 1: Block Diagram

6.0 Typical Application Diagram

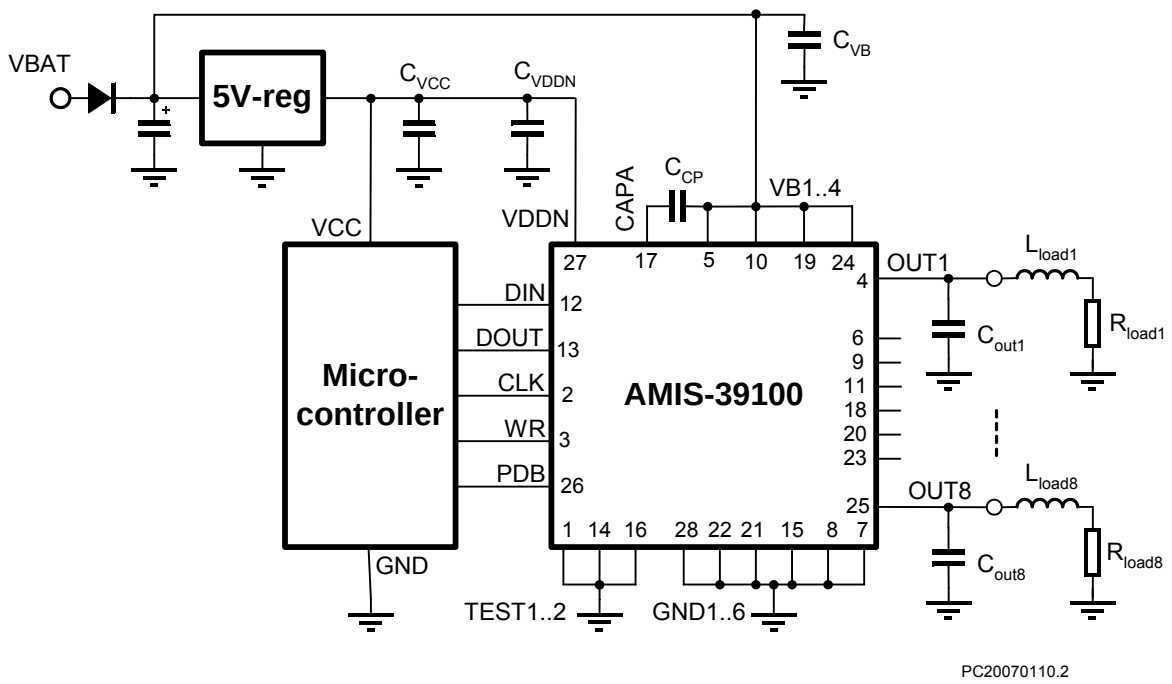

Figure 2: Typical Application Diagram

6.1 External Components

It is important to properly decouple the power supplies of the chip with external capacitors that have good high frequency properties.

The VB1, VB2, VB3, and VB4 pins are shorted on the PCB level. Also GND1, GND2, GND3, GND4, GND5, GND6, TEST, TEST1, and TEST2 are shorted on the PCB level.

Table 1: External Components

Component	Function	Min.	Value	Max.	Tol. [%]	Units
C_{VB}	Decoupling capacitor; X7R	100			± 20	nF
C_{charge_pump}	Charge pump capacitor(1)	0.47		47		nF
C_{out}(2)	EMC capacitor on connector	1				nF
C_{out}(2)	Decoupling capacitors on OUT 1 to 8; 50V	22			± 20	nF
C_{VDD}	Decoupling capacitors; 50V	22			± 20	nF
R_{Load}	Load resistance		65		± 10	Ω
L_{Load}	Load inductance at maximum current		300	350		mH

Notes:
(1) The capacitor must be placed close to the AMIS-39100 pins on the PCB.
(2) Both capacitors are optional and depend on the final application and board layout.

7.0 Pin Description

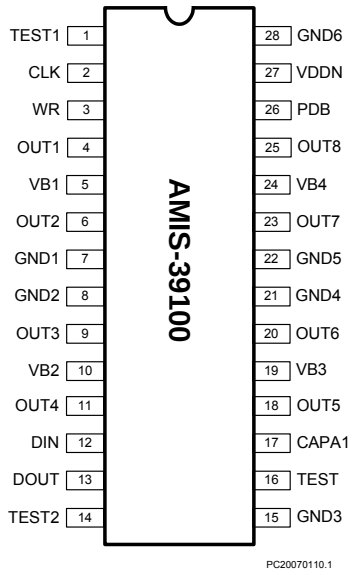

Figure 3: Pin Description of the AMIS-39100

Table 2: Pin Out

Pin	Name	Description
1	TEST1	Connect to GND
2	CLK	Schmitt trigger SPI CLK input
3	WR	Schmitt trigger SPI write enable input
4	OUT1	HS driver output
5	VB1	Battery supply
6	OUT2	HS driver output
7	GND1	Power ground and thermal dissipation path junction-to-PCB
8	GND2	Power ground and thermal dissipation path junction-to-PCB
9	OUT3	HS driver output
10	VB2	Battery supply
11	OUT4	HS driver output
12	DIN	SPI input pin (Schmitt trigger or CMOS inverter)
13	DOUT	Digital three state output for SPI
14	TEST2	Connect to GND
15	GND3	Power ground and thermal dissipation path junction-to-PCB
16	TEST	Connect to GND
17	CAPA1	Charge pump capacitor pin
18	OUT5	HS driver output
19	VB3	Battery supply
20	OUT6	HS driver output
21	GND4	Power ground and thermal dissipation path junction-to-PCB
22	GND5	Power ground and thermal dissipation path junction-to-PCB
23	OUT7	HS driver output
24	VB4	Battery supply
25	OUT8	HS driver output
26	PDB	Schmitt trigger power-down input
27	VDDN	Digital supply
28	GND6	Power ground and thermal dissipation path junction-to-PCB

8.0 Electrical and Environmental Ratings

8.1 Absolute Maximum Ratings

Stress levels above those listed in this paragraph may cause immediate and permanent device failure. It is not recommended that more than one of these conditions be applied simultaneously.

Table 3: Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VDDN	Power supply voltage	GND - 0.3	6	V
VB	DC battery supply on pins VB1 to VB4 load dump, Pulse 5b 400ms	GND - 0.3	35	V
Iout_ON	Maximum output current OUTx pins(1) The HS driver is switched on	-3000	350	mA
Iout_OFF	Maximum output current OUTx pins(1) The HS driver is switched off	-350	350	mA
I_OUT_VB	Maximum output current VB1, 2, 3, 4 pins	-700	3750	mA
Vcapa1	DC voltage on pins capa1	0	VB+16.5	V
Vdig_in	Voltage on digital inputs CLK, PDB, WR, DIN	-0.3	VDDN+0.3	V
V_{ESD}	Pins that connect the application (pins VB1..4 and Out1..8)(2) All other pins(2)	-4 -2	+4 +2	kV kV
V_{ESD}	ESD according charged device model(3)	-750	+750	V
Tj	Junction temperature (T<100 hours)	-40	175	°C
Tmr	Ambient temperature under bias	-40	105	°C

Notes:

(1) The power dissipation of the chip must be limited not to exceed the maximum junction temperature Tj.
(2) According to HBM standard MIL-STD-883 method 3015.7
(3) According to norm EOS/ESD-STM5.3.1-1999 robotic mode

8.2 Thermal Characteristics

Table 4: Thermal Characteristics of the Package

Symbol	Description	Conditions	Value	Unit
$R_{th(vj-a)}$	Thermal resistance from junction to ambient in power-SO28 package	In free air	145	K/W

Table 5: Thermal Characteristics of the AMIS-39100 on a PCB

PCB Design	Conductivity Top and Bottom Layer	R_{thja} (1)	Unit
Two layer (35um)	Copper planes according to Figure 4 + 25% copper for the remaining areas	24	K/W
Two layer (35um)	Copper planes according to Figure 4 + 0% copper for the remaining areas	53	K/W
Four layer JEDEC: EIA/JESD51-7	25% copper coverage	25	K/W
One layer JEDEC: EIA/JESD51-3	25% copper coverage	46	K/W

Note:

(1) These values are informative only.
R_{thja} = Thermal resistance from junction to ambient

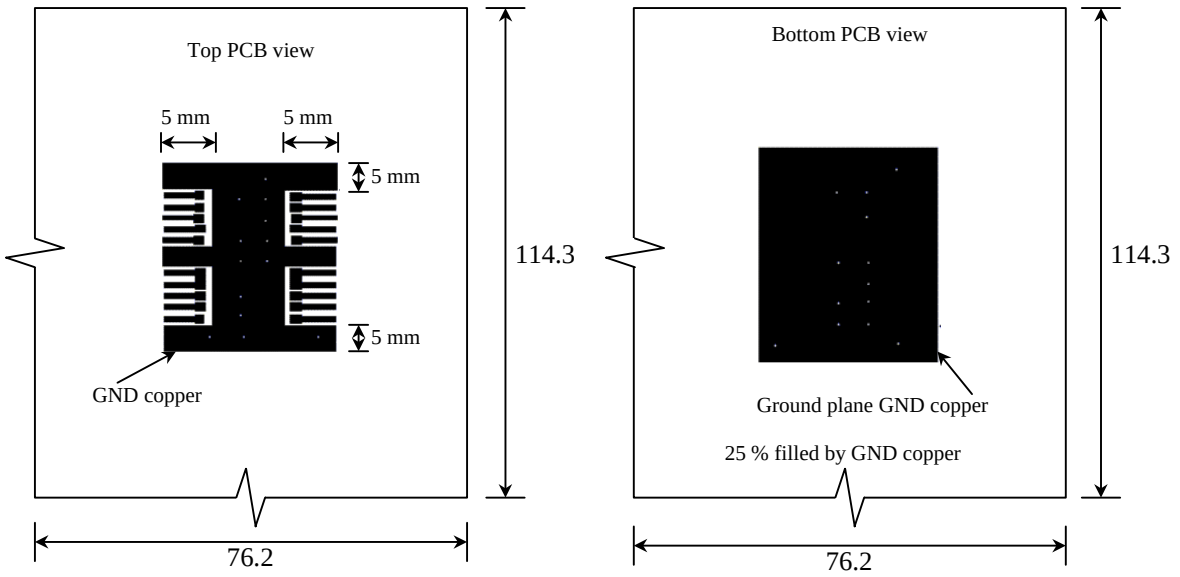

Figure 4: Layout Recommendation for Thermal Characteristics

8.3 Electrical Parameters

Operation outside the operating ranges for extended periods may affect device reliability. Total cumulative dwell time above the maximum operating rating for the power supply or temperature must be less than 100 hours.

The parameters below are independent from load type (see Section 8.4).

8.3.1. Operating Ranges

Table 6: Operating Ranges

Symbol	Description	Min.	Max.	Unit
VDDN	Digital power supply voltage	3.1	5.5	V
Vdig_in	Voltage on digital inputs CLK, PDB, WR, DIN	-0.3	VDDN	V
VB (1)	DC battery supply on Pins VB1 to VB4	3.5	16	V
Tamb	Ambient temperature	-40	105	°C

Notes:

(1) The power dissipation of the chip must be limited not to exceed maximum junction temperature Tj of 130°C.

8.3.2. Electrical Characteristics

Table 7: Electrical Characteristics

Symbol	Description	Min.	Max.	Unit
I_VB_norm(1)	Consumption on VB without load currents In normal mode of operation PDB = high		3.5	mA
I_PDB_3.3(1)(2)	Sum of VB and VDDN consumption in power down mode of operation PDB = low, VDDN 3.3V, VB = 12V, 23°C ambient CLK and WR are at VDDN voltage		25	µA
I_PDB_5(1)(2)	Sum of VB and VDDN consumption in power down mode of operation PDB = low, VDDN 5V, VB = 24V, 23°C ambient CLK and WR are at VDDN voltage		40	µA
I_PDB_MAX_VB	VB consumption in power down mode of operation PDB = low, VB = 16V		10	µA
I_VDDN_norm(1)	Consumption on VDDN In normal mode of operation PDB = high CLK is 500kHz, VDDN = 5.5V, VB = 16V		1.6	mA
R_on_1..8	On resistance of the output drivers 1 through 8 Vb= 16V (normal battery conditions and Tamb = 25°C) Vb = 4.6V (worst case battery condition and Tamb = 25°C)		 1 3	 Ω Ω
I_OUT_lim_x(1)	Internal over-current limitation of HS driver outputs	0.65	2	A
T_shortGND_HSdoff	The time from short of HS driver OUTx pin to GND and the driver de-activation; driver is Off. Detection works from VB minimum of 7V VDDN minimum is 3V	5,4		µs
TSD_H (1)	High TSD threshold for junction temperature (temperature rising)	130	170	°C
TSD_HYST	TSD hysteresis for junction temperature	9	18	°C

Notes:

(1) The power dissipation of the chip must be limited not to exceed maximum junction temperature Tj.

(2) The cumulative operation time mentioned above may cause permanent device failure.

8.4 Load Specific Parameters

HS driver parameters for specific loads are specified in following categories:

A. Parameters for inductive loads up to 350mH and $T_{ambient}$ up to 105°C
B. Parameters for inductive loads up to 300mH and $T_{ambient}$ up to 105°C
C. Parameters for resistive loads and $T_{ambient}$ up to 85°C

Table 8: Load Specific Characteristics

A. Inductive Load up to 350mH and $T_{ambient}$ up to 105°C				
Symbol	**Description**	**Min.**	**Max.**	**Unit**
I_OUT_ON_max.	Maximum output per HS driver, all eight drivers might be active simultaneously		240	mA
B. Inductive Load up to 300mH and $T_{ambient}$ up to 105°C				
I_OUT_ON_max.	Maximum output per HS driver, all eight drivers might be active simultaneously		275	mA
C. Resistive Load and $T_{ambient}$ up to 85°C				
I_OUT_ON_max.	Maximum output per HS driver, all eight drivers might be active simultaneously		350	mA
	Maximum output per one HS driver, only one can be active		650	mA
	Maximum output per HS driver, only two HS drivers from a different pair can be active simultaneously		500	mA
	Maximum output per one HS driver pair		830	mA

Note: The parameters above are not tested in production but are guaranteed by design.The overall current capability limitations need to be respected at all times.

The maximum current specified in Table 8 cannot always be obtained. The practically obtainable maximum drive current heavily depends on the thermal design of the application PCB (see Section 8.2).
The available power in the package is: (TSD_H - T_ambient) / R_{thja}
With TSD_H = 130°C and R_{thja} according to Table 5.

8.5 Charge Pump

The HS drivers use floating NDMOS transistors as power devices. To provide the gate voltages for the NDMOS of the HS drivers, a charge pump is integrated. The storage capacitor is an external one. The charge pump oscillator has typical frequency of 4MHz.

8.6 Diagnostics

8.6.1. Short-Circuit Diagnostics

The diagnostic circuit in the AMIS-39100 monitors the actual output status at the pins of the device and stores the result in the diagnostic register, which is then latched in the output register at the rising edge of the WR-pin. Each driver has its corresponding diagnostic bit DIAG_x. By comparing the actual output status (DIAG_x) with the requested driver status (CMD_x) you can diagnose the correct operation of the application according to Table 9.

8.6.2. Thermal Shutdown (TSD) Diagnostic

In case of TSD activation, all bits DIAG 1 to DIAG 8 in the SPI output register are set into the fault state and all drivers will be switched off (see Table 9). The TSD error condition is active until it is reset by the next correct communication on SPI interface (i.e. number of clock pulses during WR=0 is divisible by 8), provided that the device has cooled down under the TSD trip point.

Table 9: OUT Diagnostics

Requested driver status	CMD_x	Actual output status	DIAG_x	Diagnosis
On	1	High	1	Normal state
On	1	Low	0	Short to ground or TSD(2)
Off	0	High	1	Short to VB or missing load(1) or TSD(2)
Off	0	Low	0	Normal state(1)

Note:
(1) The correct diagnostic information is available after T_diagnostic_OFF time.
(2) All 8 diagnostic bits DIAG_x must be in the fault condition to conclude a TSD diagnostic.

8.6.3. Ground Loss

Due to its design, the AMIS-39100 is protected for withstanding module ground loss and driver output shorted to ground at the same time.

8.6.4. Power Loss

Table 10: Power Loss

VDDN	VB	Possible Case	Action
0	0	System stopped	Nothing
0	1	Start case or sleeping mode with missing VDDN	Eight switches in the off-state Power down consumption on VB
1	0	Missing VB supply VDDN normally present	Eight switches in the off-state Normal consumption on VDDN
1	1	System functional	Nominal functionality

8.7 SPI Interface

The serial peripheral interface (SPI) is used to allow an external microcontroller (MCU) to communicate with the device. The AMIS-39100 acts always as a slave and it can't initiate any transmission.

8.7.1. SPI Transfer Format and Pin Signals

The SPI block diagram and timing characteristics are shown in Figure 6 and Figure 7.

During an SPI transfer, data is simultaneously sent to and received from the device. A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DIN and DOUT). DOUT signal is the output from the AMIS-39100 to the external MCU and DIN signal is the input from the MCU to the AMIS-39100. The WR-pin selects the AMIS-39100 for communication and can also be used as a chip select (CS) in a multiple-slave system. The WR-pin is active low. If AMIS-39100 is not selected, DOUT is in high impedance state and it does not interfere with SPI bus activities. Since AMIS-39100 always shifts data out on the rising edge and samples the input data also on the rising edge of the CLK signal, the MCU SPI port must be configured to match this operation. SPI clock idles high between the transferred bytes.

The diagram in Figure 7 represents the SPI timing diagram for 8-bit communication. Communication starts with a falling edge on the WR-pin that latches the status of the diagnostic register into the SPI output register. Subsequently, the CMD_x bits – representing the newly requested driver status – are shifted into the input register and simultaneously, the DIAG_x bits – representing the actual output status – are shifted out. The bits are shifted with x=1 first and ending with x=8. At the rising edge of the WR-pin, the data in the input register is latched into the command register and all drivers are simultaneously switching to the newly requested status. SPI communication is ended.

In case the SPI master does only support 16-bit communication, then the master must first send 8 clock pulses with dummy DIN data and ignoring the DOUT data. For the next 8 clock pulses the above description can be applied.

The required timing for serial to peripheral interface is shown in Table 11.

Table 11: Digital Characteristics

Symbol	Description	Min.	Max.	Unit
T_CLK	Maximum applied clock frequency on CLK input		500	kHz
T_DATA_ready	Time between falling edge on WR and first bit of data ready on DOUT output (driver going from HZ state to output of first diagnostic bit)		2	µs
T_CLK_first	First clock edge from falling edge on WR	3		µs
T_setup(1)	Set-up time on DIN	20		ns
T_hold(1)	Hold time on DIN	20		ns
T_DATA_next	Time between rising edge on CLK and next bit ready on DOUT (capa (capacitor tied to the DOUT pin is 30pF max.)		100	ns
T_SPI_END	Time between last CLK edge and WR rising edge	1		µs
T_risefall	Rise and fall time of all applied signals (maximum loading capacitance is 30pF)	5	20	ns
T_WR	Time between two rising edge on WR (repetition of the same command)	300		µs

Note: (1) Guaranteed by design

Normal mode verification:

- The *command* is the set of eight bits loaded via SPI, which drives the eight HS drivers on or off.
- The *command* is activated with rising edge on WR pin.

Table 12: Digital Characteristics

Symbol	Description	Min.	Max.	Unit
T_command_L_max.(1)	Minimum time between two opposite commands for inductive loads and maximum HS driver current of 275mA	1		s
T_command_R(1)	Minimum time between two opposite commands for resistive loads and maximum HS driver current of 350mA	2		ms
T_PDB_recov	The time between the rising edge on the PDB input and 90 percent of VB- 1V on all HS driver outputs. (all drivers are activated, pure resistive load 35mA on all outputs)		1	ms

Note: (1) Guaranteed by design

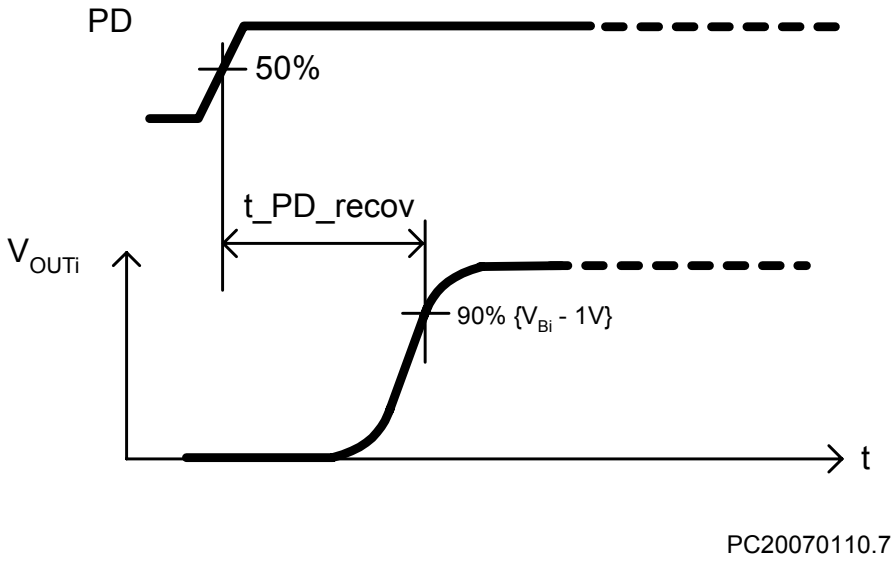

Figure 5: Timing for Power-down Recovery

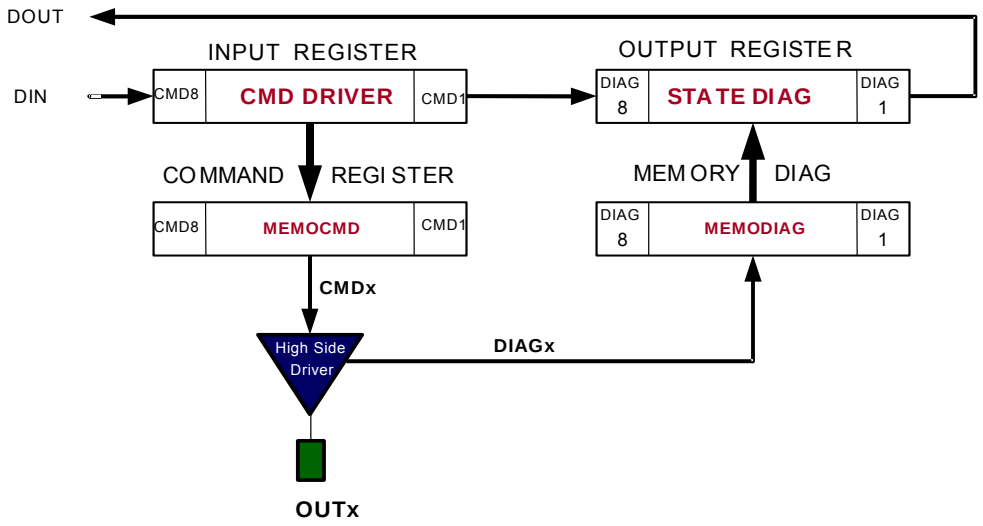

Figure 6: SPI Block Diagram

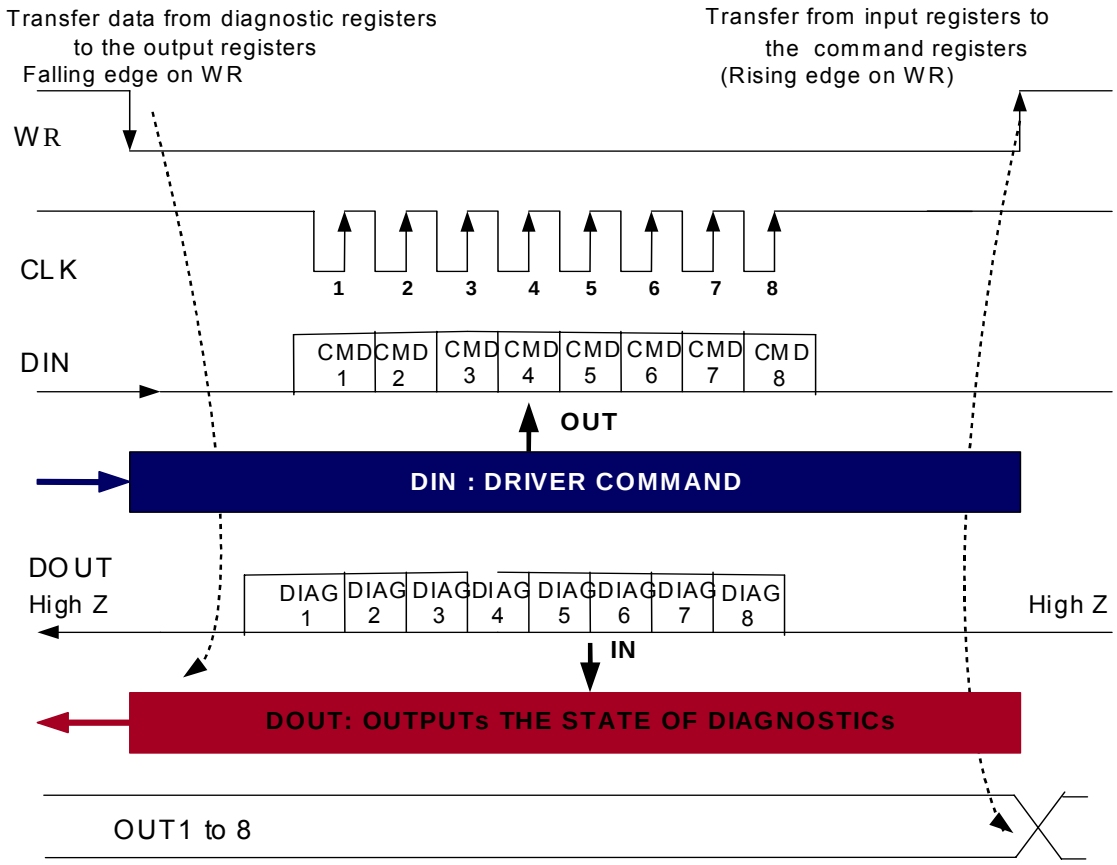

Figure 7: Timing Diagram

9.0 Assembly and Delivery

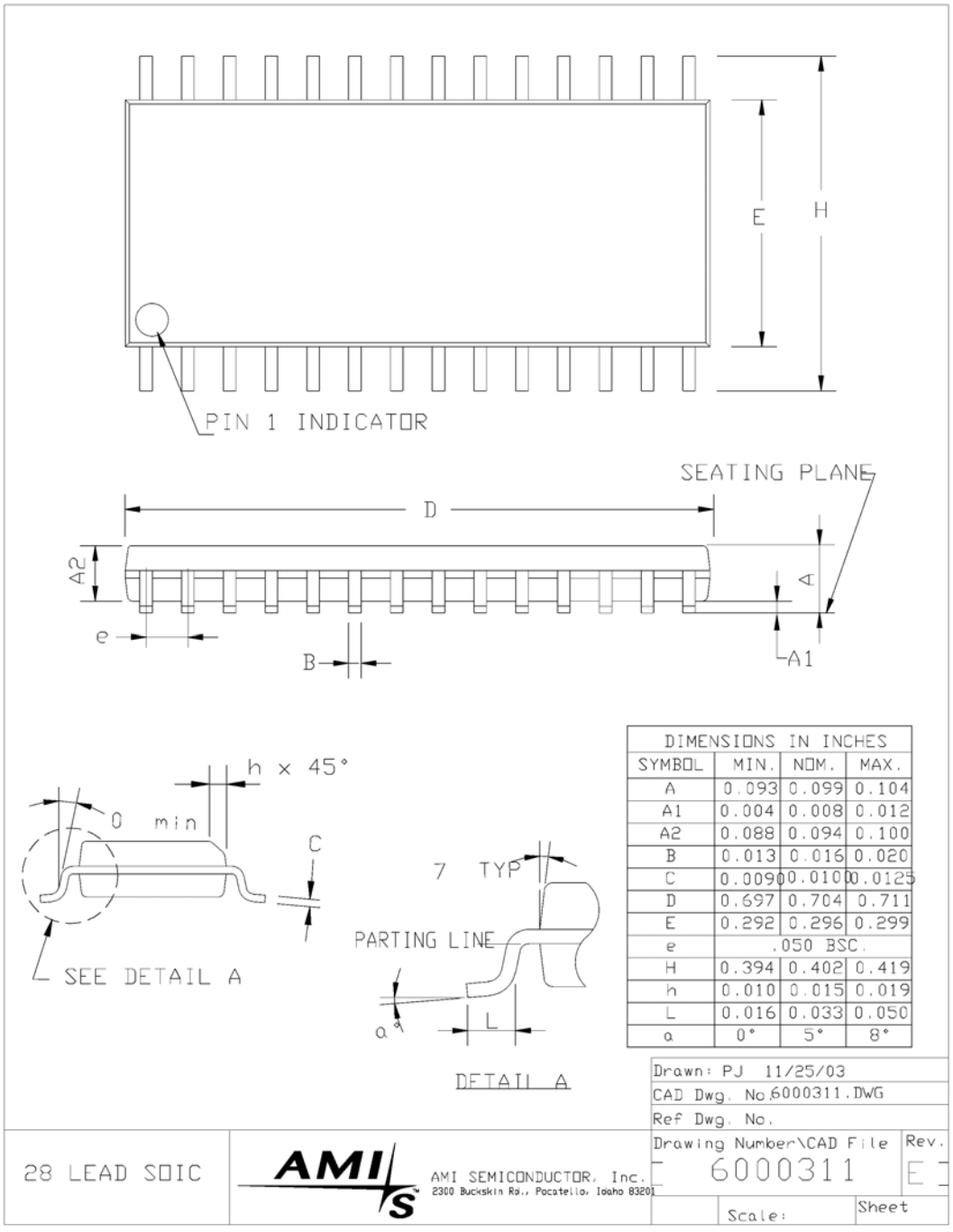

Figure 8: Package Outline Drawing

10.0 Soldering

10.1 Introduction to Soldering Surface Mount Packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in the AMIS "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011). There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

10.2 Re-flow Soldering

Re-flow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement. Several methods exist for re-flowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method. Typical re-flow peak temperatures range from 215 to 260°C.

10.3 Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems. To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
    - Larger than or equal to 1.27mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the print-circuit board;
    - Smaller than 1.27mm, the footprint longitudinal axis must be parallel to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Typical dwell time is four seconds at 250°C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C.

When using a dedicated tool, all other leads can be soldered in one operation within two to five seconds between 270 and 320°C.

Table 13: Soldering Process

Package	Soldering Method	
	Wave	Re-flow (1)
BGA, SQFP	Not suitable	Suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	Not suitable (2)	Suitable
PLCC (3), SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (3)(4)	Suitable
SSOP, TSSOP, VSO	Not recommended (5)	Suitable

Notes:

1. All SMD packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the dry pack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8mm; it is definitely not suitable for packages with a pitch (e) equal or smaller than 0.65mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5mm.

11.0 Revision History

Table 14: Revision History

Revision	Date	Description
0.1	Various	Initial document
0.2	June 2006	Document formatted into new AMIS template
0.3	January 2007	Update of some values in Tables 1, 2, 3, 6 and 7. Update of explanation in paragraph 8.6: Diagnostics, and paragraph 8.7: SPI Interface. Update of Figure 8 Added section 10.0: Soldering

12.0 Company or Product Inquiries

For more information about AMI Semiconductor, our technologies and our products, visit our Web site at: http://www.amis.com