ORIENT DISPLAY

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SPECIFICATION
FOR
LCD MODULE

MODULE NO: AMG160160P1-G-W6WFDW
VERSION NO.: V02

Customer's Approval:

	SIGNATURE	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

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DOCUMENT REVISION HISTORY

Version	DATE	DESCRIPTION	CHANGED BY
00	Nov-12-2009	First issue	Chen
01	Jul-15-2014	Update the file format	XQ Liu
02	Jul-22-2014	Update the DIMENSIONAL OUTLINE	XQ Liu

CONTENTS

1. FUNCTIONS & FEATURES

1.1. Format	: 160*160 Dots
1.2. LCD mode	: FSTN /Positive Mode /Transflective
1.3. Viewing direction	: 6 o'clock
1.4. Driving scheme	: 1/160 Duty cycle, 1/12 Bias
1.5. Power supply voltage (V_{DD})	: 3.3V
1.6. LCD driving voltage (VLCD)	: 15.6V (Reference voltage)
1.7. Operation temp	: -20~+70℃
1.8. Storage temp	: -30~+80℃
1.9. Back light	: Edge white
1.10. RoHS compliant.	

2. MECHANICAL SPECIFICATIONS

2.1. Module size	: 70.0mm(L)*76.5mm+23.1mm(FPC length)mm(W)*5.1mm(H)
2.2. Viewing area	: 63.4mm(L)*63.3mm(W)
2.3. Active area	: 55.985mm(L)*55.985mm(W)
2.4. Dot pitch	: 0.35mm(L)*0.35mm(W)
2.5. Dot size	: 0.335mm(L)*0.335mm(W)
2.6. Weight	: Approx.

3. BLOCK DIAGRAM

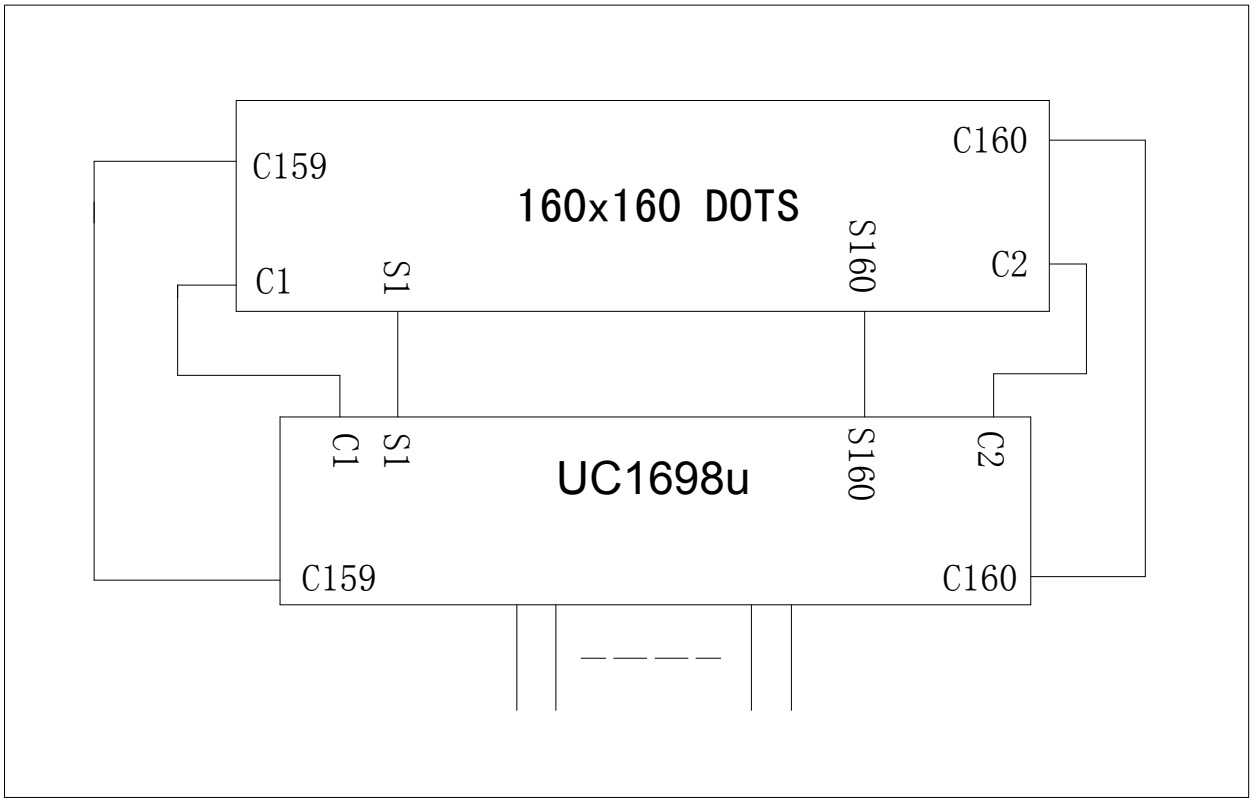
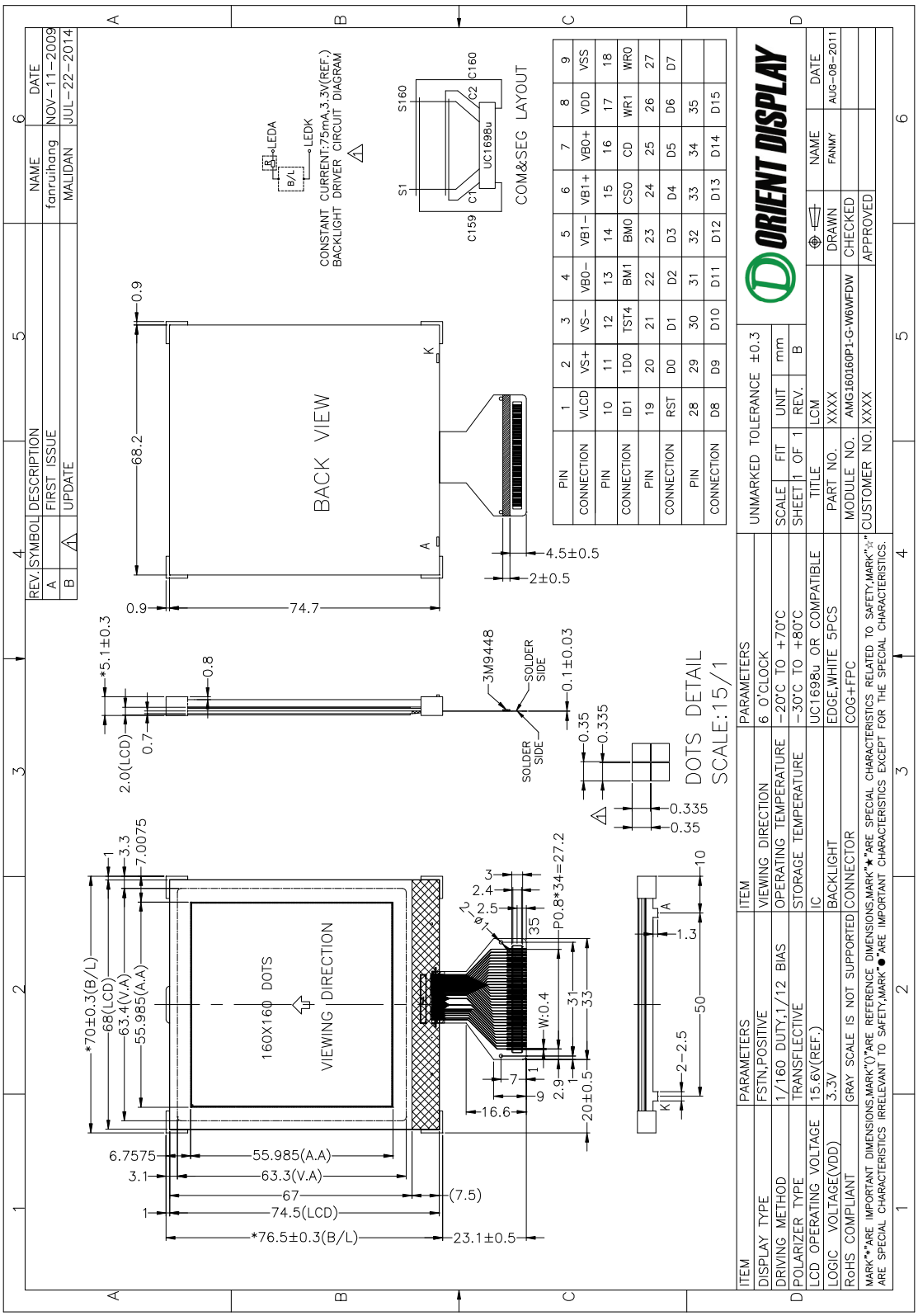


Figure 1. Block diagram

4. DIMENSIONAL OUTLINE



PIN	1	2	3	4	5	6	7	8	9
CONNECTION	VLCD	VS+	VS−	VB0−	VB1−	VB1+	VB0+	VDD	VSS
PIN	10	11	12	13	14	15	16	17	18
CONNECTION	ID1	ID0	TST4	BM1	BM0	CS0	CD	WR1	WR0
PIN	19	20	21	22	23	24	25	26	27
CONNECTION	RST	D0	D1	D2	D3	D4	D5	D6	D7
PIN	28	29	30	31	32	33	34	35	
CONNECTION	D8	D9	D10	D11	D12	D13	D14	D15	

REV.	SYMBOL	DESCRIPTION	NAME	DATE
A		FIRST ISSUE	fanruihang	NOV-11-2009
B	△	UPDATE	MALIDAN	JUL-22-2014

ITEM	PARAMETERS
DISPLAY TYPE	FSTN,POSITIVE
DRIVING METHOD	1/160 DUTY,1/12 BIAS
POLARIZER TYPE	TRANSFLECTIVE
LCD OPERATING VOLTAGE	15.6V(REF.)
LOGIC VOLTAGE(VDD)	3.3V
RoHS COMPLIANT	GRAY SCALE IS NOT SUPPORTED

ITEM	PARAMETERS
VIEWING DIRECTION	6 O'CLOCK
OPERATING TEMPERATURE	-20°C TO +70°C
STORAGE TEMPERATURE	-30°C TO +80°C
IC	UC1698u OR COMPATIBLE
BACKLIGHT	EDGE,WHITE 5PCS
CONNECTOR	COG+FPC

MARK"★"ARE IMPORTANT DIMENSIONS,MARK"()"ARE REFERENCE DIMENSIONS,MARK"★"ARE SPECIAL CHARACTERISTICS RELATED TO SAFETY,MARK"☆"ARE SPECIAL CHARACTERISTICS IRRELEVANT TO SAFETY,MARK"●"ARE IMPORTANT CHARACTERISTICS EXCEPT FOR THE SPECIAL CHARACTERISTICS.

Figure 2. Dimensional outline

5. PIN DESCRIPTION

<table>
<tr><td>1</td><td>VLCD</td><td>Power supply for LCD voltage</td></tr>
<tr><td>2~7</td><td>VS+, VS-,
VB0-, VB1-,
VB1+, VB0+</td><td>LCD SEG driving voltages.</td></tr>
<tr><td>8</td><td>VDD</td><td>Power supply for logic(+3.3V)</td></tr>
<tr><td>9</td><td>VSS</td><td>Ground</td></tr>
<tr><td>10</td><td>ID1</td><td>Selects Input Data set for 8-bit mode.
ID1=0 : 8-bit input data are D[0,2,4,6,8,10,12,14]
ID1=1 : 8-bit input data are D[0:7]
The wiring status of ID pins is available in PID[1:0] with command Get Status. Other than 8-bit mode, connect ID1 to V_{DD} for “H”, or V_{SS} for “L”.</td></tr>
<tr><td>11</td><td>ID0</td><td>ID0 pin can be used for production control.
Connect ID0 pin to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>12</td><td>TST4</td><td>Test control. This pin has on-chip pull-up resistor. Leave it open during normal operation.
TST4 is also used as one of the high voltage power supply for MTP programming operation. For COG designs, please wire out TST4 with trace resistance between 30~50 Ω.</td></tr>
<tr><td>13,14</td><td>BM1, BM0</td><td>Bus mode: The interface bus mode is determined by BM[1:0] and {DB15, DB13} by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>{DB15, DB13}</th><th>Mode</th></tr>
<tr><td>11</td><td>Data</td><td>6800/16-bit</td></tr>
<tr><td>10</td><td>Data</td><td>8080/16-bit</td></tr>
<tr><td>01</td><td>0x</td><td>6800/8-bit</td></tr>
<tr><td>00</td><td>0x</td><td>8080/8-bit</td></tr>
<tr><td>00</td><td>10</td><td>4-wire SPI w/ 8-bit token
(S8: conventional)</td></tr>
<tr><td>00</td><td>11</td><td>3/4-wire SPI w/ 8-bit token
(S8uc: Ultra-Compact)</td></tr>
<tr><td>01</td><td>10</td><td>3-wire SPI w/ 9-bit taken
(S9: conventional)</td></tr>
</table></td></tr>
<tr><td>15</td><td>CS0</td><td>Chip select signal</td></tr>
<tr><td>16</td><td>CD</td><td>Selects Control data or Display data for read/write operation. In S9 mode, CD pin is not used. Connect to V_{SS} when not used.
”L”: Control data ”H”: Display data</td></tr>
</table>

<table>
<tr><td>17,18</td><td>WR1 ,WR0</td><td>WR[1:0] control the read/write operation of the host interface. See section Host Interface for more detail.
In parallel mode, the meaning of WR[1:0] depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
<tr><td>19</td><td>RST</td><td>The RESET signal</td></tr>
<tr><td>20~35</td><td>D0~D15</td><td>Bi-directional bus for parallel host interfaces.
In serial modes, connect DB[0] to SCK, DB[8] to SDA.
<table>
<tr><th></th><th>BM=1x
(16-bit)</th><th>BM=0x
(8-bit)
ID1=0</th><th>BM=0x
(8-bit)
ID1=1</th><th>BM=00
(S8/S8uc)</th><th>BM=01
(S9)</th></tr>
<tr><td>DB0</td><td>D0</td><td>D0/D8</td><td>D0/D8</td><td>SCK</td><td>SCK</td></tr>
<tr><td>DB1</td><td>D1</td><td>–</td><td>D1/D9</td><td>–</td><td>–</td></tr>
<tr><td>DB2</td><td>D2</td><td>D1/D9</td><td>D2/D10</td><td>–</td><td>–</td></tr>
<tr><td>DB3</td><td>D3</td><td>–</td><td>D3/D11</td><td>–</td><td>–</td></tr>
<tr><td>DB4</td><td>D4</td><td>D2/D10</td><td>D4/D12</td><td>–</td><td>–</td></tr>
<tr><td>DB5</td><td>D5</td><td>–</td><td>D5/D13</td><td>–</td><td>–</td></tr>
<tr><td>DB6</td><td>D6</td><td>D3/D11</td><td>D6/D14</td><td>–</td><td>–</td></tr>
<tr><td>DB7</td><td>D7</td><td>–</td><td>D7/D15</td><td>–</td><td>–</td></tr>
<tr><td>DB8</td><td>D8</td><td>D4/D12</td><td>–</td><td>SDA</td><td>SDA</td></tr>
<tr><td>DB9</td><td>D9</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB10</td><td>D10</td><td>D5/D13</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB11</td><td>D11</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB12</td><td>D12</td><td>D6/D14</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB13</td><td>D13</td><td>–</td><td>–</td><td>0:S8/1:S8uc</td><td>0</td></tr>
<tr><td>DB14</td><td>D14</td><td>D7/D15</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB15</td><td>D15</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
</table>
Always connect unused pins to either V_{SS} or V_{DD}.</td></tr>
</table>

6. MAXIMUM ABSOLUTE LIMIT

Item	Symbol	MIN	MAX	Unit
Supply Voltage for Logic	V_{DD}	-0.3	4.0	V
Supply Voltage for LCD	---	-0.3	19.8	V
Input Voltage	Vin	-0.4	V_{DD}+0.5	V
Supply Current for Backlight	I_F(Ta = 25°C)	---	90	mA
Reverse Voltage for Backlight	V_R(Ta = 25°C)	---	0.8	V
Operating Temperature	Top	-20	70	℃
Storage Temperature	Tst	-30	80	℃

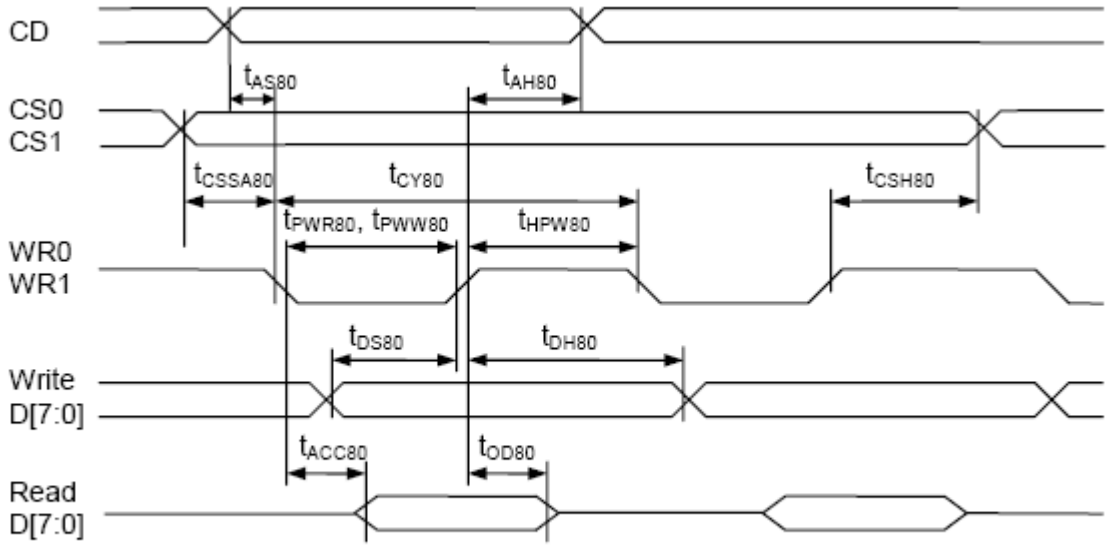
7. ELECTRICAL CHARACTERISTICS

DC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65		3.465	V
$V_{DD2/3}$	Supply for bias & pump		2.7		3.465	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ = 2.8V, 25°C		15.2	18	V
V_D	LCD data voltage	$V_{DD2/3}$ = 2.8V, 25°C	1.09		1.95	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
I_{SB}	Standby current	V_{DD} = $V_{DD2/3}$ = 3.3V, Temp = 85°C			50	μA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 16.5V		850	1100	Ω
$R_{ON(COM)}$	COM output impedance	V_{LCD} = 16.5V		950	1100	Ω
f_{LINE}	Average line rate	LC[4:3] = 10b, 25°C	-10%	37.0	+10%	Klps

8. TIMING CHARACTERISTICS

1)8080 TIMING

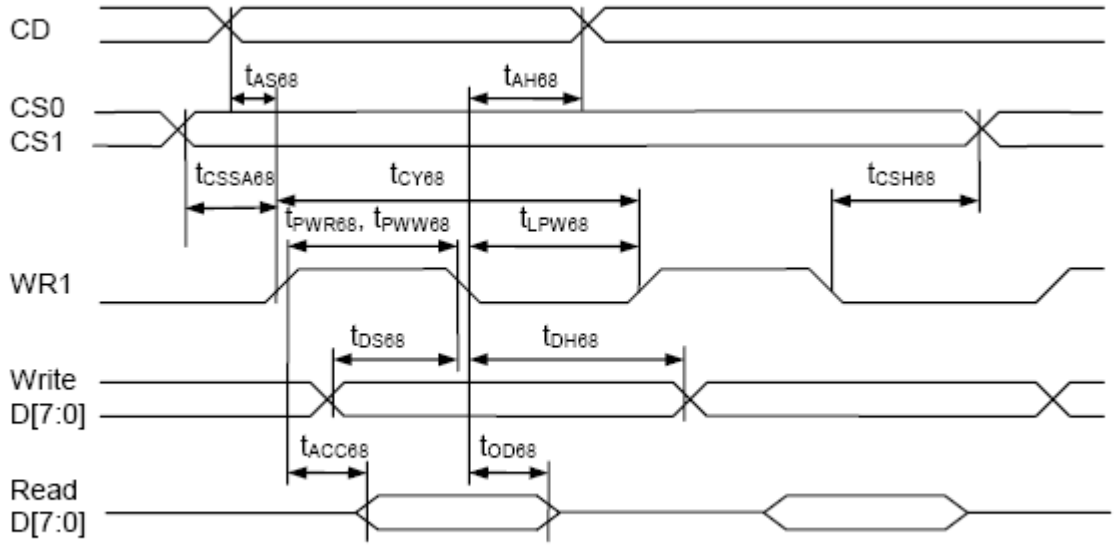


Parallel Bus Timing Characteristics (for 8080 MCU)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 170 130 100 80 90	–	nS
t_{PWR80}	WR1	Pulse width 16-bit (read) 8-bit		85 50	–	nS
t_{PWW80}	WR0	Pulse width 16-bit (write) 8-bit	 LC[7:6]=10b LC[7:6]=01b	65 40 45	–	nS
t_{HPW80}	WR0, WR1	High pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 85 65 50 40 45	–	nS
t_{DS80} t_{DH80}	D0~D15	Data setup time Data hold time		30 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
T_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		5 5		nS

2)6800 TIMING

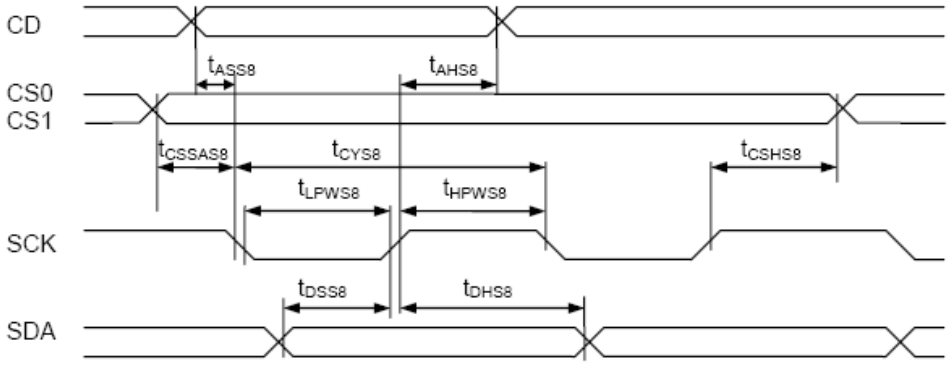


Parallel Bus Timing Characteristics (for 6800 MCU)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 170 130 100 80 90	–	nS
t_{PWR68}	WR1	Pulse width 16-bit (read) 8-bit		85 50	–	nS
t_{PWW68}		Pulse width 16-bit (write) 8-bit	 LC[7:6]=10b LC[7:6]=01b	65 40 45	–	nS
t_{LPW68}		Low pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 85 65 50 40 45	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		5 5		nS

3)S8 TIMING

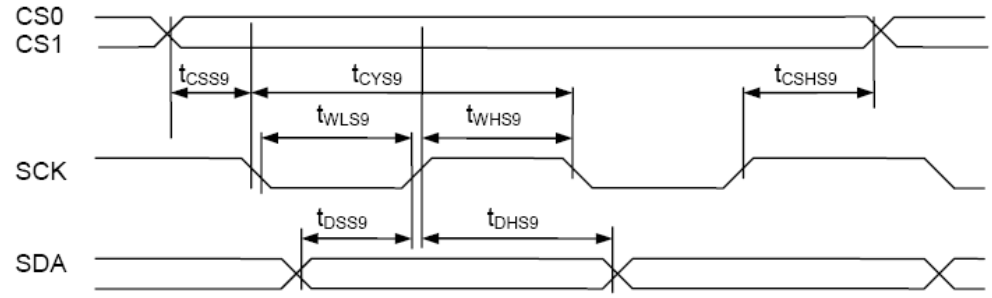


Serial Bus Timing Characteristics (for S8/S8uc)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		40	–	nS
t_{LPWS8}		Low pulse width		20	–	nS
t_{HPWS8}		High pulse width		20	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		15 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		5 5		nS

4)S9 TIMING

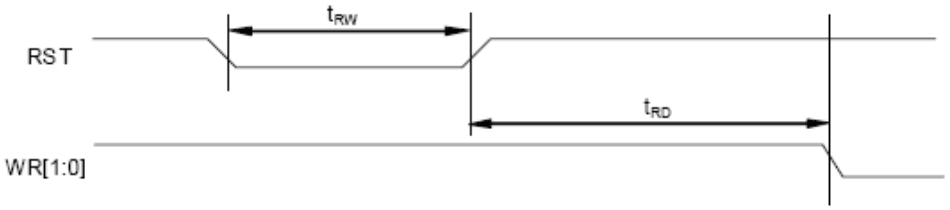


Serial Bus Timing Characteristics (for S9)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		40	–	nS
t_{LPWS9}		Low pulse width		20	–	nS
t_{HPWS9}		High pulse width		20	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		15 0	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS

5)RESET TIMING



Reset Characteristics

(1.65V ≤ V_{DD} < 3.3V, Ta= −30to+85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	μS
t_{RD}	RST, WR	Reset to WR pulse delay		10	–	mS

9. CONTROL AND DISPLAY COMMAND

The following is a list of host commands supported by UC1698u

C/D: 0: Control, 1: Data

W/R: 0: Write Cycle, 1: Read Cycle

#: Useful Data bits –: Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A
				Ver	PMO[6:0]								
				Product Code (8h)				PID[1:0]		MID[1:0]			
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Adv. Program Control	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0 or 1	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0
10	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	40H
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	0
		0	0	#	#	#	#	#	#	#	#		
14	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
15	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
16	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
17	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
18	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
19	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[4:0]	1DH
				-	-	-	#	#	#	#	#		
20	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
21	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
22	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	159
		0	0	-	#	#	#	#	#	#	#		
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	159
		0	0	-	#	#	#	#	#	#	#		
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Shared with MTP commands: Set WPC0	0
		0	0	-	#	#	#	#	#	#	#		
31	Set Window Program Starting Row Address	0	0	1	1	1	1	0	1	0	1	Set WPP0	0
		0	0	#	#	#	#	#	#	#	#		
32	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1	127
		0	0	-	#	#	#	#	#	#	#		
33	Set Window Program Ending Row Address	0	0	1	1	1	1	0	1	1	1	Set WPP1	159
		0	0	#	#	#	#	#	#	#	#		
34	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Inside
35	Set MTP Operation control	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]	10H
		0	0	-	-	-	#	#	#	#	#		

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
36	Set MTP Write Mask	0 0 0	0 0 0	1 - -	0 # -	1 # -	1 # -	1 # -	0 # -	0 # #	1 # #	Set MTPM[6:0] MTPM1[1:0]		0
37	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
38	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	N/A
39	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	N/A
40	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	N/A

NOTE:

- All other bit patterns other than commands listed above may result in undefined behavior.
- The interpretation of commands (36)~(40) depends on the setting of register MTPC[3].
  - Commands (37)~(40) are shared with commands (30)~(33). These two sets of commands share exactly the same code and control registers. When MTPC[3]=0, they are interpreted as Window Program commands and registers. When MTPC[3]=1, they function as MTP Control commands and registers.
- After MTP ERASE or PROGRAM operation, before resuming normal operation, please always
  a) Remove TST4 power source,
  b) Do a full V_{DD} ON-OFF-ON cycle.
- Under 16-bit bus mode and CD=0, D[15:8] is ignored and only D[7:0] is used. As a result, the bus cycles for commands under 16-bit bus and 8-bit bus are the same, and double-byte commands still need two bus cycles under 16-bit bus mode.

  Example:

  8-bit bus mode:

  Set PL[1:0] = 2'b11 : D[7:0] = 0010 1011

  Set PM[7:0] = 8'h8b : 1st D[7:0] = 1000 0001

  2nd D[7:0] = 1000 1011

10. BACKLIGHT CHARACTERISTICS

Ta = 25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Voltage	Vf	IF=75mA	2.9	3.1	3.3	V
Reverse Current	Ir	VR=0.8V	---	15	---	mA
Luminous Intensity (Without LCD)	Lv	IF=75mA	---	550	---	cd/m^2
Module Luminance (With LCD OFF)	Lv	IF=75mA	---	80	---	cd/m^2
Chromaticity Coordinate	X/Y	IF=75mA	0.26—0.32 0.27—0.33			---
Color	White					

Note:

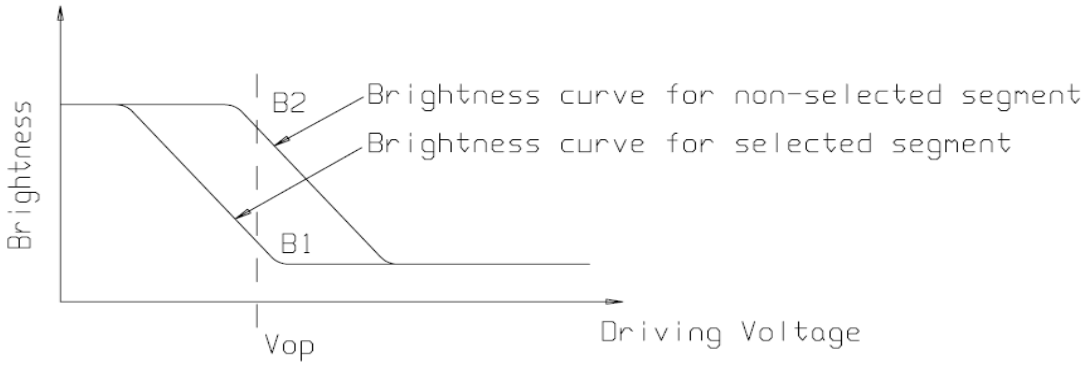
Note: when the temperature exceed 25℃, the approved current decrease rate for backlight change as the temperature increase is: -0.36x5mA/℃ based on the maximum absolute limiting current of the backlight,to make sure the backlight current<=min[75mA, 25*5-0.36*5*(Ta-25)mA] (below 25℃, the current refer to constant, which would not change with temperature).

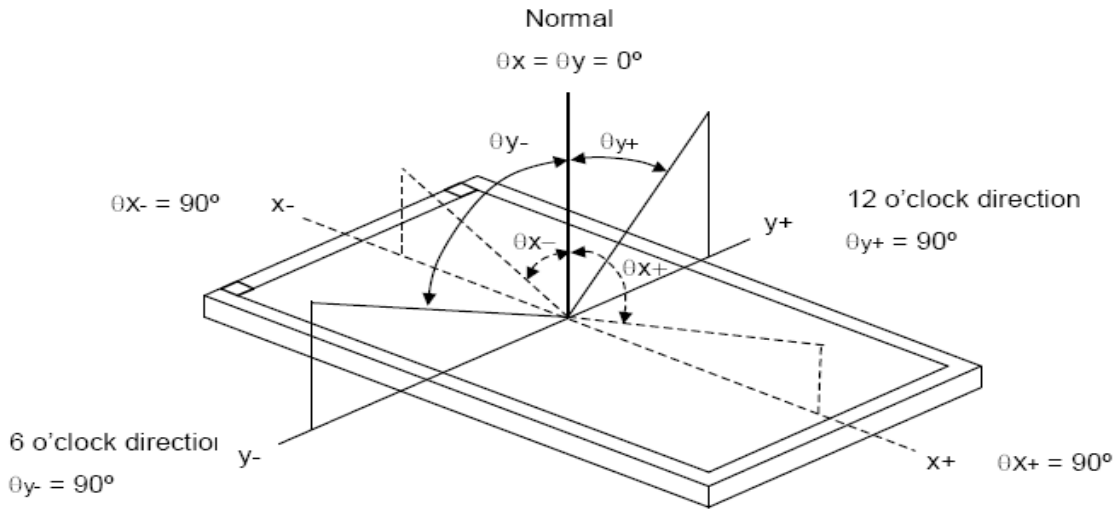
11. ELECTRO-OPTICAL CHARACTERISTICS

(Ta = 25°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	Vop	Ta = -20°C	---	---	---	V
		Ta = 25°C	15.4	15.6	15.8	
		Ta = 70°C	---	---	---	
Response time	Tr	Ta = 25°C	---	180	216	ms
	Tf		---	120	144	ms
Contrast	Cr	Ta = 25°C θx=θy=0	---	4.5	---	---
Viewing angle range	θx-	Cr≥2	30	35	---	deg
	θx+		30	35	---	deg
	θy-		35	40	---	deg
	θy+		35	40	---	deg

$$Cr = \frac{\text{Brightness of non-selected segment(B2)}}{\text{Brightness of selected segment(B1)}}$$





12. PRECAUTION FOR USING LCD/LCM

LCD/LCM is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification. The followings should be noted.

General Precautions:

1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isopropyl alcohol or ethyl alcohol, do not use water, ketone or aromatics and never scrub hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not made any modification on the PCB without consulting OD .
5. When mounting a LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and also cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal adheres to skin or clothes, wash it off immediately with soap and water.

Static Electricity Precautions:

1. CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.
3. Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.
4. The modules should be kept in anti-static bags or other containers resistant to static for storage.
5. Only properly grounded soldering irons should be used.
6. If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
7. The normal static prevention measures should be observed for work clothes and working benches.
8. Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

Soldering Precautions:

1. Soldering should be performed only on the I/O terminals.
2. Use soldering irons with proper grounding and no leakage.
3. Soldering temperature:300±5℃
4. Soldering time: 2 to 3 second.
5. Use eutectic solder with resin flux filling.
6. If flux is used, the LCD surface should be protected to avoid spattering flux.
7. Flux residue should be removed.

Operation Precautions:

1. The viewing angle can be adjusted by varying the LCD driving voltage Vo.
2. Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3. Driving voltage should be kept within specified range; excess voltage will shorten display life.
4. Response time increases with decrease in temperature.
5. Display color may be affected at temperatures above its operational range.
6. Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7. When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.For long-term storage,the temperature should be 0°C~40°C,and the relative humidity should be kept 40%~60%.

Limited Warranty

OD LCDs and modules are not consumer products, but may be incorporated by OD's customers into consumer products or components thereof, OD does not warrant that its LCDs and components are fit for any such particular purpose.

1. The liability of OD is limited to repair or replacement on the terms set forth below. OD will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between OD and the customer, OD will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with OD general LCD inspection standard . (Copies available on request)
2. No warranty can be granted if any of the precautions state in handling liquid crystal display above has been disregarded. Broken glass, scratches on polarizer mechanical damages as well as defects that are caused accelerated environment tests are excluded from warranty.
3. In returning the LCD/LCM, they must be properly packaged; there should be detailed description of the failures or defect.

13. LCM TEST CRITERIA(A1 LEVEL)

1. Objective

The LCM test criteria are set to formalize OD's LCM quality standards with reference to those of the customer for inspection, release and acceptance of finished LCM products in order to guarantee the quality required by the customer.

2. Scope

The criteria are applicable to all the LCM products manufactured by OD.

3. Equipments for Inspection

Electrical testing machines, vernier calipers, ampere meter, multi-meter, microscopes, anti-static wrist straps, finger cots, labels, tri-phase thermal shock chamber, constant temperature and humidity chamber, high-low temperature experimenting box, refrigerators, constant voltage power supply (DC）)) , desk Lamps, etc.

4. Sampling Plan and Reference Standards

4.1.1 Based on GB/T 2828.1---2003/ISO2859-1:1999：

Inspection items	Sampling Rate	AQL Assessment
Appearance	Normally checking the sampling plan one time and performing general inspection level II	MA=0.4 MI=1.0
Function	Normally checking the sampling plan one time and performing general inspection level II	MA=0.4 MI=1.0
Size	N=3	C=0

4.1.2 GB/T 2828.1---2003/ISO2859-1:1999 checking the counting sampling procedure and sampling table.

4.1.3 GB/T 1619.96: Test methods for TN LCD parts.

4.1.4 GB/T 12848.91: General Specification for STN LCD parts

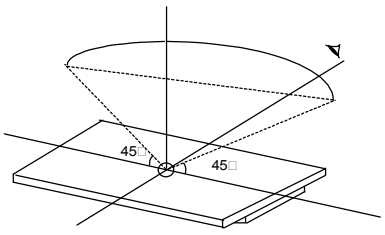
4.1.5 GB2421-89: Basic Environmental Test Procedures for Electrical and Electronic Products

4.1.6 IPC-A-610C: The acceptance condition for electrician assembled.

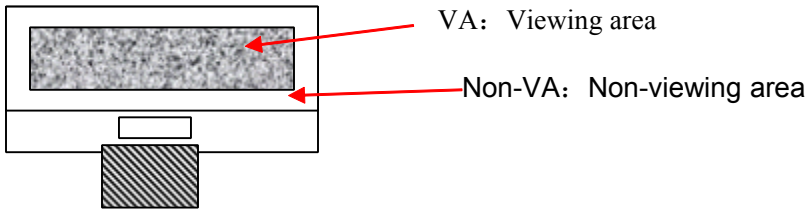
5. Inspection Conditions and Inspection Reference

5.1 Cosmetic inspection: shall be done normally at 25±5℃ of the ambient temperature and 45±20%RH of relative humidity, under the ambient luminance greater than 300luxand at the distance of 30cm apart between the inspector's eyes and the LCD panel and normally in reflected light. For back-lit LCMs, cosmetic inspection shall be done under the ambient luminance less than 100lux with the backlight on.

5.2 The LCM shall be tested at the angle of 45° both left side and right side, and 0-45° both top side and bottom side (for STN LCM, at 20°~55°):



5.3 Definition of VA



5.4 Inspection with naked eyes（exclusive of the inspection of the physical dimensions of defects carried out with magnifiers）.

5.5 Electrical properties: Inspection with the self-made/special LCM test jigs against the product documents or drawings; display contents and parameters shall conform to their documents requirements and the display effect to the drawing.

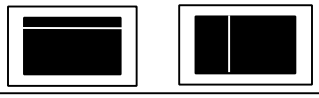
5.5.1 Test voltage（V）：(Determined) according to the operating instruction of test jigs assuming the external circuit can be adjusted unless the customer otherwise specifies driving voltage(s). (Display) effects are controlled within the specified range of voltage variation (If no specific requirements, display effects are controlled at Vop = 9V or Vop ±0.3V when Vop is below 9V; if Vop is above 9V, display effects are controlled at Vop ±3% at least).For display products with the customer-specified fixed Vop, display effects are controlled by adjusting the internal circuit; if necessary, acceptable limit samples shall be built.

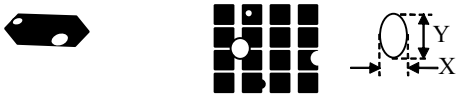
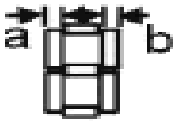
5.5.2 Current Consumption（I）：Refer to approved product specifications or drawings.

5.5.3 Size: for the outline dimension and the position which maybe affect customer assembled all should conform to the technical drawing requirements.

6. Defects and Acceptance Standards

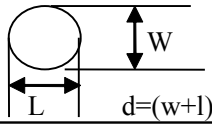
6.1 Electrical properties test

No.	Defects	Description	Accepted standard	MAJ	MIN
6.1.1	Missing segmet	SEG/COM dot and character missing segment caused by its wire broken/poor contact(s) and internal open circuit. 	Reject	√	
6.1.2	No display/	The products no picture display under normally	Reject	√	

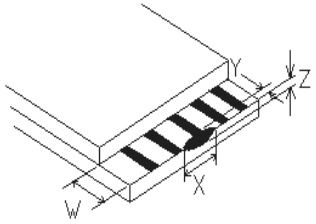
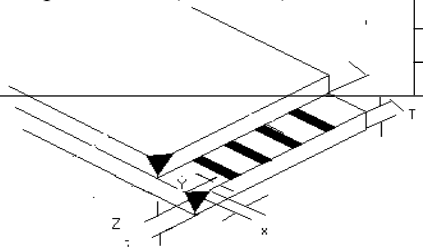
	reaction	connected situation.			
6.1.3	Mis-dispaly/ abnormaly display	Displaying pattern and sequence not conform to the requirement or abnormally display when scanning as per the correct procedure.	Reject	√	
6.1.4	Wrong viewing angle	When powered on, the clearest viewing direction of display pattern is not conform to the requested one(or not conform the direction of the customer approved samples)	Reject	√	
6.1.5	Dim or dark display	Overall contrast is either too dark or too dim under normal operation	Beyond the voltage tolerance, reject	√	
6.1.6	Responsed slowly	When power on or off some parts response time is different from others.	Reject	√	
6.1.7	Exceed segment	As misalignment and insufficient etching caused abnormally display, display with exceed pattern or display with abnormally symbol, row or columns when power on.	Refer to the dot/line standard		√
6.1.8	Dim segment	Under the normal voltage, the contrast of vertical and horizontal segments is uneven and the depth of display segments with different contrast ratio.	Reject or refer to its samples		√
6.1.9	PI black/ white spot	Partial black and white spots visible when changing display contents due to defective PI layer in the inner of LCD.	Refer to the spot/line criteria for the visible spots when display image remains still; others OK		√
6.1.10	Pinhole /white spot	Fragmental patterns appearing when it powered on caused by missing ITO.  d = (X+Y)/2	Refer to the dot/line standard		√
6.1.11	Partten distortion	The pattern displayed width is either wider, narrower or deformed than the specified, caused by its misalignment and resulting in unwanted heave(s) or missing:|Ia-Ib|≤1/4W (W is the normal width)  	|Ia-Ib|>1/4W, Reject		√
6.1.12	High current	The current of LCD is higher than the standard one.	Reject		√
6.1.13	Cross talk	The degree of cross talk should not beyond the limited samples.	Refer to its limited samples	√	

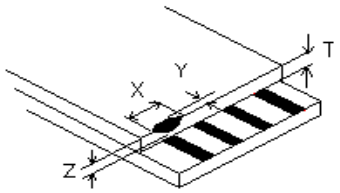
6.2 LCD appearance defect:

6.2.1 Dot and line defects (defined within VA, spots out of VA do not account)

No.	Defects	Average diameter (d)	Acceptable quantity	MAJ	MIN
6.2.1.1	Spot defects (black spot, foreign material, nick, scratches, including LC with wrong orientation）	d≤0.20	3		√
		0.20<d≤0.25	2		
		0.25<d≤0.30	1		
		0.30<d	0		
6.2.1.2	Line defects (scratches and line with foreign materials)  Line length＝L Line width＝W	W≤0.01	Not counted		√
		L≤3.0，W≤0.02	3		
		L≤3.0，W≤0.03	3		
		L≤3.0，W≤0.05	1		
		Note: when W>0.1mm it can regard as spot defect one.			
6.2.1.3	Polarizer with air bubble or convex-concave dots defect 	d≤0.3	3		√
		0.3<d≤0.5	2		
		0.5<d≤0.8	0		
Note: each of the same product should not exceed with 4 spot and line defects and the distance between each two spot should ≥5mm.					

6.2.2 Glass Damages (for LCMs without bezels and whose LCD edges exposed and for LCMs with bezels, including COG, H/S and directly assembled with BL LCMs)

No.	Defects	Acceptance Standard（unit : mm）		MAJ	MIN
6.2.2.1	chipping on conductive angle 	X	≤3.0		√
		Y	≤1/3W		
		Z	≤1/2t		
		Acceptable quantity	2		
		When Y≤0.2mm, the length of X doesn't count; for chip neither on lead nor through, when X≤1/10L， Y≤1/2W max, it doesn't count.			
6.2.2.2	chip on corner(ITO lead) 	X	≤1/10L		√
		Y	≤2/3W		
		Z	≤t		
		Acceptable quantity	2		

		For chips on the end sealing corners, refer to 6.2.2.3 and they must be out of the frame epoxy. For chips on lead, refer to 6.2.2.1			
6.2.2.3	Chip on sealed area (outer chip)  	X	≤1/8L		√
		Y	≤1/2H		
		z	≤ 1/2t		
		Acceptable quantity	2		
		The standard for inner chip on sealed area is the same as the standard for outer. For chip on the reverse of ITO contact pad ledge, refer to 6.2.2.1 for chip on the reverse of ITO contact pad ledge for the value of Y.			
Note: X means the length of chip; Y means the width of the chip; Z means the thickness of the chip; W means the width of the stage of the two glasses; L means the length of the glass; H means the distance between the glass edge and the inner side of frame glue; t means the thickness of the glass.					

6.2.3 Others

No.	Defects	Description	Acceptance standard	MAJ	MIN
6.2.3.1	Rain ball/ bottom color	There is two different color in the same one product or the same batch products with two different colors	Reject or refer to the limited samples		√
6.2.3.2	Leaking ink (LC)	/	Reject	√	
6.2.3.3	Without protect film	/	Reject		√
6.2.3.4	Splay mark	Inspecting whether the surface of polarizer with splay marks against the light	Refer to the limited samples		√

6.3 Backlight components:

No.	Defects	Description	Acceptance standard	MAJ	MIN
6.3.1	Backlight not working, wrong color	/	Reject	√	
6.3.2	Color deviation	When powered on, the LCD color differs from its sample and found that the color not conforming to the drawing after testing.	Refer to sample and drawing		√
6.3.3	Brightness deviation	When powered on, the LCD brightness differs from its sample and is found after testing not conforming to the drawing; or if it conforms to the drawing but the brightness over ±30% than its sample.	Refer to sample and drawing		√
6.3.4	Uneven brightness	When powered on, the LCD brightness is uneven on the same LCD and out of the specification of the drawing. The no	Refer to sample and drawing		√

		specification evenness= (the max value- the min value)/ mean value< 70%.			
6.3.5	Spot/line scratch	When power on, it with dirty spot, scratches and so on spot and line defects	Refer to 6.2.1		√
6.3.6	BL wrapped	The BL should paste tightly on the PCB.	The BL can be allowed within 1mm wrapped parts, if them not affect its appearance and outline dimension.		√
6.3.7	Flicker and with LED shade	When power on, each bright source should not with flicker and the brightness should evenness and without LED shades.	Reject	√	

6.4 Metal frame (Metal Bezel)

No.	Defects	Description	Acceptance standard	MAJ	MIN
6.4.1	Material/surface treatment	Metal frame/surface treatment do not conform to the specifications.	Reject	√	
6.4.2	Tab twist inconformity/ Tab not twisted	Wrong twist method or direction and twist tabs are not twisted as required.	Reject	√	
6.4.3	Oxidization	Oxidation on the surface of the metal bezel	Reject		√
6.4.4	Painting peel off, discoloration, dents, and scratches	1）the front surface with painting peel off and scratched can be see the bottom: Dot : D≤0.5mm, exceeds 3; Line: length ≤3.0mm, width ≤0.05mm , exceeds 2; 2）front dent, air bubble and side with painting peel off which scratched can be see the bottom: Dot: D≤1.0mm, exceeds 3; Line: length ≤3.0mm, width ≤0.05mm, exceeds 2.	Reject		√
6.4.5	Burr	Burr(s) on metal bezel is so long as to get into viewing area.	Reject		√

6.5 PCB/COB

No.	Defects	Description	Acceptance standard	MAJ	MIN
6.5.1	Improper Epoxy Cover	1） Contacts exposure within the white circle for COB chip bonding. 2） The height of epoxy cover is out of the product specifications and drawing. 3） The epoxy cover over the COB chip exceeds the circle by more than 2mm in diameter, which is the maximum distance the epoxy cover is allowed to exceed the circle. 4） Existence of obvious linear mark(s) or chip-exposing pinhole on the epoxy cover.	Reject		√

		5） The pinhole diameter on the epoxy over exceeds 0.25mm and there is foreign matter in the pinhole.			
6.5.2	PCB appearance defect	1） Oxidized or contaminated gold fingers on PCB. 2） Bubbles on PCB after reflow-soldering. 3） Exposure of conductive copper foil caused by peeled off or scratched solder-resist coating. For the conductive area of PCB repaired with the solder resist coating material, the diameter ψ of the repaired area on the circuit must not exceed 1.3mm while for the non-conductive area of PCB repaired with the solder resist coating material, the diameter ψ must not exceed 2.6mm; the total number of repaired areas on PCB must be less than 10; otherwise, the PCB must be rejected.	Reject		√
6.5.3	Wrong or missing Components on PCB	1） Components on PCB are not the same as defined by drawing such as wrong, excessive, missing, or mis-polarized components. (The bias circuit of LCD voltage or the backlight current limiting resistance is not adjusted unless specified by the customer.） 2） The JUMP short on PCB shall conform to the mechanical drawing. If excessive or missing soldering occurs, the PCB shall be rejected. 3） For components particularly required by the customer and specified in the mechanical drawing and/or component specifications, their specifications must conform to those of the suppliers; otherwise they shall be rejected.	Reject	√	

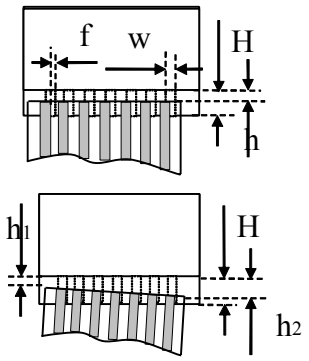
6.6 Connector and other components

No.	Defects	Description	Acceptance standard	MAJ	MIN
6.6.1	Out of Specification	The specification of connector and other components do not conform to the drawing.	Reject		√
6.6.2	Position and order	Solder position and Pin# 1 should be in the positions specified by the drawing.	Reject		√
6.6.3	Appearance	1）Flux on PCB components and pins. 2）The pin width of a PIN connector exceeds ½ of the specified pin width.	Reject		√
6.6.4	Glue amount	Flat cable connector: as the conducted wire fixed with glue, if the glue not fully covered the exposed wire and the copper part around holes will be rejected.	Reject		√
6.6.5	Through holes blocked	Socket connector: the components can not plug-in units as the through holes blocked and deformation; the locks which with lock catch can not make the external connector to be locked.	Reject		√

6.7 SMT (Refer to IPC-A-610E the second standard if not specified)

No.	Defects	Description	Acceptance standard	MAJ	MIN
6.7.1	Soldering solder defects	Cold, false and missing soldering, solder crack and insufficient solder dissolution.	Reject		√
6.7.2	Solder ball/splash	Solder ball/tin dross causing short circuit at the solder point. There are active solder ball and splash.	Reject		√
6.7.3	DIP parts	Floated or tilted DIP parts, keypad, and connectors.	Reject		√
6.7.4	Solder shape	The welded spot should be concave and excessive or insufficient solder or solder burr on the welded spot must be rejected.	Reject		√
6.7.5	Component pin exposure	For the DIP type components, 0.5~2mm component pin must be remained after cutting the soldered pin and the solder surface neither should not be damaged nor should the component pin is fully covered with solder; otherwise rejected.	Reject		√
6.7.6	Poor Appearance	The LCMs become yellow-brown or black as the residual resin or solder oil. There is white mist residual at the solder point caused by PCB cleaning.	Reject		√

6.8 Hot Pressing components (including H/S，FPC, etc.）

No.	Defects	Description	Acceptance standard	MAJ	MIN
6.8.1	Out of its specification		Reject	√	
6.8.2	Size		Refer to its drawing		√
6.8.3	Position	 Note: H=ITO pin length, W=ITO pin width, f= heat seal or the misplaced width of TAB.	1, If f≤1/3w，h ≤1/3H, and its conform to the size and specification on drawing, which will be received. 2, The contact area of dielectric material conductor position and pressing material over 1/2 (controlling as per each ITO position) will be received.		√
6.8.4	Foreign Matter in Hot pressing area	If foreign matter in non-conductive heat compression area shall not cause short, it is OK. If foreign matter in conductive heat compression area does not exceed 50% of the heat pressure area, it is OK.	Receive		√
6.8.5	Fold marks		Refer to the limited samples.		√

6.9 General Appearance

No.	Defects	Description	Acceptance standard	MAJ	MIN
6.9.1	Connection material	Damaged or contaminated FPC or H/S gold fingers or FFC contact pin side with exposed copper foil or base materials. Sharp folds on FPC, FFC, COF, H/S (unless designed for). Solder paste larger than 2/3 of pin width on the gold finger of FPC and PCB. Pierced or folded FPC/FFC exceeding limit sample.	Reject		√
6.9.2	Poor reinforcing band	The protect tape using for reinforce which not complete covered the needed protection circuits (such as H/S, FFC, FPC, etc.) or it not joint with its pasted material or it glued on the output side of pins.	Reject		√
6.9.3	Surface dirt	The surface of finished LCMs with smudge, residual glue, and finger prints, etc; solder spatters or solder balls on non-soldered area of PCB/COB. Non-removed defect mark or label on LCMs.	Reject		√
6.9.4	Assembly black spot	Smears or black spots found on LCMs after backlight or diffusion barrier are assembled.	Refer to 6.2.1		√
6.9.5	Product mark	Missing, unclear, incorrect, or misplaced part numbers and/or batch marks.	Reject		√
6.9.6	Inner packing	Packing being inconsistent with quantity and part number on packing label, specifications or the customer order - either short-packed or over-packed.	Reject		√

7. Reliability test

Test items	Condition	Time （hrs）	Acceptable standard
Store in high temperature	-30℃	240hrs	Its function and appearance qualified before and after test
Operation under high temperature	-20℃		
Store in low temperature	80℃		
Operation under low temperature	70℃		
Humidity test	60℃,90%RH		
Temperature cycle	-30C ← 25°C →+80°C (30 min ← 5 min → 30min)	10 cycles	
Note1:The temperature allowable deviation is ±5℃ and the humidity allowable deviation is ±5%RH.			

8. Packing

8.1 The acceptance inspection of product packing shall meet design requirements. The product packaging label shall bear not only product name, part number, quantity, product date code but also QA's qualifying stamp for each production stage. Incomplete or wrong label shall be unacceptable.

8.2 When there are problems with packing safety conformity such as shock resistance, moisture resistance, anti ESD and press resistance, packing shall be disqualified.

8.3 When customer's special requirements for packing confirmed and accepted by OD, packing shall be inspected and released according to them.

8.4 RoHS and non-RoHS compliant products shall be labeled clearly and separately. Unless otherwise specified by the customer, "RoHS" labels shall be used for all RoHS compliant products.

9. Others

9.1 Items not specified in this document or released on compromise should be inspected with reference to mutual agreement and limit samples.