

Dual N-Channel Logical Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN 3x3 saves board space
- Fast switching speed
- High performance trench technology

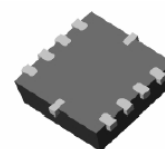
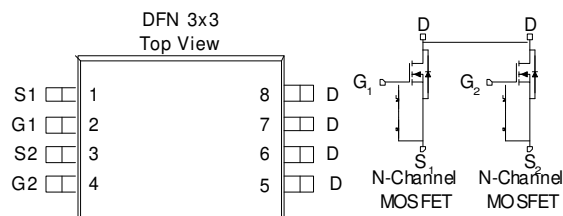


RoHS
COMPLIANT
HALOGEN
FREE



ESD Protected
2000V

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
20	0.012 @ $V_{GS} = 4.5$ V	9.2
	0.014 @ $V_{GS} = 2.5$ V	8.5



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	9.2	A
	$T_A = 70^\circ\text{C}$		7.5	
Pulsed Drain Current ^b		I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a		I_S	1.5	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.5	W
	$T_A = 70^\circ\text{C}$		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typ	Max	
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	72	83	$^\circ\text{C/W}$
	Steady State		100	120	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions				Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	0.3			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			±10	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V			1	μA
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 55°C			10	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	30			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 2 A			0.012	Ω
		V _{GS} = 2.5 V, I _D = 2 A			0.014	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 10 V, I _D = 2 A		25		S
Diode Forward Voltage ^A	V _{SD}	I _S = 2 A, V _{GS} = 0 V		0.89		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} =10V, V _{GS} =4.5V, I _D =2A		13.4		nC
Gate-Source Charge	Q _{gs}			0.9		
Gate-Drain Charge	Q _{gd}			2.0		
Turn-On Delay Time	t _{d(on)}	V _{DD} =10V, V _{GS} =4.5V, I _D =1A , R _{GEN} =10Ω		18		nS
Rise Time	t _r			25		
Turn-Off Delay Time	t _{d(off)}			50		
Fall-Time	t _f			25		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information

