

AMC DOC. #:AMC7661_B (LF)
March 2004



AMC7661

STANDARD VOLTAGE DETECTOR

DESCRIPTION	FEATURES
The AMC7661 series are low power, highly accurate voltage detectors by CMOS with programmable trimming technology. The detect voltage is extremely precise with temperature drift. AMC7661 series are available both CMOS and N Channel output configurations.	■ 2% accuracy ■ Detect voltage range from 1.6V to 6.0V ■ Low power consumption of typ. 0.7μA with $V_{IN} = 5V$. □ CMOS and N Channel open drain output configurations available. □ Detect voltage accuracy of typ. $\pm 1000\text{ppm}/^{\circ}\text{C}$ with temperature drift.

APPLICATIONS	PACKAGE PIN OUT
■ System battery life and charge voltage monitors ■ Microprocessor reset ■ Power-on reset ■ Power failure detection ● Output Stage Options: AMC7661□C: CMOS Output AMC7661□N: N Channel Open Drain Output	AMC76611-x.xPK 3-Pin Plastic SOT-89 Surface Mount (Top View) AMC76612-x.xPK 3-Pin Plastic SOT-89 Surface Mount (Top View) AMC76611-x.xDBT 3-Pin Plastic SOT-23 Surface Mount (Top View) AMC76612-x.xDBT 3-Pin Plastic SOT-23 Surface Mount (Top View)

ORDER INFORMATION				
$T_A (^{\circ}\text{C})$	PK	Plastic SOT-89	DBT	Plastic SOT-23
		3-pin		3-pin
0 to 70	AMC76611C-x.xPK		AMC76611C-x.xDBT	
0 to 70	AMC76611C-x.xPKF(Lead Free)		AMC76611C-x.xDBTF(Lead Free)	
0 to 70	AMC76611N-x.xPK		AMC76611N-x.xDBT	
0 to 70	AMC76611N-x.xPKF(Lead Free)		AMC76611N-x.xDBTF(Lead Free)	
0 to 70	AMC76612C-x.xPK		AMC76612C-x.xDBT	
0 to 70	AMC76612C-x.xPKF(Lead Free)		AMC76612C-x.xDBTF(Lead Free)	
0 to 70	AMC76612N-x.xPK		AMC76612N-x.xDBT	
0 to 70	AMC76612N-x.xPKF(Lead Free)		AMC76612N-x.xDBTF(Lead Free)	
Note: 1.PK package is available in Tape & Reel. Append the letter "T" to part number (i.e. AMC76611C-x.xPKT and etc.). DBT package is only available in Tape & Reel. 2.The letter "F" is marked for Lead Free process.				

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EXPANDED ORDER INFORMATION					
Device Name	Detect Voltage	Symbolization			
		AMC76611C	AMC76611N	AMC76612C	AMC76612N
AMC7661□-2.5DBT	2.5V	1C25	1N25	2C25	2N25
AMC7661□-2.7DBT	2.7V	1C27	1N27	2C27	2N27
AMC7661□-3.3DBT	3.3V	1C33	1N33	2C33	2N33

TYPICAL APPLICATION

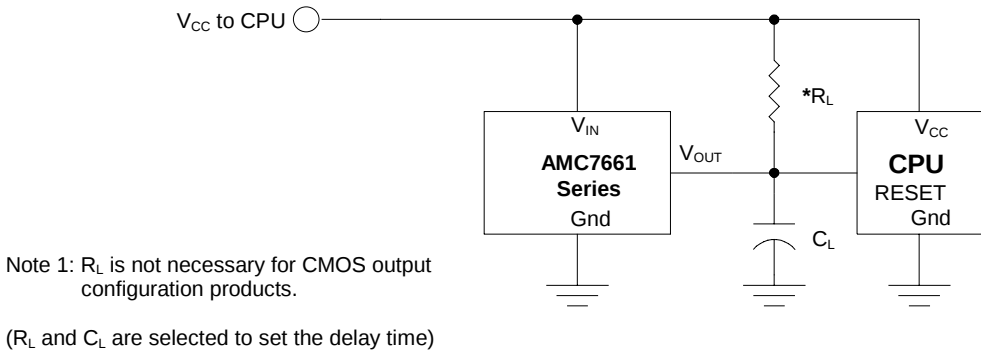


Figure 1. Application circuit for CPU resetting

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage, V _{IN}		12V
Output Current, I _{OUT}		50mA
Output Voltage, V _{OUT}	CMOS Output Configuration	0.3V to (V _{IN} – 0.3V)
	N Channel Open Drain Output Configuration	0.3V to V _{IN}
Storage Temperature Range		-65 to 150
Lead Temperature (soldering, 10 seconds)		260
Note 1: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.		

RECOMMENDED OPERATING RATINGS

Temperature Range	-40 $\leq T_J \leq 125$
Input Voltage, V_{IN}	12V(Max.)

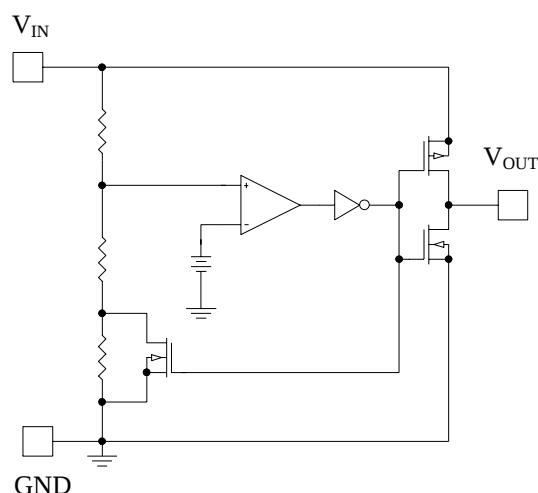
POWER DISSIPATION TABLE

Package	θ_{JA} ($^{\circ}C/W$)	Derating factor ($mW/^{\circ}C$) $T_A \geq 25^{\circ}C$	$T_A \leq 25^{\circ}C$ Power rating (mW)	$T_A = 70^{\circ}C$ Power rating (mW)	$T_A = 85^{\circ}C$ Power rating (mW)
PK	71(note)	14.1	1763	1128	916
PKF	71(note)	14.1	1763	1128	916
DB	285	3.5	438	280	228
DBF	285	3.5	438	280	228

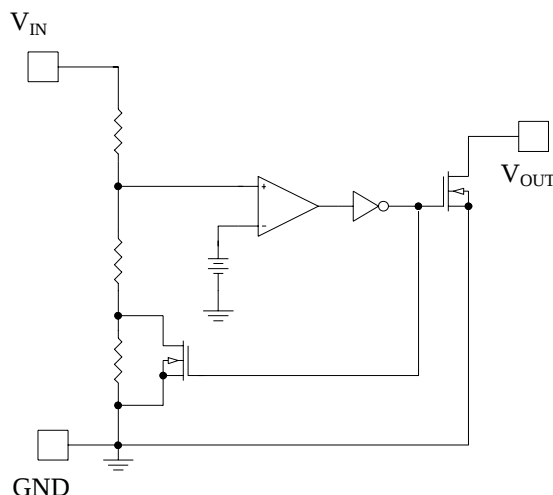
Note:

- For PK package, Thermal Resistance-Junction to Tab (θ_{JT}) = $35^{\circ}C/W$. $T_J = T_{TAB} + (P_D \times \theta_{JT})$
- θ_{JA} : Thermal Resistance-Junction to Ambient
Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/PC-board system.
All of the above assume no ambient airflow.

BLOCK DIAGRAM



AMC7661□C
CMOS Output



AMC7661□N
N Channel Open Drain Output

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DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply the operating ambient temperatures $T_J = 25^\circ\text{C}$.

Parameter	Symbol	Test Conditions		AMC7661			Units	
				Min	Typ	Max		
Detect Voltage	V _{DF}			0.98 × V _{DF}	V _{DF}	1.02 × V _{DF}	V	
Supply Current	I _{CC}		V _{IN} = 1.5V		0.7	2.3	μA	
			V _{IN} = 2.0V		0.8	2.7		
			V _{IN} = 3.0V		0.9	3.0		
			V _{IN} = 4.0V		1.0	3.2		
			V _{IN} = 5.0V		1.1	3.6		
Hysteresis Range	V _{HYS}			0.02 × V _{DF}	0.05 × V _{DF}	0.08 × V _{DF}	V	
Operating Voltage	V _{IN}			0.7		10	V	
Output Current	I _{OUT}	Nch V _{DS} = 0.5V	V _{IN} = 1.0V	1.0	2.2		mA	
			V _{IN} = 2.0V	3.0	7.7			
			V _{IN} = 3.0V	5.0	10.1			
			V _{IN} = 4.0V	6.0	11.5			
			V _{IN} = 5.0V	7.0	13.0			
		Pch (with CMOS Output), V _{DS} = 2.1V	V _{IN} = 8.0V			-10.0	-2.0	mA
		Delay Time	t _{delay}	V _{IN} changes from 0.6V to 10V. Note 1				0.2
Temperature Coefficient		-40°C ≤ T _{OPERATION} ≤ 85°C			± 100		ppm/%	

Note:

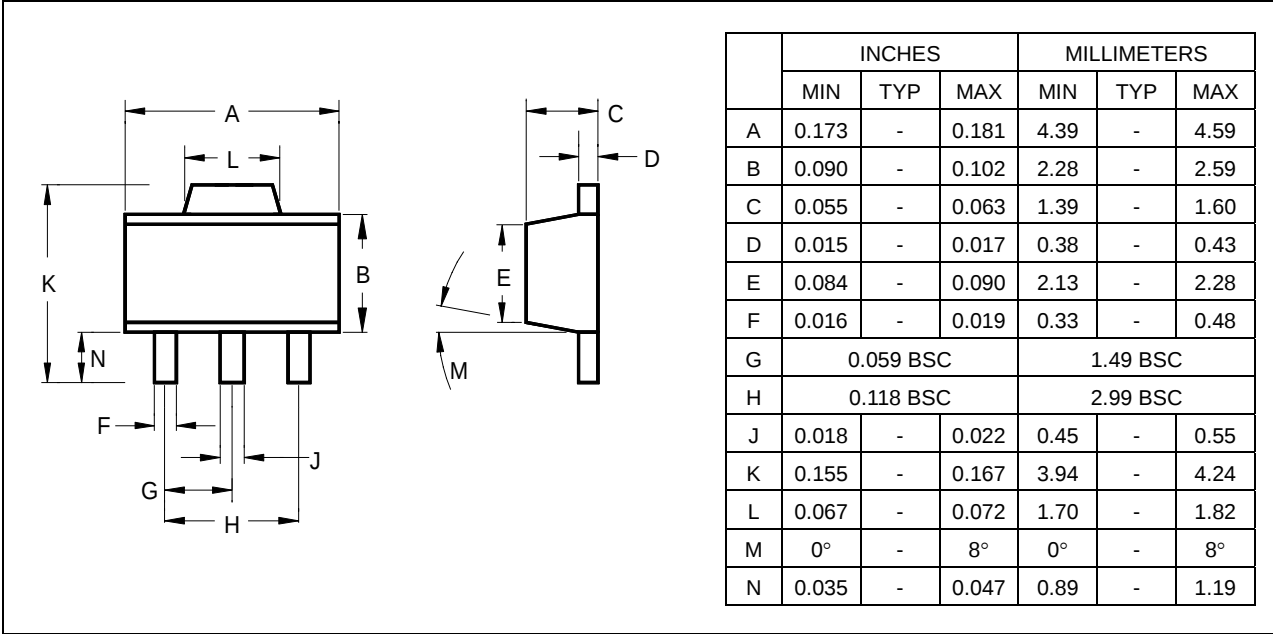
1. Delay time represents the time required for V_{OUT} equals to V_{IN} when V_{IN} voltage exceeds threshold voltage.

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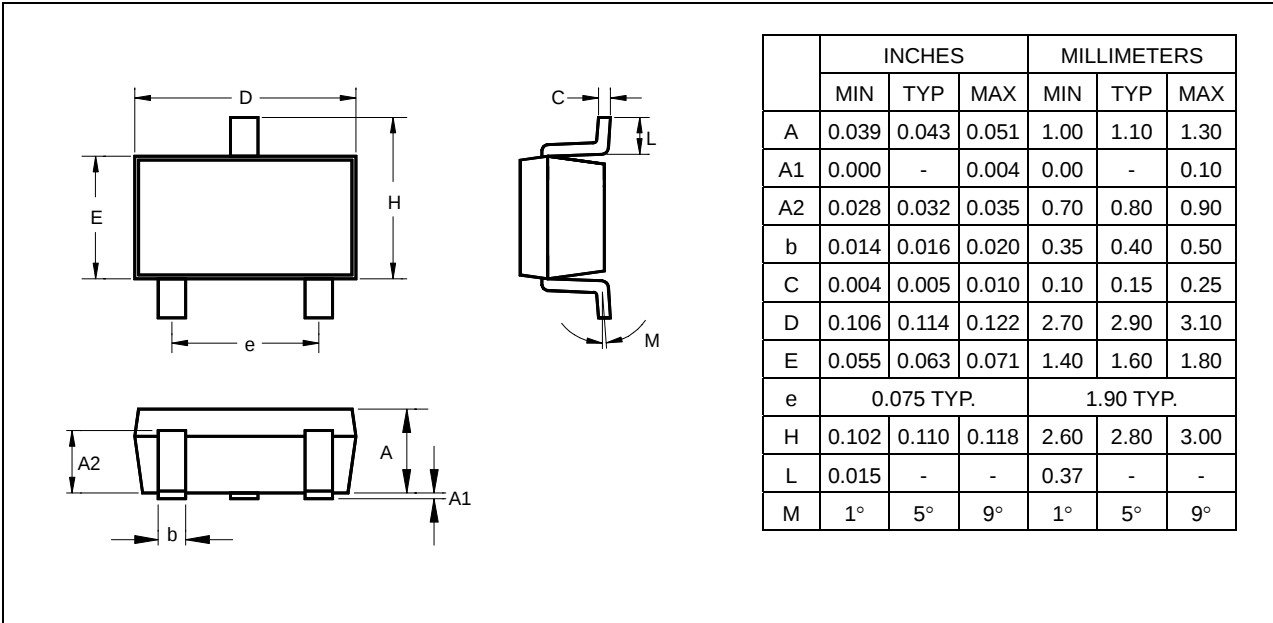
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3-Pin Surface Mount SOT-89



Surface Mount SOT-23



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IMPORTANT NOTICE

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