Preliminary

Am95C75

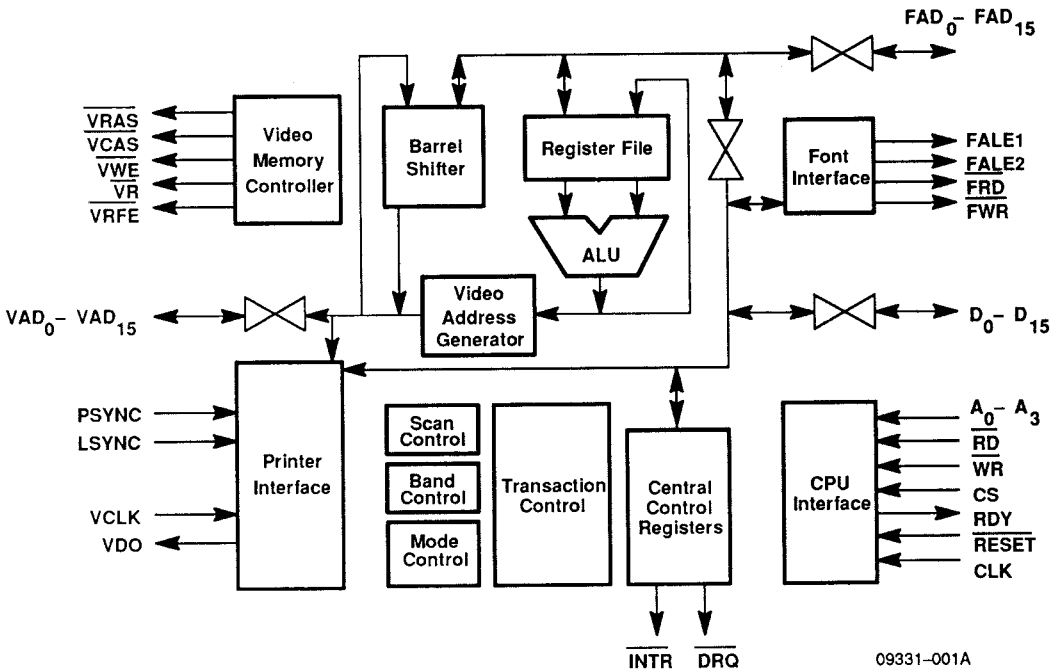
Raster Printer Controller (RPC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 20 Mb/s printing of combined text and graphics
- Triple-bus architecture for independent host, font memory and page buffer interfaces and direct connection to print engines
- Supports any combination of transparent, opaque and textured images at pixel addressable positioning
- 24-bit addressing provides for page buffers up to 16K x 16K pixels and 16M words of font memory space
- Supports two band buffers with automatic virtual address conversion to reduce memory requirements
- On-board programmable DRAM controller with refresh
- Synchronous or asynchronous interface to print engines with a broad range of page size and margins
- Operating modes for direct interface to Am95C76 Orthogonal Rotation Processor (ORP)

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Am95C75 Raster Printer Controller (RPC) is a high-performance CMOS processor for controlling the real-time requirements of a raster printing system. It is designed to assemble text and graphical images into a partial or full page buffer from either of two memory spaces or from the host and serially transmit that image information to an asynchronous print engine. A high degree of programmable options assures simple interfacing to a broad range of host, memory, and printer configurations.

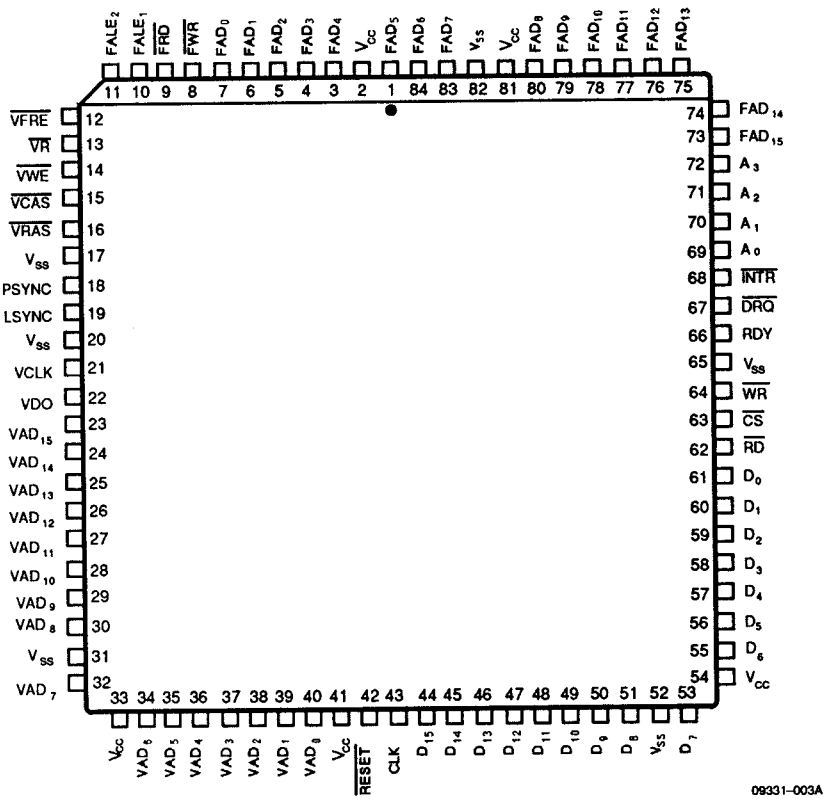
The RPC receives source and destination address information (or image data) from the host CPU or DMA controller, and performs block transfers of data to rectangular areas at the destination address in the buffer. The image blocks are of arbitrary size and pixel alignment and may be combined with background information using the overlay options. Characters may be textured using the additional source address of a texture word or array. In addition to the buffer assembly operations, the RPC can transfer font or graphic information with the host to or from the static RAM or ROM Font memory or the DRAM Video memory of the buffer.Two other modes support reading and writing of the Am95C76 Orthogonal Rotation Processor (ORP) which resides in Font memory space.

Printing can begin when a page or band is completely assembled and is controlled by Page and Line Sync signals provided by the print engine. Pixel data is serialized at a rate controlled by the Video clock (VCLK). Page Size and Margins are determined by the values programmed in the RPC control registers. In systems where two band buffers are used, one band may be assembled while the other band is being scanned out. The RPC manages all address conversion so that the host need only provide a destination address for each image block that corresponds to the virtual position of that block on the full page. Band control logic in the RPC insures that the bands alternate properly according to the scanning requirements of the printer. Image blocks or fonts that are sliced by a band boundary cause interrupts that allow the remaining portion to be transferred into the next band.

The system bus interface of the RPC allows the control registers to reside in host I/O or memory space and operations are initiated automatically when the address information for the transfer is provided. An internal address pointer sequences through the control registers required to setup a block transfer so that the host may write them to a single port address if that is desired. The RPC will interrupt the CPU or request a DMA when the transfer is complete. Interrupt options allow the host to be updated on transfer, printing, and error conditions by reading status information.

CONNECTION DIAGRAM

PLCC



09331-003A

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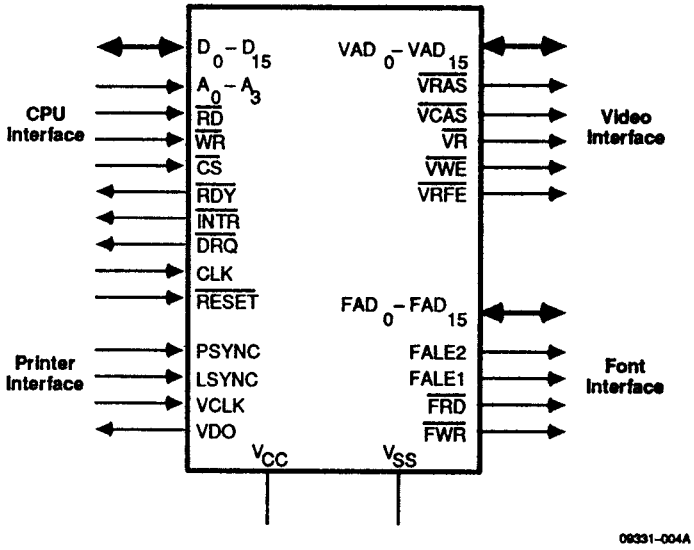
LOGIC SYMBOL

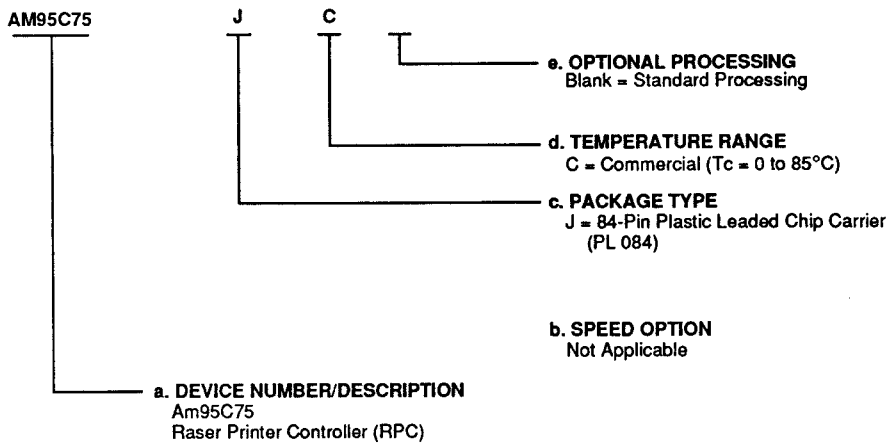


ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM95C75	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

5

PIN DESCRIPTION

Interface Signal Description

The RPC has four independent groups of pins to interface to the other resources of the printing system. The CPU Interface connects to the host to provide control of all operations. The Font Memory Interface connects to an optional static memory of RAM or ROM for storage of character fonts, textures and other blocks of data. The Font Memory Interface also interfaces directly to the Am95C76 ORP. The Video Memory Interface connects to standard Dynamic RAMs for the page buffer or for storage of downloaded fonts or other data. This latter case permits a system with a single memory architecture. The Printer Interface accepts timing information from the print engine and supplies serial pixel data for the rasterized page.

CPU Interface Signals

A_0–A_3
Address Bus (Input)

The 4-bit Address Bus is used to select one of sixteen internal registers for reading or writing. It must be held valid while the access is taking place.

CLK
Clock (Input)

The Clock input provides the timing reference for all operations controlled by the RPC except printing. All memory operations on the Font or Video Interfaces will occur relative to Clock edges. Accesses on the CPU Interface may be asynchronous to the Clock.

$\overline{CS}$
Chip Select (Input; Actve LOW)

Chip Select must be held LOW to qualify a read or write access by the host. Chip Select may be held LOW for multiple accesses.

D_0–D_{15}
Data Bus (Input/Output; Three-State)

The 16-bit bidirectional Data Bus is used for all read and write accesses by the host system. The bus is an output whenever $\overline{CS}$ and $\overline{RD}$ are active and is an input whenever $\overline{CS}$ and $\overline{WR}$ are active.

$\overline{DRQ}$
DMA Request (Output; Actlve LOW)

The Data Request output is driven LOW when the RPC is ready to accept the address information required to transfer an image block and is driven HIGH when the last word of address information is received. Five words are required for a normal Dispatch operation and eight words are required for a textured Dispatch operation. Data Request will only be driven LOW when the RPC is in Dispatch, ORP Load or ORP Read Mode. It is intended for direct connection to a DMA controller.

$\overline{INTR}$
Interrupt (Output; Active LOW)

The Interrupt output is driven LOW whenever the RPC detects a condition that requires the attention of the CPU and the Interrupt Enable bit is set. Interrupt is driven HIGH when status is read by the CPU to identify the cause of the interrupt. All interrupt status bits are cleared after the register is read.

$\overline{RD}$
Read (Input; Active LOW)

The active-LOW Read input determines when the contents of the selected internal register are driven onto the Data Bus.

RDY
Ready (Output)

The Ready output is driven LOW at the start of a Read or Write access when the data is not immediately available or cannot be accepted. The host must insert wait states and hold Read or Write active until Ready goes HIGH to complete the access successfully. If Read or Write go HIGH while Ready is being driven LOW, the access is aborted and Ready will go HIGH. In this abort case, there is no guarantee that the access was accepted or ignored.

$\overline{RESET}$
Reset (Input; Actve LOW)

The active-LOW $\overline{RESET}$ input causes the RPC to terminate any operation in progress and enter the idle state. $\overline{RESET}$ must be held LOW for a minimum of four CLK cycles. After Reset, all bidirectional buses will be in a high impedance state and all internal registers must be programmed to begin operation.

$\overline{WR}$
Write (Input; Active LOW)

The active-LOW Write input determines when the contents of the Data Bus are loaded into the selected internal register.

Font Memory Interface Signals

FAD_0–FAD_{15}

Font Address/Data Bus (Input/Output; Three-State)

The 16-bit bidirectional Font Address/Data Bus carries all address and data information for Font Memory accesses. The presence of information on this bus is always controlled by the signals described below.

FALE1

Font Address Latch Enable 1 (Output)

The FALE1 output is driven HIGH when the least significant 16 bits of the 24-bit Font Memory address are being driven onto FAD_0–FAD_{15}. This address information must be latched on the HIGH-to-LOW transition of FALE1. The lower address cycle, containing FALE1, occurs on every memory cycle.

FALE2

Font Address Latch Enable 2 (Output)

The FALE2 output is driven HIGH when the most significant 8 bits of the 24-bit Font Memory address are being driven onto FAD_0–FAD_7. This address information must be latched on the HIGH-to-LOW transition of FALE2. The upper address cycle, containing FALE2, is sometimes skipped when the upper address is unchanged from the previous memory cycle.

$\overline{FRD}$

Font Read (Output; Active LOW)

The active-LOW Font Read output is driven LOW during a Font Memory access when data is to be driven onto the FAD_0–FAD_{15} bus by the memory. $\overline{FRD}$ stays low for 1 to 8 CLK cycles depending on the number of Font Memory Wait states programmed.

$\overline{FWR}$

Font Write (Output; Active LOW)

The active-LOW Font Write output is driven LOW when valid data is being driven onto the FAD_0–FAD_{15} bus by the RPC to be strobed into the Font Memory. $\overline{FWR}$ stays low for 1 to 8 CLK cycles depending on the number of Font Memory Wait states programmed. The FAD data out is valid for the duration of $\overline{FWR}$.

Video Memory Interface Signals

VAD_0–VAD_{15}

Video Address/Data Bus (Input/Output; Three-State)

The 16-bit bidirectional Video Address/Data Bus carries all address and data information for Video Memory accesses. The presence of information on this bus is always controlled by the signals described below.

$\overline{VCAS}$

Video Column Address Strobe (Output; Active LOW)

The $\overline{VCAS}$ output is driven LOW to indicate that a valid column address is being output on the VAD_0–VAD_{15} bus. The HIGH-to-LOW transition of $\overline{VCAS}$ is normally used to strobe the column address into dynamic RAMs. The column address cycle follows a row address cycle except during memory refresh operations.

$\overline{VR}$

Video Read (Output; Active LOW)

The $\overline{VR}$ output is driven LOW to indicate that external VAD bus transceivers should drive Video Memory data onto the VAD_0–VAD_{15} bus to be input by the RPC. This signal can be used to avoid bus contention between the Video Memory address being driven out and the memory data being received by the RPC.

$\overline{VRAS}$

Video Row Address Strobe (Output; Active LOW)

The $\overline{VRAS}$ output is driven LOW to indicate that a valid row address is being output on the VAD_0–VAD_{15} bus. The HIGH-to-LOW transition of $\overline{VRAS}$ is normally used to strobe the row address into dynamic RAMs.

$\overline{VRFE}$

Video Refresh Enable (Output; Active LOW)

The $\overline{VRFE}$ output is driven LOW for the duration of a Video Memory Refresh operation. This signal can be used to control the bank select decoder so that all memory chips receive $\overline{RAS}$ on the refresh row address cycle.

$\overline{VWE}$

Video Write Enable (Output; Active LOW)

The $\overline{VWE}$ output is driven LOW to indicate that valid data is being output on the VAD_0–VAD_{15} bus. The HIGH-to-LOW transition of $\overline{VWE}$ is normally used to strobe data into dynamic RAMs.

Printer Interface Signals

LSYNC

Line Sync (Input)

The LOW-to-HIGH transition of the LSYNC input is used to start a scan line sequence that may consist of a decrement of the Y-Margin count or the start of the X-Margin control process prior to the scan out of serial pixel data for a line. LSYNC will only be recognized if the conditions for a PSYNC have been met.

PSYNC

Page Sync (Input)

The LOW-to-HIGH transition of the PSYNC input is used to start the Y-Margin control process if the RPC has been initialized to scan out the serial pixel information of a page on the VDO output. PSYNC will be recognized if the RC bit in the Mode Register is set and the beginning of the first scan line has been loaded in the the RPC shift register. Otherwise PSYNC will be ignored.

VCLK

Video Clock (Input)

The VCLK input determines the data rate for serialization of pixel data on the VDO output during scan out. If the Printer Interface is being operated in Synchronous Mode, the serial data rate equals the VCLK rate. In Asynchronous Mode the data rate equals the VCLK rate divided by four. The mode determines whether LSYNC must be synchronous to VCLK in addition to the VCLK division control. PSYNC has no timing requirement related to VCLK in either mode.

VDO

Video Data Out (Output)

The VDO output provides the serial pixel data that is used by the print engine to scan out the page. When the Printer Interface is inactive or during the X or Y Margin time, the VDO output remains HIGH. VDO may toggle at the pixel rate during the active page area and the output polarity is selected by the VP bit in the Mode Register.

FUNCTIONAL DESCRIPTION

Register Description

The RPC contains 16 user-addressable registers that may be accessed by the CPU Interface. Each register has a unique location as selected by the A_0–A_3 address pins. These registers may be grouped into the Temporary Register, Operation Control Registers, Source Address Registers, Texture Address Registers and Destination Address Registers according to Table 1.

Table 1. RPC Registers

	Port Address	Name
	0	Temporary Register (Temp)
Operation Control Registers:	1	Mode/Status Register (Mode)
	2	Margin Register (XMGR, YMGR)
	3	Page X Size Register (PXSR)
	4	Page Y Size Register (PYSR)
	5	Video Band Boundary Register (VBBR)
	6	Video Memory Refresh Rate Register (VMRR)
	7	Memory Timing Register (MTR)
Source Address Registers:	8	Source Address Register 1 (SAR1)
	9	Source Address Register 2 (SAR2)
	10	Source Address Register 3 (SAR3)
Texture Address Registers:	11	Texture Address Register 1 (TAR1)
	12	Texture Address Register 2 (TAR2)
	13	Texture Address Register 3 (TAR3)
Destination Address Registers:	14	Destination Address Register 1 (DAR1)
	15	Destination Address Register 2 (DAR2)

In order to minimize the number of registers that must be programmed to begin RPC operations, some registers have unrelated bytes or fields packed together. Some of the address registers contain control fields that specify options for the address or the related operations.

For Dispatch operations, the address registers may be loaded using the automatic sequencing feature provided by the RPC. This allows all words to be written to the Temporary Register at Port 0 in the proper order, and be loaded into the correct location. Repetitive operations may be programmed by the host without complex port address changes using this feature. The Texture Address Registers are automatically skipped if texturing is not selected, so only five words must be loaded for each non-textured Dispatch.

The Temporary Register, at Port 0, serves as a holding register for data in some RPC operations. In Font Load, Font Read and Graphics Load modes, the TEMP holds data for transfer between the host and the Font or Video Memory Interfaces. Since the host and the RPC internal controller must share access, the TEMP may not always be ready for the host, and the RDY pin will be driven inactive until the internal operation is complete.

In Dispatch and ORP Modes, the TEMP location can be used for writing values to the SAR, TAR and DAR words. These words must be written in the proper order to be loaded correctly. When the last word (DAR2) is written to Port 0, the operation is initiated. The next word written to Port 0 (after $\overline{DRQ}$ goes active) will be assumed to be SAR1 for the start of the next operation. These address registers may also be read or written using their explicit port addresses.

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Operation Control Registers

The Operation Control Registers are normally initialized once after the power-up and $\overline{\text{RESET}}$ is applied, and with the exception of the Mode Register, are not changed frequently during the operation of the RPC. These registers provide the system configuration information for the printer and memory interfaces. See Figure 1 for the placement of control bits and fields in these registers.

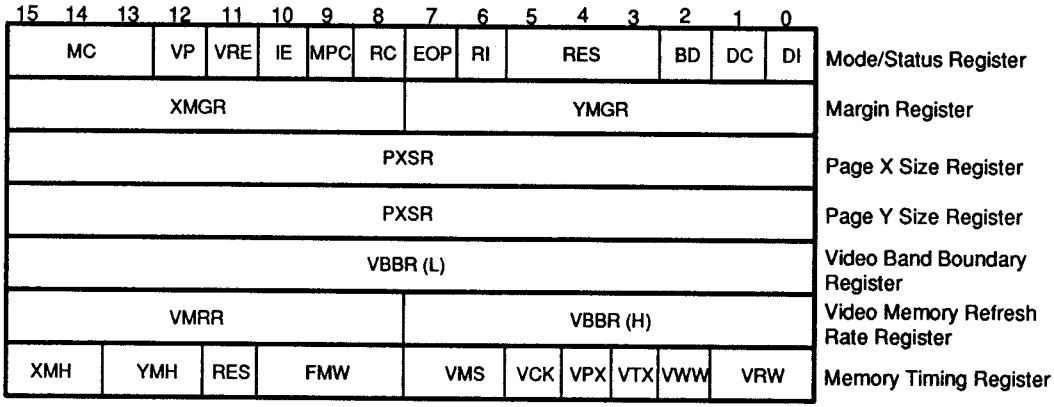


Figure 1. Operation Control Registers

Mode/Status Register

The upper byte of the Mode/Status Register allows the operation type and various options to be selected and the lower byte provides a read-only access to Status flags (see Figure 2). The Status may be read at any time during RPC operations and special provision has been made to optimize the response of the Ready pin for accesses of this register. Flag bits that are active will be cleared after each read access to insure that each read accurately reflects the current Status. Writes to the Mode Register may not be recognized until the RPC has completed the current operation, however, changing certain bits in the Mode may cause unexpected results if care is not taken to allow printing operations to complete.

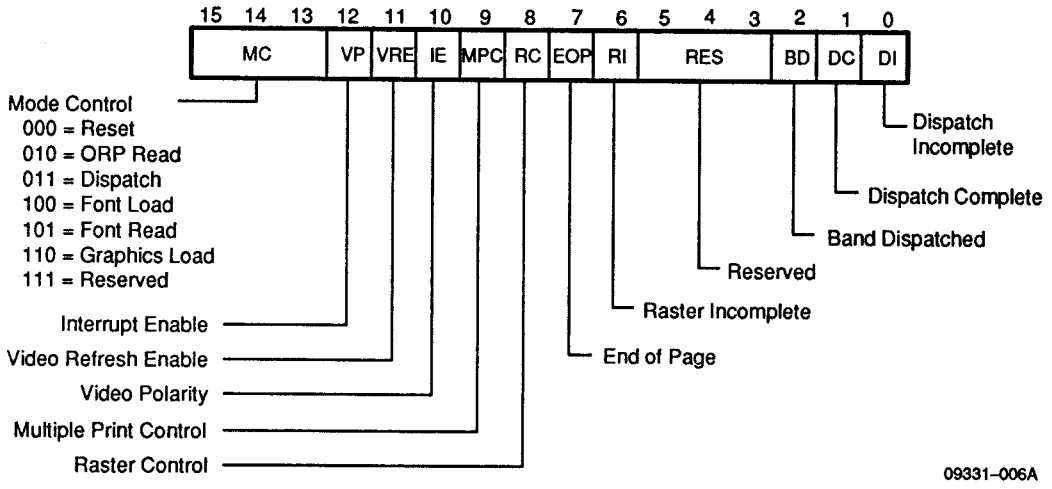


Figure 2. Mode/Status Register

Bits 13, 14 and 15 of the Mode Register are the Mode Control field and are used to select the operation type according to Table 2.

Table 2. Mode Control Field

Bit	15	14	13	Operation Type
	0	0	0	Software Reset
	0	0	1	ORP Read
	0	1	0	ORP Load
	0	1	1	Dispatch
	1	0	0	Font Load
	1	0	1	Font Read
	1	1	0	Graphics Load
	1	1	1	Reserved

The Software Reset code is executed as a command when it is written to the Mode Register to clear an existing operating mode. This causes any current operation to be terminated (except Dynamic RAM Refresh). Certain internal scratch registers are initialized and the band control logic is cleared to Band 0. A Software Reset is normally issued after each full page is printed. Band-buffer systems may be setup to alternate bands continuously as subsequent pages are printed and then reset is not required.

The RPC maintains current page and reference registers to be used in address calculations. Software Reset, as well as activating the $\overline{\text{RESET}}$ pin, causes these values to be cleared so that the next sequence of Dispatching and Scan-out begins at the top of Video Memory space. Software Reset must be issued after each page is printed to control the limit of physical memory space in a single full-page buffer system. It does not alter the contents of any of the programmable address registers.

Video Polarity is selected by bit 12 of the Mode Register. This bit is reset to zero to specify that a HIGH level on the Video Data Out (VDO) pin indicates a black image and a LOW level indicates a white image. VP is set to a one to specify that a HIGH level indicates white and a LOW indicates black. Regardless of the setting of the VP bit, the VDO pin is driven HIGH when the printer is outside the printable area defined by the page size, or when printing is idle.

Bit 11 of the Mode Register is the Video Refresh Enable bit. It is cleared when the $\overline{\text{RESET}}$ pin is activated or by writing to the Mode Register with a zero in that bit. The Video Refresh Rate Register should be initialized before VRE is set. If VRE is cleared by writing the Mode Register, only a Refresh cycle currently in progress would be completed.

Bit 10 of the Mode Register is the Interrupt Enable bit. In order for the RPC to activate the Interrupt pin, the IE bit must be set. Clearing IE will cause $\overline{\text{INTR}}$ to go inactive if an interrupt was currently pending.

The Multiple Print Control is bit 9 of the Mode Register. This bit is zero in the normal case where each page is printed once. The RPC normally performs read-modify-write cycles on the Video Memory for scanning out the pixel data to be printed. This allows "white" to be written back to each memory word in order to erase each page in preparation for the next. If MPC is set, a memory read cycle is used to allow the same page to be scanned out multiple times. The MPC bit must be cleared before the last printing of a page to clear the buffer. MPC can only be used in systems with a full-page buffer. Writing the Mode Register to set MPC and RC should not be done while Dispatching is in progress. MPC should be set at the beginning of page assembly or some time before RC to ensure that it is recognized the first time the page is printed. When the video bands are configured as two full page buffers, MPC should must be set before the dispatch of the first page or before the dispatch of the second page.

Printing is enabled by setting the Raster Control, bit 8 of the Mode Register. RC should not be set until at least the first band of the page has been Dispatched so that the first words of the first scan line can immediately be fetched for loading into the shift register. Once this pixel data is ready to be serialized onto the VDO pin, the RPC can recognize a PSYNC input. Otherwise, PSYNC and LSYNC are ignored.

RC is cleared by the RPC when the printing of a page is complete. RC is also cleared by a Raster Incomplete error condition. If RC is cleared by writing the Mode or the $\overline{\text{RESET}}$ pin, a printing operation in progress will be terminated and cannot be restarted mid-page. Setting RC by writing the Mode will not take effect if the EOP flag is set. This allows Mode changes during printing without erroneously starting a new page.

The low byte of the Mode Register contains status information that cannot be modified by a write access, unless Software Reset is selected in the Mode Control field. This will clear all status flags and deactivate any interrupt condition that was pending.

End-of-Page is indicated by bit 7 of the Status byte. This occurs when the printing of a page is complete as determined by the X and Y Margin and Size values that were programmed into the RPC. EOP causes the Interrupt pin to be activated and is cleared when the Status Register is read.

Bit 6 of the Status byte indicates a Raster Incomplete error condition has been detected. This occurs when the LSYNC input is activated and the current scan line has not been completely serialized to the printer as programmed in the Page X Size Register. This condition cannot be recovered from and may be due to incorrectly programmed X Size or insufficient VCLK frequency. RI causes an interrupt and clears RC.

Bit 2 of the Status byte is the Band Dispatched flag. This flag is activated when the destination of a Dispatch operation equals or exceeds the Video Band Boundary of the current band. The RPC will not dispatch this character but rather, will interrupt to provide an opportunity to

eration equals or exceeds the Video Band Boundary of the current band. The RPC will not dispatch this character but rather, will interrupt to provide an opportunity to dispatch any partial characters to the next band first. A second Dispatch operation (of the same or different character) into the next band will cause the RPC to complete the dispatch. See the section on Video Bands for additional information on band control.

Bit 1 of the Status byte is the Dispatch Complete flag. This bit indicates that the last Dispatch or ORP Operation completed transferring the entire image block. This condition does not cause an interrupt and is intended for use in systems that poll status after each Dispatch to determine when the next operation may be started. When DC is set the RPC will also activate $\overline{DRQ}$.

Dispatch Incomplete is indicated by bit 0 of the Status byte. This occurs when the image block being dispatched extends beyond the Video Band Boundary of the current band. The RPC stops the Dispatch at that point and generates an interrupt. The SAR, TAR and DAR registers for the remaining partial character may be read from the RPC for use when the next band is being dispatched. See Video Bands for more information on handling sliced characters.

Margin Register

The Margin Register, at Port 2, holds the least significant 8 bits of the X Margin in the high byte and the least significant 8 bits of the Y Margin in the low byte. The Memory Timing Register at port 7 holds the two most significant bits for each of the margins. Together, these registers allow up to 1,023 pixels in the X direction and 1,023 lines in the Y direction for margin area that will always be scanned out before the printable area begins.

Page X Size Register

The Page X Size Register is at Port 3. This specifies the number of pixels in the printable area of a scan line, not including the X Margin. A full 16-bit value is supported.

Page Y Size Register

The Page Y Size Register is at Port 4. This specifies the number of lines in the printable area of a page, not including the Y Margin. A full 16-bit value is supported.

Video Band Boundary Register

The 16-bit word at Port 5 plus the low byte of Port 6 comprise the Video Band Boundary. Bit 7 of the byte at Port 6 is the most-significant bit of this 24-bit address. The Video Band Boundary points to the word address of the beginning of the second band in Video Memory space. The beginning of the first band is always 0 and bands must start on a line boundary, which is internally calculated using the PXSR rounded up to a multiple of 16 pixels. For a full-page buffer system, the Video Band Boundary must be set to a value greater than the size of the page.

Video Memory Refresh Rate Register

The register at Port 6 holds the Video Memory Refresh Rate in the high byte and the most-significant 8 bits of the VBBR in the low byte. The VMRR specifies the number of CLK cycles that will elapse between dynamic memory refresh cycles if refreshing is enabled by the VRE bit in the Mode Register. The value programmed will depend on the refresh interval of the memory chips used and the frequency of the CLK input.

Memory Timing Register

The Memory Timing Register at Port 7 contains control information for the Video and Font Memory interfaces, in addition to the two most-significant bits for the X and Y Margins. This register must be programmed before any memory or printer operations are used. The MTR is not cleared by $\overline{RESET}$. See Figure 3 for the bit position assignments of this register.

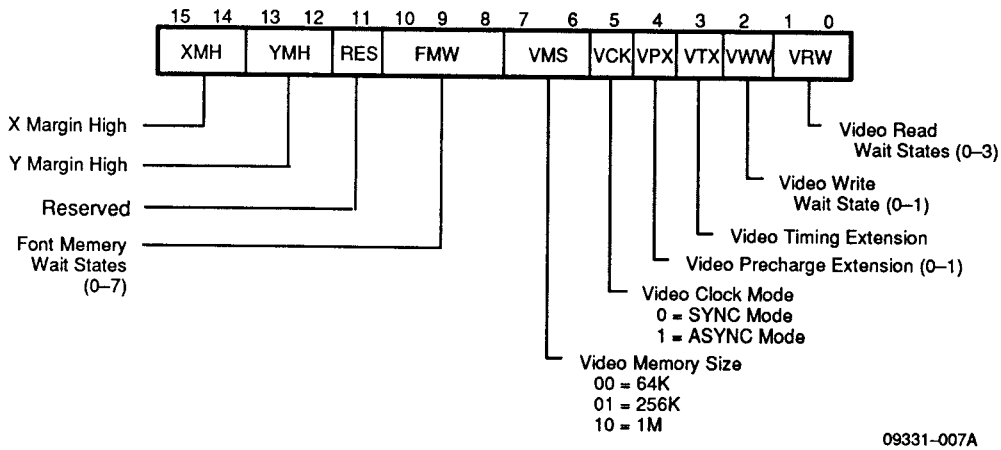


Figure 3. Memory Timing Register

Bits 15 and 14 of the MTR correspond to bits 9 and 8 respectively, of the X Margin value. Bits 13 and 12 correspond to bits 9 and 8 respectively, of the Y Margin value. These bits must be loaded with zeros if the margin values are less than 256.

Bits 10, 9 and 8 form the Font Memory Wait States field of the MTR with bit 10 being the most significant bit. This provides for 0 to 7 wait states to be inserted into every Font Memory cycle. Wait states extend T2 (see Font Memory Timing diagrams) of the cycle to extend $\overline{FRD}$ and $\overline{FWR}$ as required by the static memories. Bits 7 and 6 of the MTR form a 2-bit field that is used to select the Video Memory Size. This is determined by the type of dynamic RAM chips that are used for the Video Memory. The options, 64K, 256K and 1M, result in differences in how the Bank Select, Row address and Column address are output on the VAD bus during address cycles. Table 3 defines the use of the VMS field.

Table 3. VMS Control Field

MTR 7	6	DRAM	Bank Address	Row/Col Address
0	0	64K	VAD_{15}–VAD_8	VAD_7–VAD_0
0	1	256K	VAD_{15}–VAD_9	VAD_8–VAD_0
1	0	1M	VAD_{15}–VAD_{10}	VAD_9–VAD_0
1	1	Reserved		

Bit 5 of the MTR determines the VCLK mode for printing operations. If this VCK bit is a zero, Synchronous mode is selected. This means that the LSYNC input must change synchronously to the VCLK and meet the setup time specified. In this mode the pixel rate equals the VCLK rate. If the VCK bit is a one, Asynchronous mode is selected and LSYNC does not need to have any timing relationship to VCLK. In Asynchronous mode the VCLK is divided by four to determine the pixel rate.

An important feature of the RPC relates to Asynchronous mode. The internal synchronization of LSYNC can result in some variation in the position of the starting pixel of successive scan lines, relative to VCLK. In order to minimize this variation, the RPC attempts to detect the rising edge of LSYNC during both phases of VCLK and starts the VCLK divider on the phase it is detected. This limits the variation to one eighth of a pixel due to the divide by four of the VCLK rate. A VCLK frequency of up to 32 MHz may be used in this Asynchronous mode.

The Video Precharge Extension option is selected by bit 4 of the MTR. When VPX is a zero, the minimum dynamic RAM precharge time, when $\overline{VRAS}$ and $\overline{VCAS}$ are inactive, is nominally 1.5 CLKs. (See AC Timing Specifications to determine exact values.) If VPX is set to one, an additional CLK cycle is inserted into the minimum precharge time. This may be required for some RAMs.

An optional Video Timing Extension cycle is selected by bit 3 of the MTR. When VTX is set to one, an additional CLK cycle is inserted after the Row address cycle of each memory access. During this cycle the Row address is held valid on the VAD bus and the falling edge of $\overline{VCAS}$ is delayed to the next CLK cycle. This may be used to provide additional time for bank select decoders. The VTX bit does not affect the timing of memory Refresh cycles.

Bit 2 of the MTR is the Video Write Wait State bit. When set, it allows one wait state to be inserted to extend T3 of a Video Memory Write cycle and to extend T5 of a Read-Modify-Write cycle. This extends $\overline{VWE}$ and VAD Data Out by one CLK. This may be required for some RAMs.

Bit 1 and 0 of the MTR form the Video Read Wait States field. The VRW allows 0 to 3 wait states to be inserted to extend T2 of Video Memory Read and Read-Modify-Write cycles. This extends $\overline{VR}$ and delays the requirement for valid Data In on the VAD bus. Bit 1 is the most-significant bit of this field that is encoded to correspond to the number of waits desired.

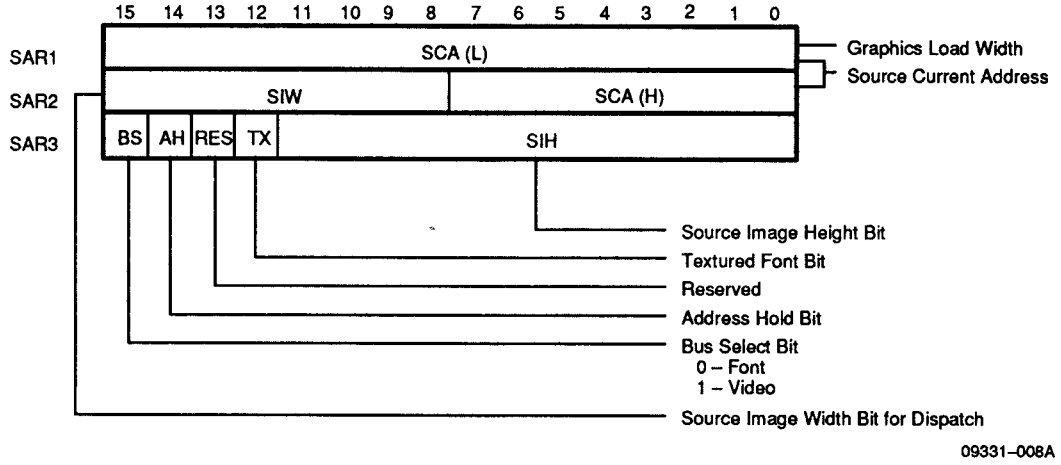


Figure 4. Source Address Register

Source Address Registers

The Source Address Registers provide information for Dispatch operations. This information is assumed to be correct when the Dispatch is initiated by loading DAR2. Additionally, SAR1 is used for the width in a Graphics Load operation.

The first word of the Source Address Registers holds the lower 16 bits of the current Source Address (Figure 4). The upper 8 bits of this 24-bit address are held in the low byte of SAR2. Since the Source Address is updated as an operation progresses, reads of SAR1 or SAR2 may not return the original value. This is essential for handling sliced characters. The high byte of SAR2 holds the value of the Source Image Width in words for a Dispatch. This allows images from 16 to 4,096 pixels wide. SAR1 must be loaded with the width in words for a Graphics Load operation wherein the address is contained in the DAR. The width value does not change during an operation.

The lower 12 bits of SAR3 hold the Source Image Height, which can be from 1 to 4,096 scan lines. The height value is updated like the address during an operation to handle sliced characters. The remaining upper bits of SAR3 hold control information.

Bit 15 of SAR3 is the Bus Select bit for the source of the character in a Dispatch operation. When this bit is a zero, the character is loaded from the Font Memory. When it is a one, the character is loaded from the Video Memory.

Bit 14 of SAR3 is the Address Hold bit. When this bit is set, the source address for a Dispatch operation is not incremented. This allows a single word to be transferred repeatedly to create a block at the destination that is filled with a pattern, or allows a source to be read from a fixed location like the ORP.

Bit 12 of SAR3 is the Textured Font bit (TX). When this bit is set, a Textured Dispatch operation is performed. The Texture Address Registers must be loaded with valid information. The RPC will sequence through the TAR locations when automatically loading the parameters for a Dispatch that are being written to Port 0 if the TX bit is detected in SAR3. During Dispatch, two read cycles will be performed to load the Font word (first) and the Texture word (second), and then a read-modify-write cycle will merge the Font, Texture and background at the Destination Address. The Font and Texture can be in any combination of Font Memory or Video Memory, but the Destination of a Dispatch is always the Video Memory. Due to the additional read cycle, the performance of a Textured Dispatch may be less than non-textured, depending on how the memory cycles are programmed.

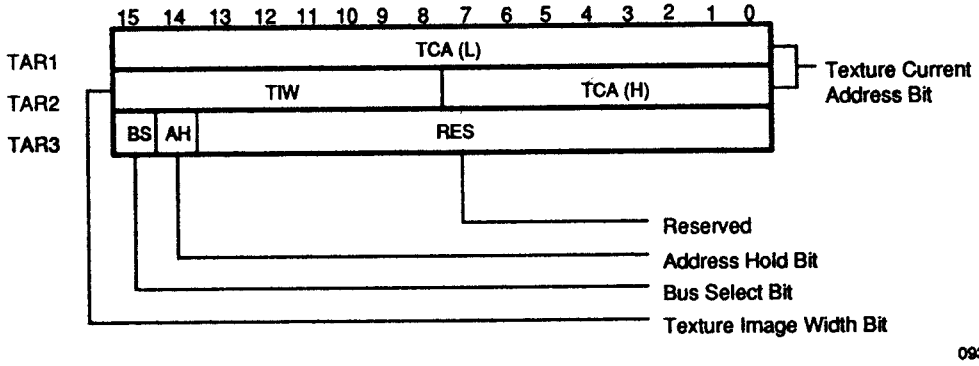


Figure 5. Texture Address Registers

Texture Address Registers

The Texture Address Registers are organized the same as the SAR words, however TAR3 contains less information (Figure 5). TAR1 holds the lower 16 bits of the current Texture Address and the low byte of TAR2 holds the upper 8 bits of this 24-bit address. The high byte of TAR2 holds the Texture Image Width which must be at least equal to the Source Image Width. In TAR3, only the two most significant bits are used.

Bit 15 of TAR3 is the Bus Select bit for the Texture. When this bit is a zero, the Texture is loaded from the Font Memory. When it is a one, the Texture is loaded from the Video Memory.

Bit 14 of TAR3 is the Address Hold bit. When this bit is set, the Texture Address for a Dispatch is not incremented. This allows a one word texture to be repeatedly applied to a character of any size.

The remaining lower bits of TAR3 are not used. A Texture Image Height is not required because the Source Image Height is used for determining the height of the block to be Dispatched. A Texture array must be as high as the largest character it is intended to be applied to. When setting up a Dispatch operation, the DAR must be the last two words programmed regardless of whether they were preceded by the SAR or TAR.

Destination Address Register

The Destination Address Registers are used in all of the RPC operating modes (Figure 6). While the SAR and TAR are predominantly used for only Dispatch, the address information for Font Load, Font Read, Graphics Load and the ORP modes is held in the DAR. It should be noted that the address for a Font Read is actually a "source" address, but the DAR is used to make programming consistent.

5

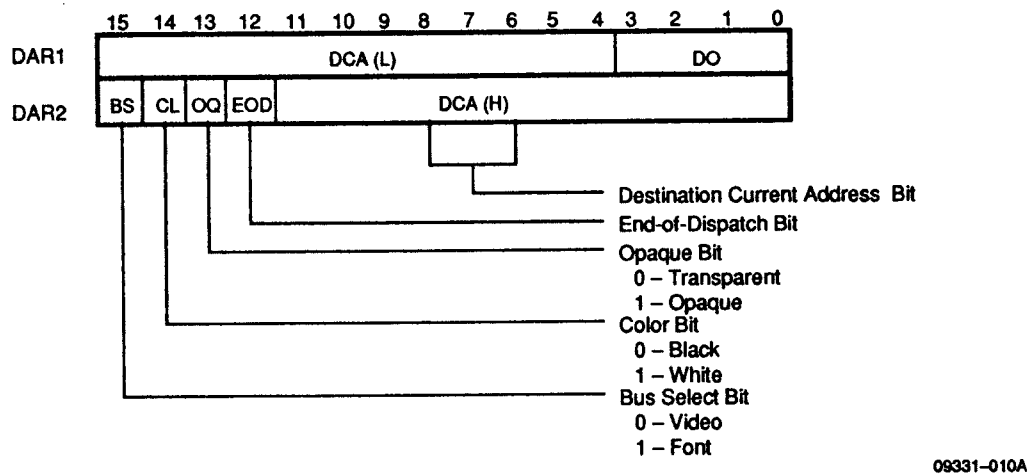


Figure 6. Destination Address Registers

DAR1 holds the lower portion of the Destination Address. In Dispatch and Graphics Load modes, the address is a 28-bit value to provide arbitrary pixel alignment of the words being transferred. The four least significant bits hold the Destination Offset field of DAR1, and provide the 0 to 15 pixel displacement for the starting point of pixel data for each destination word. Consequently, the 16 bits of DAR1 provide the lower 16 bits of the address in these two modes.

In Font Load, Font Read and ORP modes, DAR1 holds the lower 12 bits of the 24-bit address value in bits 15 through 4. Since the transfers in these modes must be word aligned, the four least-significant bits of DAR1 must be loaded with zeros.

DAR2 holds the most significant 12 bits of the Destination Address in the lower 12-bit positions of the word. This is the case for either a 24-bit or 28-bit address. The four most-significant bits of DAR2 hold control information for the current operation. Since the Destination Address is updated as the operation progresses, reads of DAR1 or DAR2 may not return the original value.

Bit 15 of DAR2 is the Bus Select bit. Font Load and Font Read modes may select either Font Memory or Video Memory space. When the BS bit is zero, Video Memory is selected. When it is a one, the Font Memory is selected. For Dispatch, Graphics Load and ORP modes, the BS bit is ignored. The destination for Dispatch and Graphics Load is always Video Memory. The ORP must reside on the Font Memory interface.

Bit 14 of DAR2 is the Color bit (CL). It is used to select whether the active area of a character is printed as black or white. When CL is zero, the character will be black. When CL is one, the character will be white.

Bit 13 of DAR2 is the Opaque bit (OQ). It is used to select whether the inactive area of a character is transparent or opaque. When OQ is zero, the space around the character is transparent and any existing background information will show through. When OQ is a one, the space around the character is opaque and will white-out any existing background. OQ must be a one for Font Load mode.

When both the CL and OQ bits are set, the inactive area around a character will be printed as black. This will black-out any existing background information. See the Video Operations Table for details.

The CL and OQ bits are effective only in Dispatch and Graphics Load modes. These two operations always generate read-modify-write cycles on the destination in Video Memory, so the background information can be preserved if appropriate. They also generate an extra cycle and mask portions of each word according to the Destination Offset. Font Load mode, even to the Video Memory, does a single aligned write cycle, so the offset must be zero and the OQ bit must be a one.

Bit 12 of DAR2 is the End-of-Dispatch bit. The presence of this flag overrides all other information in the SAR, TAR and DAR registers, and triggers an internal operation in the RPC. This sequence indicates that the last Dispatch of a page has been completed. This allows the next Dispatch operation to begin the next page, even if multiple blank bands are required to complete printing of the current page. The RPC will automatically shift out "white" pixels until the correct Page Y Size is reached.

The EOD flag may be set by explicitly writing the DAR to Ports 14 and 15, or by writing a "dummy" Dispatch sequence of the five words of SAR and DAR to Port 0. The RPC automatically initiates an operation after DAR2 is written. In the EOD case, it will be the internal operation that sets up for the next band and adjusts internal registers. DAR1 and DAR2 should both be written to ensure that the DMA Request output is controlled correctly. The next $\overline{DRQ}$ may not occur until printing has progressed to the band marked by the EOD.

Table 4. Video Operations

Case #	OQ Bit	CL Bit	TX Bit	Source Pixel	Texture Pixel	Background Pixel	Result Pixel
1	0	X	X	0	X	0	0
2	0	X	X	0	X	1	1
3	X	0	0	1	X	X	1
4	X	0	1	1	0	X	0
5	X	0	1	1	1	X	1
6	X	1	0	1	X	X	0
7	X	1	1	1	0	X	1
8	X	1	1	1	1	X	0
9	1	0	X	0	X	X	0
10	1	1	X	0	X	X	1

Notes:

Case 1 and 2: *Background shows through transparent inactive pixel*
Case 3: *Normal active pixel*
Case 4 and 5: *Texture overwrites active pixel*
Case 6: *CL reverses active pixel*
Case 7 and 8: *CL reverses texture that overwrites active pixel*
Case 9: *OQ causes inactive pixel to overwrite background*
Case 10: *CL and OQ reverses inactive pixel and overwrites background*

Operating Modes

The RPC performs six operating modes to support the transfer of pixel data among the memory resources of a printing system. These modes may be used to obtain capabilities and performance beyond the range of a general purpose processor executing the same tasks. Working jointly with a host processor, the RPC frees the host from the heavy data transfer burden, and allows it to perform higher level tasks for which it is better suited. Together, the RPC and host CPU can implement the most sophisticated features of an advanced printing system.

The fundamental operation for which the RPC is optimized is the transferring of stored rectangular image blocks to the page buffer. This is Dispatch mode and a number of options are available to augment it. In addition, three modes are provided to allow transfers of data between system memory space and the two memory interfaces controlled by the RPC. Graphics Load mode allows rectangular image blocks to be written to the page buffer with the same overlay options as Dispatch. Font Load and Font Read modes allow data to be transferred for storage and retrieval in a sequential word manner. ORP Load and ORP Read modes allow the RPC to efficiently work with the Am95C76 ORP to rotate image blocks in the process of assembling the page buffer.

Dispatch Mode

Dispatch is selected by writing 011 to the Mode Control field. Then in order to initiate a Dispatch, the CPU must load the Source Address Registers (SAR1-3) and Destination Address Registers (DAR1-2) and optionally the Texture Address Registers (TAR1-3) if texturing is desired. Loading these address registers may be done by writing to the explicit port location for each one or by writing them in sequence to Port 0. The sequence is SAR-DAR (five words) or SAR-TAR-DAR (eight words) for a textured Dispatch. The TAR words must be inserted if the Textured Font bit (TX) in SAR3 is set. The DAR words must be written last to deactivate the $\overline{DRQ}$ pin and trigger the start of the Dispatch operation.

The Source image and texture may be stored in either Font or Video Memory independently, as selected by their respective Bus Select (BS) bits. They will be read from consecutive word locations unless Address Hold (AH) is selected for either. AH is useful for area fill or for one-word textures. The texture addressing will not always be for consecutive memory locations if the Texture Image Width is greater than the Source Image Width. In this case, a new line of texture will be started with each new line of the Source image so that it will be consistently applied to images of varying size. Bit 15 of each image data word is assumed to be the left-most pixel and bit 0 is the right-most as they are read from the storage area.

The destination for Dispatch is always Video Memory. A Dispatch operation does not need to be word aligned, as the DAR provides a 28-bit address where the four least significant bits of DAR1 are an offset to indicate the position of the starting pixel in each word. Read-Modify-Write cycles are performed on the Video Memory words, the new image data is shifted as needed and any partial words outside the sides of an image block are masked so they remain unchanged. Dispatching progresses from left to right and top to bottom. The width must be specified in words and the image block must fit in the available Page X Size rounded up to a multiple of 16 pixels. (The block can't extend beyond the right side of the page.)

The data options for a Dispatch are controlled by the TX bit in SAR3 and the Color (CL) and Opaque (OQ) bits in DAR2. When TX is set, the RPC reads the first word of the Source image followed by the first word of the Texture. Then the first RMW cycle is performed at the Destination. This may modify a full word or partial word depending on the offset. This sequence allows the image, texture and any background information in the Video buffer to be combined. When the BS bits in SAR3 and TAR3 are both zero, indicating Font Memory, the read accesses after the first can occur in parallel with the Video Memory cycles to achieve higher performance. If the Font is stored in Video Memory, accesses can not occur in parallel. If only the Texture is stored in Video Memory, Font accesses can still be in parallel. Without texturing, the highest performance is obtained since one access is eliminated.

When a Dispatch operation completes, the Dispatch Complete (DC) bit in the Status is set and the $\overline{DRQ}$ pin is activated to request the next Dispatch. ($\overline{DRQ}$ can only be activated when the RPC is in Dispatch or ORP modes.) In cases where a Dispatch cannot complete normally, the $\overline{INTR}$ pin is activated. These interrupt conditions may be used for systems where the Video buffer is divided into two bands.

Video Bands

The RPC provides full support for systems having a Video Memory space that is much less than a full page. These features can also be used in systems having two full page buffer areas since the total memory space is limited only by the 28-bit address of the DAR. When the Video buffer is divided into two bands, Dispatching can be in progress in one band while printing is supported from the other band that has already been Dispatched. The bands alternate function in this manner until a page, or multiple pages are complete. This approach allows printer performance that may be limited only by the pixel rate of the print engine.

Since printing can be enabled by setting the Raster Control bit (RC) in the Mode register as soon as the first band is Dispatched, it is essential that all full or partial characters in the first band are completely Dispatched before the second band is begun. Each subsequent band of the page must be fully Dispatched in the time it takes to print the previous band, and Dispatching cannot progress into the next band until the printing of its previous contents is complete. The band control logic of the RPC will ensure that the printer is supplied with a con-

tinuous flow of pixels and that Dispatching is held off if necessary.

The first band will always start at location 000 0000 Hex in Video Memory, which corresponds to the upper left corner. The size of the two bands is determined by the value programmed in the Video Band Boundary (VBB). This value must be the address of the first word of the second band. During Dispatch of the first band, the RPC compares the current destination address to the VBB. If it is greater than or equal to the VBB, the Dispatch is stopped, the Dispatch Incomplete (DI) flag is set and $\overline{INTR}$ is activated.

The DI interrupt must be processed by the host CPU to handle the cases of characters that were sliced by the band boundary. This requires reading the contents of the SAR, TAR (if used) and DAR, and saving this information in a sliced character table in system memory. These partial characters can be Dispatched into the next band after the current band is complete. In the DI case, the $\overline{DRQ}$ pin is activated for the next Dispatch after DAR2 is read. The remaining full or partial characters are Dispatched to the current band and DI is activated whenever a sliced character is detected.

When the starting address for a Dispatch equals or exceeds the current band boundary, the operation is not initiated, the Band Dispatched (BD) flag is set, the current Band for Dispatching is toggled and $\overline{INTR}$ is activated. This provides the opportunity to Dispatch any entries in the sliced character table to the new band. The BD interrupt will be delayed if the previous data in the new band has not been completely scanned out to the printer. After BD is set, the second attempt to Dispatch into the new band will be accepted. If there are no sliced characters pending, the address for the first whole character of the new band should be sent a second time. (Actually only the DAR words need to be rewritten to trigger the Dispatch.)

The RPC calculates the current band boundary from the VBB and automatically converts the DAR provided into the correct physical memory address for the current band. Characters need only be sorted according to the virtual address on the full page. Each horizontal line of a character is maintained in the correct position according to the Image Width and the Page X Size Register.

After the last Dispatch of the band that has the last characters on a page, one final set of DAR words must be written to the RPC with the End-of-Dispatch (EOD) flag set. This may be accomplished by writing to Ports 14 and 15 explicitly, or by sending a dummy Dispatch sequence to Port 0. When EOD is detected, the rest of the registers are ignored and an internal operation is executed. This marks the band as the last of a page and allows the next Dispatch to begin a new page without causing any interrupts. The current page may contain multiple blank bands after the one marked by EOD. The RPC will automatically scan out "white" until the Page Y Size Register indicates that the page is complete. Dispatching of the first band of the next page does not have to be delayed to accomplish this.

In a system with a single full-page buffer, an EOD sequence is not required. Instead, printing can be enabled after the last Dispatch of the page. After printing is complete, as indicated by the End-of-Page interrupt, a Software Reset must be written to the Mode Register. This causes internal registers to be adjusted so that the next page will begin at the top of Video Memory space. Then Dispatch mode can be reselected and the next page can be started.

Graphics Load Mode

Graphics load is selected by writing 110 to the Mode control field. Then SAR1 must be loaded with the correct Image Width in words, and the DAR must be loaded with the 28-bit address of the upper left-hand corner of the destination. A Graphics Load block does not have to be word aligned. The four least significant bits of DAR1 are an offset to indicate the position of the starting pixel in each word. Each memory cycle to the destination in Video Memory is triggered by a CPU write of image data to the Temporary Register at Port 0. The RPC performs Read-Modify-Write cycles so the Graphics block image may be combined with any existing background information, according to the CL and OQ bits of DAR2, in the same manner as Dispatch.

Graphics Load progresses from left to right until the number of words indicated by the Image Width have been written. Then the RPC calculates the start of the next horizontal line of the block according to the Image Width and the Page X Size Register, and continues with the sequence of image words being received from the CPU. Lines will continue from the top down until the CPU stops writing to Port 0. If the DAR offset is not zero, the last word written by the CPU should complete a horizontal line. If a partial line is desired, the last portion of the last word written mid-line will not be transferred to Video Memory unless one more word is written by the CPU. This extra word should be blank.

Graphics Load is effectively terminated when the CPU programs any new operation. There is no inherent Image Height required. The starting DAR is assumed to be the physical memory location desired and no address conversion is performed to adjust for the current Video Band like a Dispatch. Graphics Load can be used among Dispatch operations as long as the image block fits in the current band and the DAR provided is the correct physical memory address. This should always be the case in a full-page buffer system.

Video Data Operations

In Dispatch and Graphics Load the CL and OQ options determine how the image is combined with the background. When CL is zero, the active area of a character is printed as ones, or black. When CL is a one, the character is printed as zeros, or white. When OQ is zero, the inactive pixels of an image block will be transparent and allow any background information to show through. When OQ is a one, the inactive pixels will white-out any background information. If both CL and OQ are set, the normal resultant pixels (i.e., when CL equals zero and OQ equals one) get reversed. The active pixels of a

character will become zeros unless they are to be textured and the texture pixel is a zero, then they will be ones. The inactive pixels of the block will become ones and effectively black-out any background. Table 4 shows the result for all combinations of data and options.

Font Load Mode

Font Load Mode is used for storing information from the CPU to Font Memory or Video Memory. It is selected by writing 100 to the Mode Control field. The DAR must be programmed with a 24-bit address and the Bus Select bit must be zero to indicate Video Memory or one to indicate Font Memory. Since Font Load performs word aligned write cycles to the destination, the OQ bit must be a one and the CL bit and the offset field must be zeros.

Font Memory write cycles are triggered each time the CPU writes to the Temporary Register at Port 0. The Destination Address is incremented after each write cycle. The operation ends when the CPU stops writing data to Port 0, or a new operation is programmed. The DAR may be changed as needed for multiple Font Load operations.

Font Read Mode

Font Read Mode allows the CPU to access stored information in either the Font Memory or the Video Memory. It is selected by writing 101 to the Mode Control field. The DAR must be programmed with a 24-bit address for the first word to be read and the Bus Select bit must be zero to indicate Video Memory or one to indicate Font Memory. The CL, OQ, and offset field are ignored.

As soon as DAR2 is loaded, the RPC reads the first word into the Temporary Register and waits for the CPU to read it out. Each access of Port 0 by the CPU causes the DAR to be incremented and another word to be read from Font or Video Memory. The CPU can read as many words as desired, change the DAR or program a new operation as needed.

ORP Load Mode

ORP Load Mode allows the RPC to load data from the Font Memory to the Am95C76 for character rotation. It is selected by writing 010 to the Mode Control field. SAR1 must be programmed with a word count that is the exact number of words to be loaded into the ORP. The DAR must be loaded with the 24-bit address for the first word to be loaded. When DAR2 is loaded, the RPC executes a continuous stream of Font Memory read cycles until the word count reaches zero. BS, CL, OQ, and the offset in the DAR are ignored. The data can be strobed into the ORP and is of no consequence to the RPC. When the word count in SAR1 has been decremented to zero, the RPC will set the DC bit and activate the $\overline{\text{DRQ}}$ pin to request the next operation. The CPU can alternate ORP Load and Dispatch operations in order to transfer rotated characters to the Video buffer.

ORP Read Mode

ORP Read Mode allows the RPC to read rotated data from the ORP to be stored in Font Memory. It is selected by writing 001 to the Mode Control field. SAR1 must programmed with the word count and the DAR must be loaded with the 24-bit address of the destination of the first word. Loading DAR2 triggers a continuous stream of Font Memory write cycles until the word count reaches zero. The RPC does not drive any data onto the FAD_0-FAD_{15} bus during the $\overline{\text{FWR}}$ strobe. This is provided by the ORP in the proper sequence. The DC bit and the $\overline{\text{DRQ}}$ pin are activated as in ORP Load.

5

Printer Operation

The RPC provides a number of programmable options in order to easily interface to a variety of print engines and accommodate a broad range of page sizes. This information must be programmed into the appropriate Operation Control Registers (OCR) before printing is initiated. Some of the OCR words are required to execute memory operations and it is recommended that the entire OCR be loaded after the power-up and Reset. This is best accomplished by loading the Memory Timing Register (MTR) at Port 7 first, and then continuing in descending order to the Mode at Port 1. This insures that the Refresh Rate will be setup before Refresh is enabled and that all other options are correctly initialized. Page Size and Margin values may be altered as needed for different pages but this must be done before any Dispatching or Graphics Load operation is started.

In most systems an Opaque Dispatch operation should be used to initially clear the entire Video Memory buffer. The SAR can be held pointing to an all zero word. Since the maximum size of a Dispatched block is 4096 x 4096 pixels, several operations may be required. Once this is done after power-up, The RPC will automatically clear the buffer area after each page is printed, unless the Multiple Page option is used.

The Printer Interface may be operated in either Synchronous or Asynchronous Mode, depending on how the print engine timing generates LSYNC relative to VCLK. If the rising edge of LSYNC occurs synchronous to VCLK and meets the setup time required, SYNC Mode can be used and the pixel rate on the VDO pin will equal the VCLK rate. If LSYNC has no fixed timing relationship to VCLK, ASYNC Mode should be used and the pixel rate will be the VCLK rate divided by four. PSYNC needs no fixed timing relationship to VCLK, but the rising edge of PSYNC must precede LSYNC by a minimum of one VCLK so the Y Margin may be evaluated. The printer mode is selected by the VCK bit in the Memory Timing Register at Port 7.

The polarity of the VDO output is selected by the Video Polarity (VP) bit in the Mode Register. When VP is a zero, VDO outputs a HIGH level to indicate a black (active) pixel and a LOW level to indicate white. When VP is a one, VDO outputs a LOW for black and HIGH for white. In any case, VDO is driven HIGH when printing is idle or printing is outside the active page area defined by the page size.

Printing cannot be initiated until the Video buffer has been prepared with the first page or band using Dispatch or Graphics Load. Once this has been done, the Raster Complete (RC) bit in the Mode Register may be set and the RPC will load the internal shift register for the VDO output with the first word from Video Memory location 000 0000 hex. Normally Read-Modify-Write cycles are used to support scan-out, so that each word is written with zeros as scanning progresses in preparation for the next band or page. If the MPC bit is set in the Mode Register, read cycles are used for scan-out so that the same full page can be printed more than once. MPC should be set in advance of RC, or it can be set with RC if there is no memory operation in progress.

The RPC provides two interrupts to simplify the control of printing. The End-of-Page flag in the Mode/Status Register is set and the $\overline{\text{INTR}}$ pin is activated when a number of lines equal to the Page Y Size Register have been shifted out on VDO. The RC bit is automatically cleared at this time. This interrupt can be used to control when the next page is started or when the Multiple Print Control bit (MPC) should be cleared before the last printing of a single page that was printed multiple times. RC cannot be set if EOP is active.

The Raster Incomplete (RI) flag indicates an error condition during printing that cannot be recovered from. RI is set when an LSYNC is detected in the middle of an active scan line. LSYNC cannot be accepted until a number of pixels equal to the programmed Page X Size have been scanned out. RC is cleared if RI is set and the RPC must be programmed to start over on a page after the cause of RI has been determined.

System Interface

The System Interface of the RPC can be operated completely asynchronously to the CLK input. Accesses by the host CPU or external DMA controller may be made at any time and will be internally synchronized by the RPC. The RDY output will be driven inactive if the access cannot be immediately completed.

During Dispatch or ORP modes, the $\overline{DRQ}$ output can be used to control when the RPC is ready for the next operation to be programmed. $\overline{DRQ}$ will be driven active after each operation is completed or when a DI or BD interrupt has been handled. Alternatively, Status may be polled to determine when each Dispatch is complete by testing the DC flag. Status flags are only cleared after Status is read, so DC can stay active through multiple Dispatches. The RDY output may be used to extend CPU accesses until the RPC is able to accept new information, but this may be a long time during a large Dispatch and care must be taken not to modify essential values in the middle of an operation. The Mode/Status Register is always accessible to the CPU but some changes to control bits may not take effect immediately if an operation is in progress. Software Reset and changes to RC are always recognized.

Font Interface

Font Memory cycles may be programmed for automatic insertion of wait states by the FMW field of the MTR. During Dispatch, Font cycles may skip the upper address cycle and FALE2 if it does not need to be updated. This is done to improve performance.

When the Am95C76 ORP is used, it must reside in Font Memory space. The ORP may be programmed or accessed by using Font Load and Font Read modes to the locations reserved for it. ORP Loads and Dispatch operations may be alternated so that rotated characters may be assembled into the page buffer as desired.

Video Interface

The timing for Video Memory cycles may be programmed by several fields in the MTR register at Port 7. The Video Memory Size (VMS) field selects the type of Dynamic RAM that is used in the Video buffer in order to provide the correct combination of Row and Column addresses and bank select bits. The Video Precharge Extension (VPX) bit increases the precharge time when $\overline{VRAS}$ and $\overline{VCAS}$ are inactive by one CLK if needed by the RAMs. The Video Timing Extension (VTX) bit increases the Row address hold time by one CLK to allow for bank decoding if needed by the memory system.

The Video Write Wait State (VWW) bit and the Video Read Wait State (VRW) field allow wait states to be automatically inserted to extend Video Memory cycles to match the performance of the Dynamic RAMs used. For details on wait states see the MTR register description and the Video Memory cycle timing diagrams.

RESET

The $\overline{RESET}$ pin must be activated by the system after power-up. This causes an internal operation that initializes scratch registers that are used for calculation of memory addresses. In addition, the Mode Register is cleared. All other user-accessible registers must be properly initialized before any RPC operations are started. The Video buffer must be cleared by programming appropriate Dispatch operations. $\overline{RESET}$ will always terminate any operations in progress including Refresh of the Video Memory.

A Software Reset operation may be executed by changing the Mode Control field to 000 from any other value. This will terminate an operation in progress and initialize internal scratch registers to begin a new Dispatch in Band 0, and begin printing at the top of Video Memory space. Software Reset will not alter the setting of the VP, VRE or IE bits in the Mode/Status Register and dynamic memory Refresh will not be interrupted.

5

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Ambient Operating Temperature	–55 to +125°C
Maximum V_{cc} Relative to V_{ss}	–0.3 to +7.0 V
DC Voltage Applied to Any Pin Relative to V_{ss}	–0.5 to Vcc+0.3 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{cc})	+4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges

Parameter Symbol	Parameter Descriptions	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		–0.3	0.8	V
V_{IH}	Input HIGH Voltage	CLK Input only	+2.0	V_{CC}+0.3	V
		All other inputs	+2.0	V_{CC}+0.3	V
V_{OL}	Output LOW Voltage	I_{OL}= 8.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH}= –5.0 mA	+2.4		V
II	Input Leakage Current	0.4 ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	0.4 ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{CC}	Power Supply Current			70	mA

CAPACITANCE*

Parameter Symbol	Parameter Descriptions	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance			25	pF
$C_{I/O}$	I/O Pin Capacitance			25	pF
C_{OUT}	Output Pin Capacitance			25	pF

* Parameters are not "Tested".

SWITCHING CHARACTERISTICS over operating ranges

Parameter Number	Parameter Symbol	Parameter Description	Min.	Max.	Unit
1	t_{CLK}	CLK Cycle Time	80	1000	ns
2	t_W	CLK HIGH Pulse Width	35		ns
3	t_W	CLK LOW Pulse Width	35		ns
4	t_{PD}	CLK Edge to Output Valid Delay		45	ns
5	t_{PD}	CLK Edge to Output Float Delay (Note 1)		55	ns
CPU INTERFACE					
6	t_S	A_0–A_3 Valid to $\overline{RD}$ or $\overline{WR}$ FE Setup	10		ns
7	t_H	$\overline{RD}$ or $\overline{WR}$ RE to A_0–A_3 Valid Hold	10		ns
8	t_S	$\overline{CS}$ Valid to $\overline{RD}$ or $\overline{WR}$ FE Setup	0		ns
9	t_H	$\overline{RD}$ or $\overline{WR}$ RE to $\overline{CS}$ RE Hold	10		ns
10	t_{PD}	$\overline{RD}$ or $\overline{WR}$ FE to RDY Delay		40	ns
10a	t_{PD}	$\overline{WR}$ FE to $\overline{DRQ}$ RE Delay		40	ns
11	t_{PD}	Data Out Valid to RDY RE Delay	CLK HIGH –10		ns
12	t_H	RDY RE to or $\overline{WR}$ RE Hold	25		ns
13	t_H	$\overline{RD}$ RE to Data Out Valid Hold	0		ns
14	t_D	$\overline{RD}$ RE to Data Out Float Delay (Note 1)		55	ns
15	t_S	Data In Valid to $\overline{WR}$ RE Setup	20		ns
16	t_H	$\overline{WR}$ RE to Data In Valid Hold	20		ns
17	t_W	$\overline{WR}$ LOW Width (Note 2)	60		ns
18	t_W	$\overline{WR}$ Recovery	1 CLK+20		ns
19	t_W	$\overline{RD}$ Recovery	0.5		CLK
FONT INTERFACE					
20	t_H	FALE1 or FALE2 FE to FA[illegible] Hold	10		ns
21	t_S	Data In Valid to CLK R[illegible]	10		ns
22	t_H	$\overline{FRD}$ RE to Data In V[illegible]	0		ns
23	t_H	$\overline{FWR}$ RE to Data Out Va[illegible] Hold	10		ns
23a	t_W	FALE1 or FALE2 HIGH Width	CLK LOW –10		ns
VIDEO INTERFACE					
24	t_S	Da[illegible] Valid to CLK RE Setup	20		ns
25	t_H	$\overline{VR}$ R[illegible] to Data In Valid Hold	0		ns
PRINTER INTERFACE (Notes 3, 4)					
26	t_{CLK}	VCLK Cycle Time (Synchronous Mode)	50	2000	ns
27	t_W	VCLK HIGH Pulse Width (Synchronous Mode)	20		ns
28	t_W	VCLK LOW Pulse Width (Synchronous Mode)	20		ns
29	t_{CLK}	VCLK Cycle Time (Asynchronous Mode)	31	2000	ns
30	t_W	VCLK HIGH Pulse Width (Asynchronous Mode)	10		ns
31	t_W	VCLK LOW Pulse Width (Asynchronous Mode)	10		ns
32	t_W	PSYNC Pulse Width	1		VCLK
33	t_D	PSYNC RE to LSYNC RE Delay	50		ns
34	t_W	LSYNC Pulse Width	1		VCLK
35	t_S	LSYNC RE to VCLK RE Setup (Synchronous Mode)	15		ns
36	t_D	VCLK RE to VDO Valid Delay (Synchronous Mode)		40	ns
37	t_D	VCLK Edge to VDO Valid Delay (Asynchronous Mode)	1.5 VCLK + 45		ns

Notes:

1) Parameter #5 and #14–Float times indicate that the RPC is no longer driving bus outputs and are measured by determining when outputs that were driven LOW have risen above a level of 0.8 V.

2) Parameter #17–$\overline{WR}$ Width (LOW)–applies only when RDY does not go LOW. When the RPC is not ready to accept a write, specs #10 and #12 will apply and determine the necessary write width.

Notes (continued):

3) PSYNC will not be recognized immediately after the Raster Scan Control bit (RC) is set by the CPU. Two words must be prefetched from the Video Memory before printing of a new page can begin. This requires two Read-Modify-Write cycles plus completion of any memory cycle in progress (approximately 25 CLKs minimum). A PSYNC that occurs before the data for VDO is ready will be ignored.

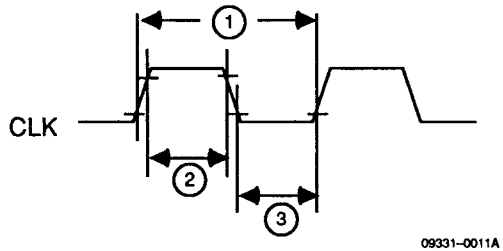
4) LSYNC for a new line cannot occur immediately after the last pixel of the previous line has been clocked out by VCLK. At least 10 VCLKs must occur between the last valid pixel on VDO and the next LSYNC in order for the X Margin and X Size values to be processed correctly.

Output-to-Output Timing Relationships

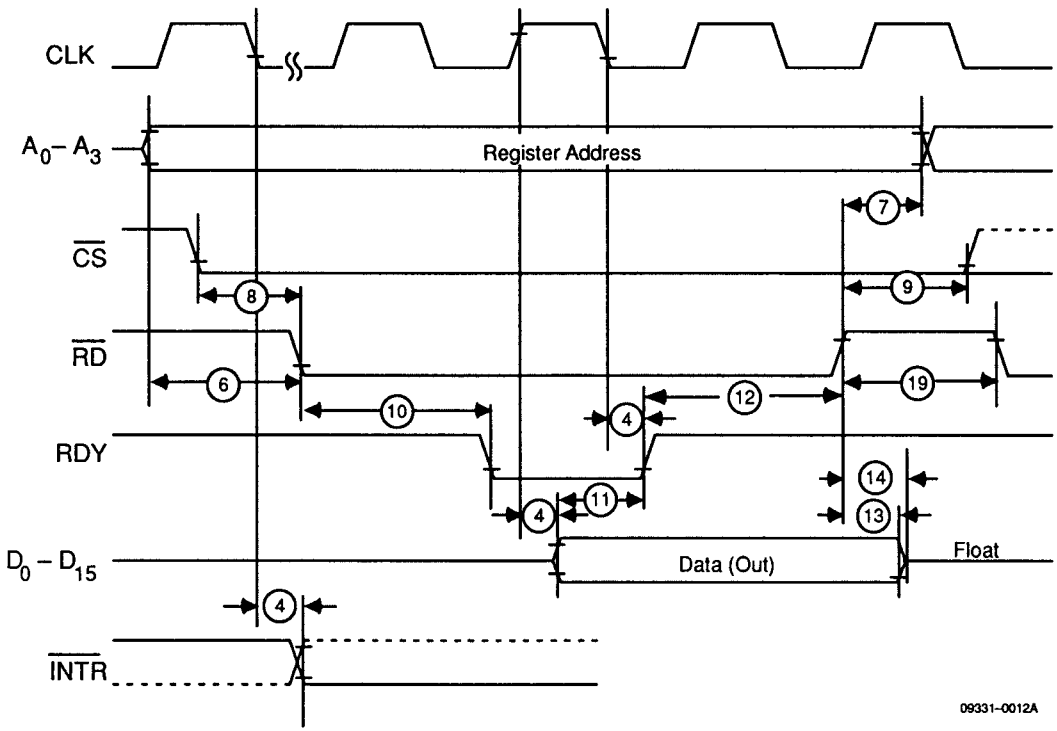
Parameter #4 CLK Edge to Output Valid Delay–can be used for all clocked outputs as indicated in the timing diagrams. All outputs are clocked in the same manner and the delay for any two unrelated outputs will track within 10 ns. Output-to-output relationships can be determined by the number of full or half CLKs between them according to the formula:

TD = (n CLKs x Cycle Time)–10 ns

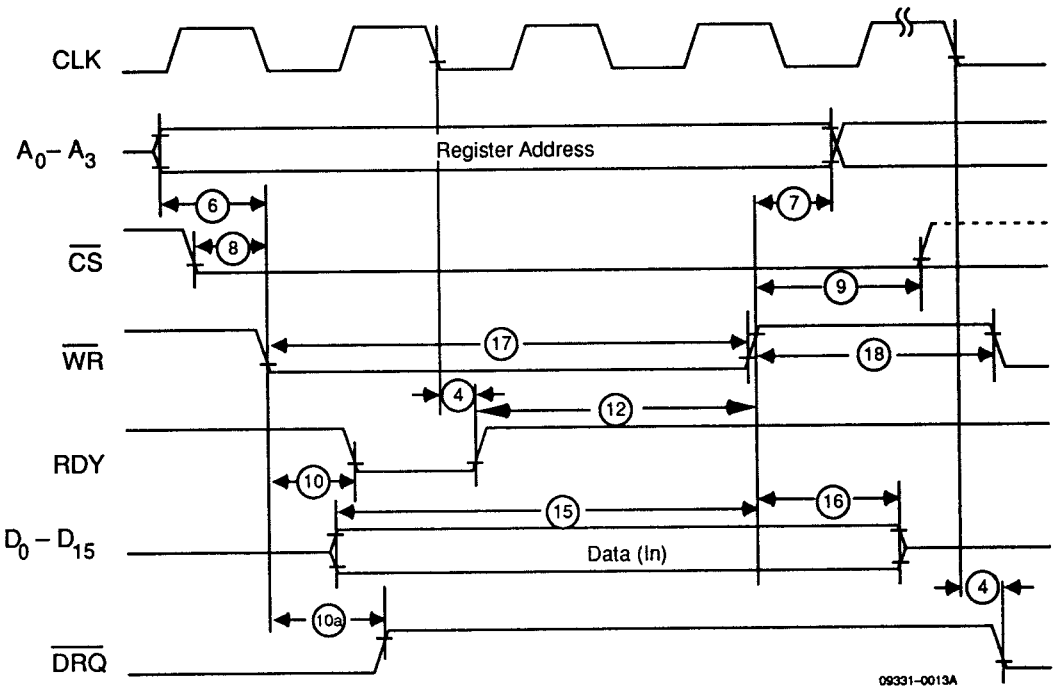
SWITCHING WAVEFORMS



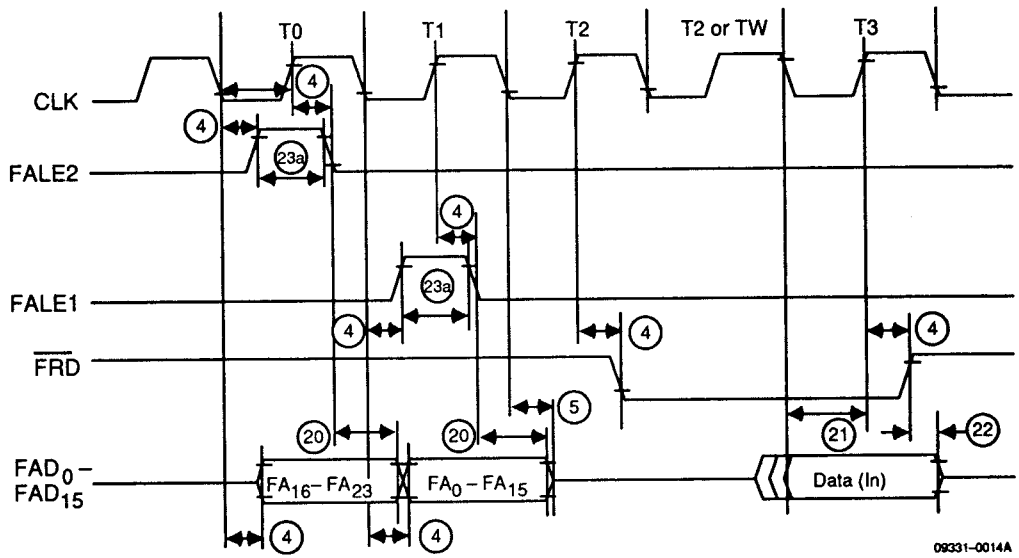
Clock Cycle Timing



CPU Read Access Timing

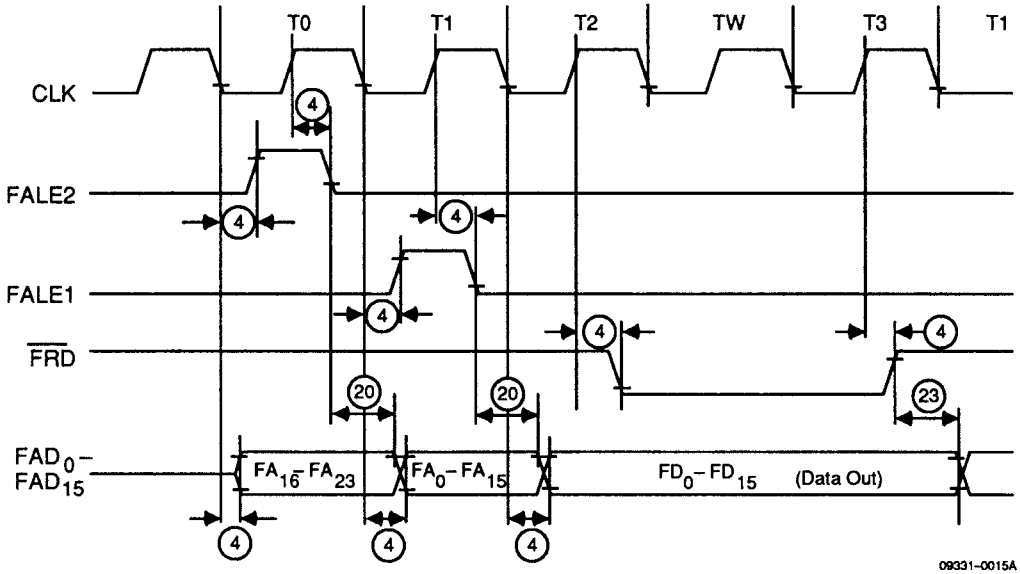


CPU Write Access Timing

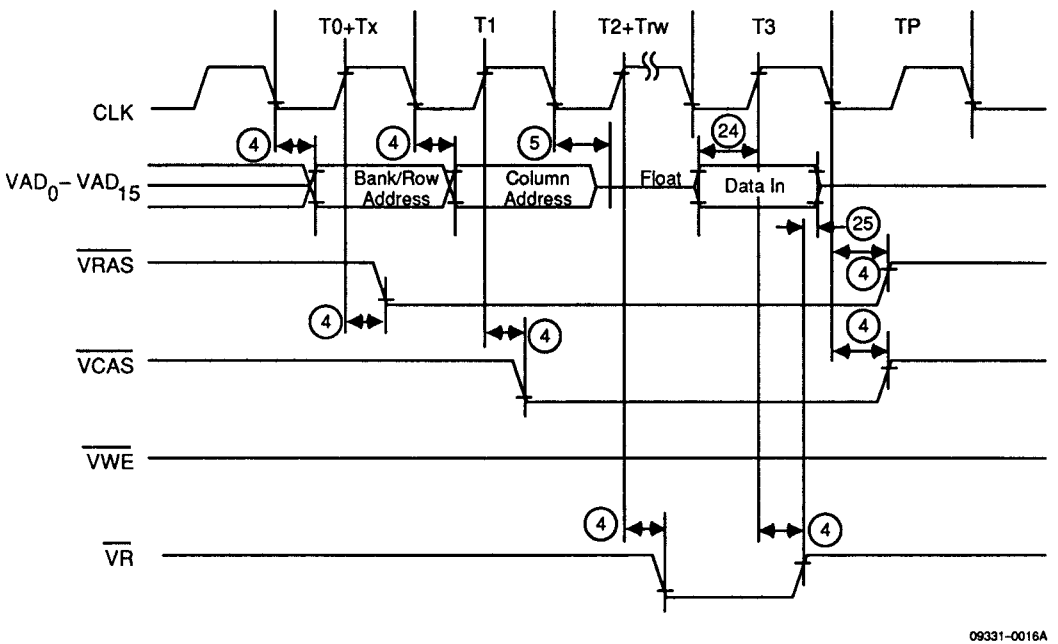


Font Memory Read Access Timing

SWITCHING WAVEFORMS (continued)

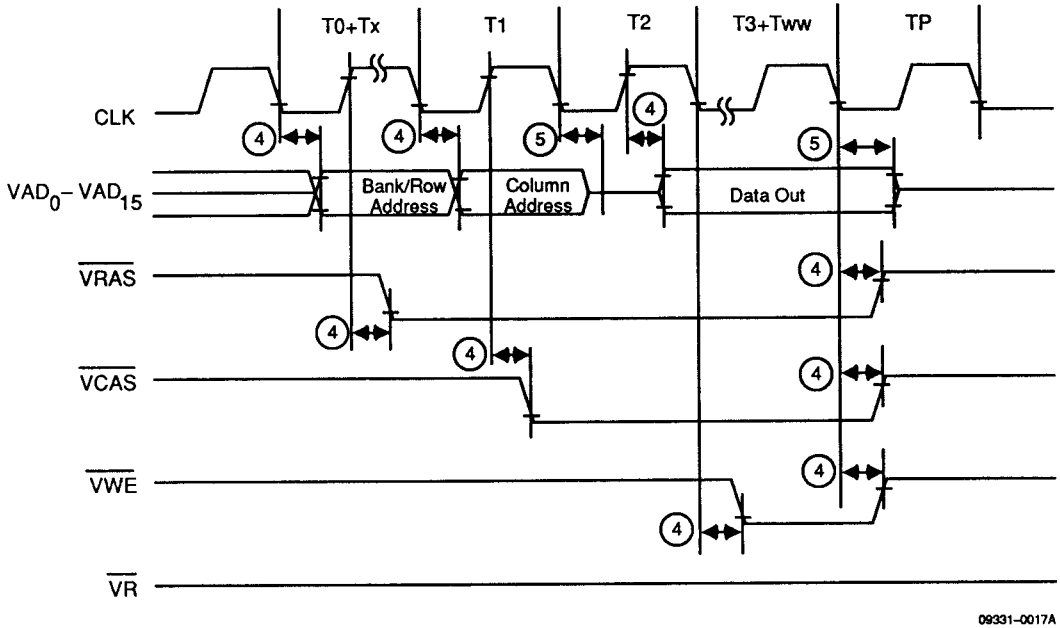


Font Memory Write Access Timing

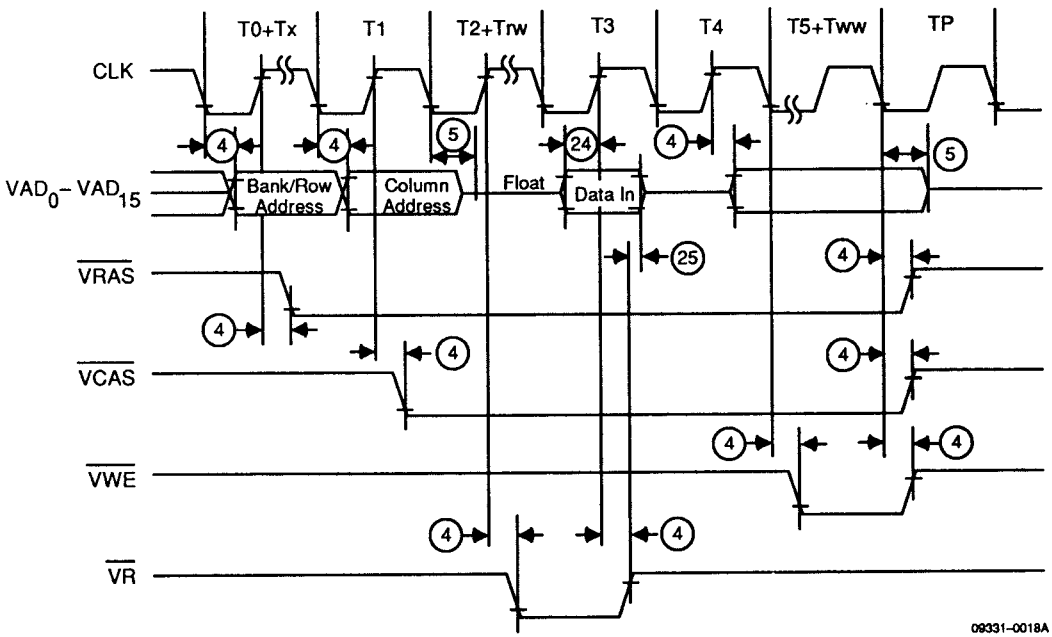


Video I/F Read Access Timing

SWITCHING WAVEFORMS (continued)

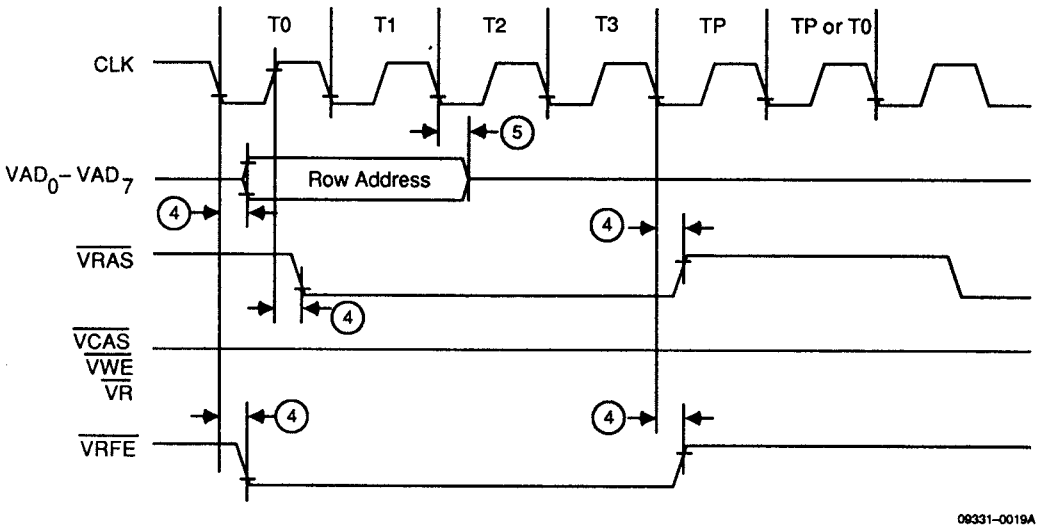


Video I/F Write Access Timing

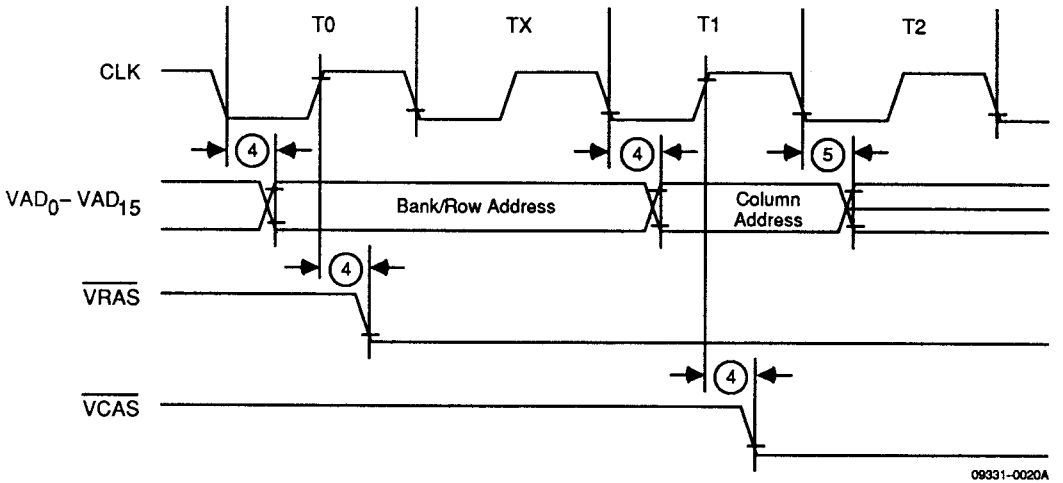


Video I/F Read-Modify-Write Access Timing

SWITCHING WAVEFORMS (continued)

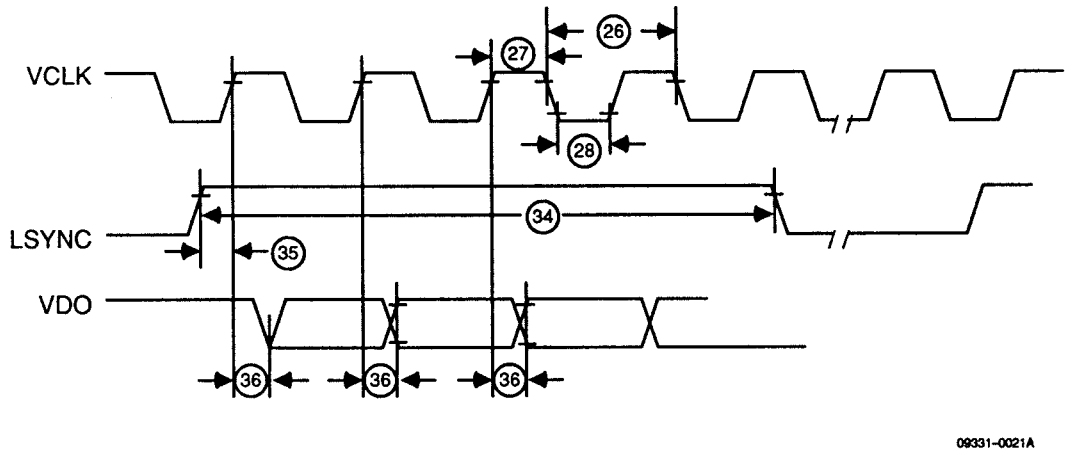


Video I/F Refresh Timing



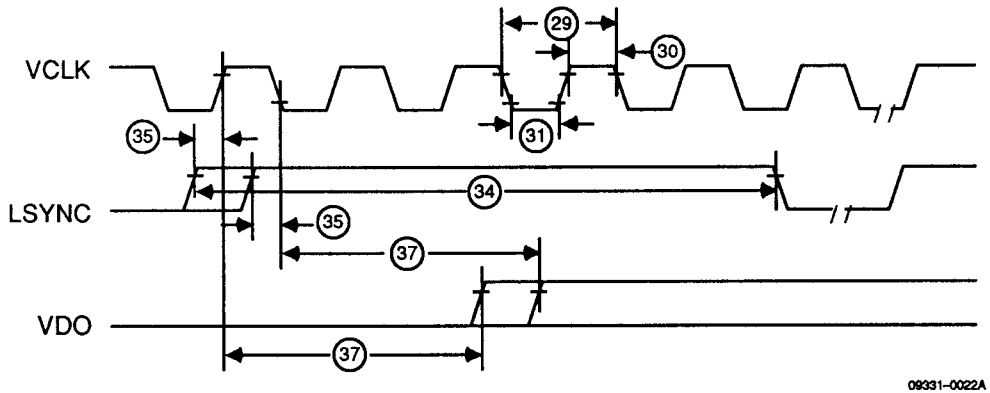
Video Extension Timing

SWITCHING WAVEFORMS (continued)



09331-0021A

LBP Timing (SYNC Mode)



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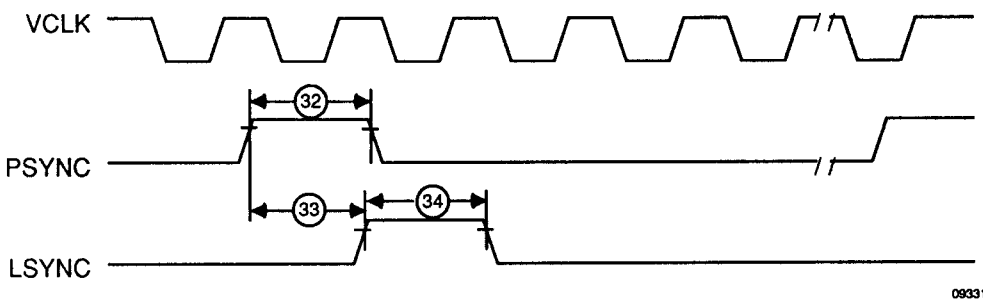
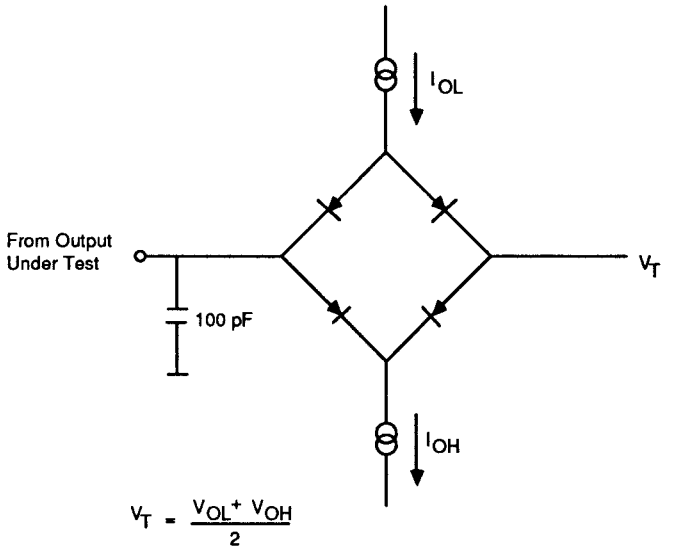
LBP Timing (ASYNC Mode)



09331-0023A

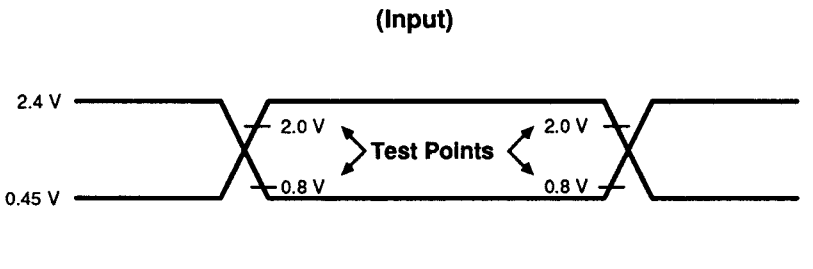
PSYNC Timing

SWITCHING TEST CIRCUIT



09331-0024A

SWITCHING TEST WAVEFORM



10487-030A