

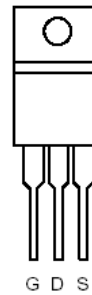
## N-Channel 60-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

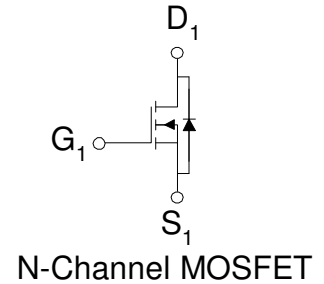
- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TO-220 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
60	9.9 @ $V_{GS} = 10V$	90 <sup>a</sup>
	13 @ $V_{GS} = 4.5V$	

TO-220CFM



Top View



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		$V_{DS}$	60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$T_C = 25^\circ\text{C}$	$I_D$	90	A
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	240	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	90	A
Power Dissipation <sup>a</sup>	$T_C = 25^\circ\text{C}$	$P_D$	300	W
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	0.5	$^\circ\text{C/W}$

### Notes

- Package Limited
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 uA	1		4	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V			1	uA
		V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C			25	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	120			A
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A			9.9	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A			13	
Forward Tranconductance <sup>A</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		30		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 34 A, V <sub>GS</sub> = 0 V		1.1		V
Dynamic <sup>b</sup>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 90 A		49		nC
Gate-Source Charge	Q <sub>gs</sub>			9.0		
Gate-Drain Charge	Q <sub>gd</sub>			10		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 25 V, R <sub>L</sub> = 25 Ω , I <sub>D</sub> = 34 A, V <sub>GEN</sub> = 10 V		16		nS
Rise Time	t <sub>r</sub>			10		
Turn-Off Delay Time	t <sub>d(off)</sub>			50		
Fall-Time	t <sub>f</sub>			23		

## Notes

- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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