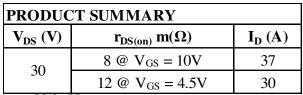
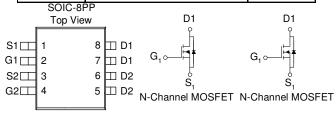
## Dual N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

•	Low r <sub>DS(on)</sub> provides higher efficiency and
	extends battery life

- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology











ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NO					
Paramete r		Symbol	Limit	Units	
Drain-Source Voltage	$V_{DS}$	30	V		
Gate-Source Voltage			20	v	
	$T_A=25^{\circ}C$		37		
Continuous Drain Current <sup>a</sup>	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	$\mathbf{I}_{\mathrm{D}}$	30	A	
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	±50			
Continuous Source Current (Diode Conduction) <sup>a</sup>			13	A	
D : a	$T_A=25^{\circ}C$	$P_{\mathrm{D}}$	16	W	
Power Dissipation <sup>a</sup>	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	rD	10	•••	
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Maximum	Units		
M · T a	t <= 10 sec	$R_{ heta JA}$	35	<sup>0</sup> C/N/		
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	$R_{ heta JC}$	8	°C/W		

1

## Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Analog Power AM7930N

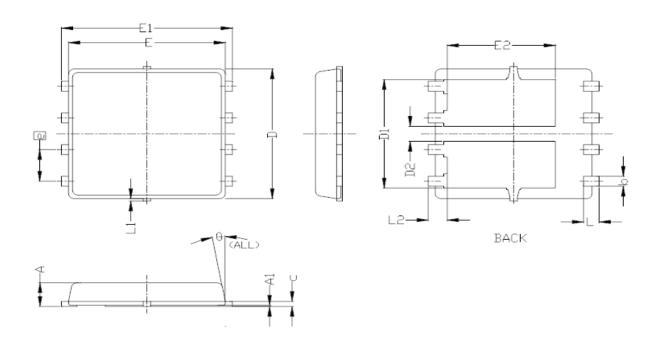
SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)								
D 4	G 1 1		Limits			TT .4		
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit		
Static								
Gate-Threshold Voltage	$V_{GS(th)}$	VGS = VDS, $ID = 250  uA$	1			V		
Gate-Body Leakage	$I_{GSS}$	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA		
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			A		
Drain-Source On-Resistance <sup>A</sup>	r	VGS = 10  V, ID = 1  A			8	mΩ		
Drain-Source On-Resistance	r <sub>DS(on)</sub>	VGS = 4.5  V, ID = 1  A			12	11132		
Forward Tranconductance <sup>A</sup>	$g_{\mathrm{fs}}$	$V_{DS} = 15 \text{ V}, I_D = 1 \text{ A}$		40		S		
Dynamic	•				-5	<u>-</u>		
Total Gate Charge	$Q_{\mathrm{g}}$	N-Channel		10		пС		
Gate-Source Charge	$Q_{gs}$	$V_{DS}$ =15V, $V_{GS}$ =4.5V, $I_{D}$ =1A		6				
Gate-Drain Charge	$Q_{\mathrm{gd}}$	ν <sub>DS</sub> =13 ν, ν <sub>GS</sub> =4.3 ν, 1 <sub>D</sub> =1/1		9				
Input Capacitance	$C_{iss}$	N-Channel		2000				
Output Capacitance	$C_{oss}$	$V_{DS}$ =15V, $V_{GS}$ =0V, f=1MHz		300		pF		
Reverse Transfer Capacitance	$C_{rss}$	VDS-13 V, VGS-0 V, 1-11V1112		200				
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel		10				
Rise Time	t <sub>r</sub>	$V_{DD}$ =15V, VGS=10V, ID=1A ,		20		nS		
Turn-Off Delay Time	$t_{d(off)}$	$R_{\rm GEN}$ =25 $\Omega$		50				
Fall-Time	$t_{ m f}$	10GEN-2522		30				

## Notes

- a. Pulse test:  $PW \le 300$ us duty cycle  $\le 2\%$ .
- b. Guaranteed by design, not subject to production testing.

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## Package Information



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES			
STIMBULS	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.85	0. 95	1.00	0.033	0. 037	0. 039	
A1	0.00		0.05	0.000		0.002	
b	0.30	0.40	0.50	0.012	0.016	0.020	
c	0. 15	0. 20	0. 25	0.006	0.008	0.010	
D		5. 20 BSC 0. 205 E			0.205 BSC		
D1	4. 35 BSC			0. 171 BSC			
D2	0.50	0.60	0.75	0.020 0.024 0.03			
E	5. 55 BSC			0. 219 BSC			
E1	6. 05 BSC			0. 238 BSC			
E2	3.82 BSC			0. 150 BSC			
e	1. 27 BSC			0. 050 BSC			
L	0.45	0. 55	0.65	0.018	0.022	0.026	
L1	0		0. 15	0		0.006	
L2	0. 68 REF			0. 027 REF			
θ	0°		10°	0°		10°	