Am78/8831•Am78/8832

Three-State Line Driver

Distinctive Characteristics

- Three-State Line Drivers pin-for-pin equivalent to the DM78/8831 and DM78/8832
- Mode control for quad single-ended or dual differential operation
- Common bus operation
- High-drive capability
- 40mA sink and source current
- Series 54/74 compatible
- 13ns typical propagation delay
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

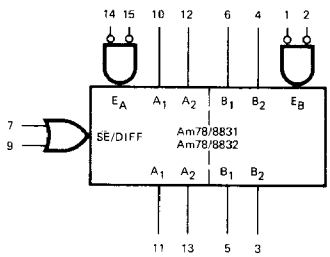
The Am78/8831 and Am78/8832 line drivers can be used either as a quad single-ended driver or as a dual differential driver. Each driver has a three-state output making the device particularly suitable for party-line operation where several drivers are directly connected to the same bus. The Am78/8832 does not have the V_{CC} clamp diodes found on the Am74/8831.

When used for single-ended operation the two differential/single-ended control inputs are held LOW. The device then operates as four independent non-inverting drivers. For differential working at least one differential/single-ended control input is held HIGH. The A-channel inputs are connected together and the B-channel inputs are connected together. Signal inputs will then pass non-inverted to the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

For party-line operation outputs of different channels are tied together, and outputs of all channels except one are forced into the third high impedance state by having at least one of the channel disable inputs HIGH. The channel that is enabled has both channel disable inputs LOW, and the low-output impedance of this output at both logic levels controls the level of the bus, provides good capacitance drive and insures good waveform integrity.

The channel which is enabled can conveniently be selected by a decoding matrix using Am9301 1-of-10 or Am9311 1-of-16 active LOW output decoders. The high drive capability at both logic levels enables drivers to drive a low impedance line and still supply the inverse leakage current of several disabled drivers.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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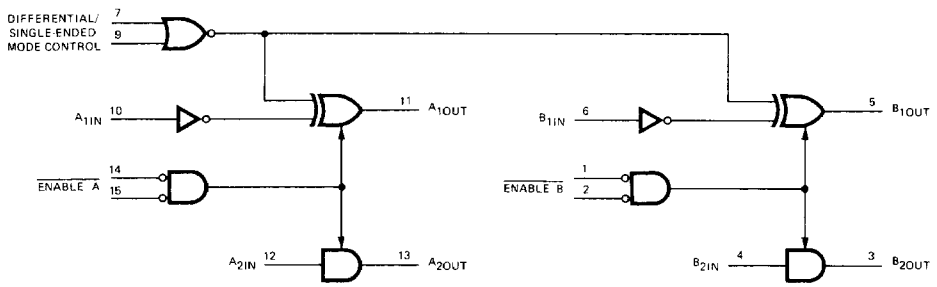
LOGIC DIAGRAM



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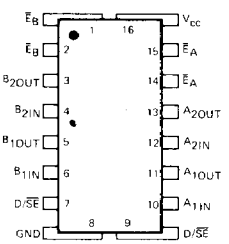
ORDERING INFORMATION

Package Type	Temperature Range	Am78/8831 Order Number	Am78/8832 Order Number
Molded DIP	0°C to +75°C	DM8831N	DM8832N
Hermetic DIP	0°C to +75°C	DM8831J	DM8832J
Dice	0°C to +75°C	AM8831X	AM8832X
Hermetic DIP	−55°C to +125°C	DM7831J	DM7832J
Hermetic Flat Pak	−55°C to +125°C	DM7831W	DM7832W
Dice	−55°C to +125°C	AM7831X	AM8832X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA
Time that 2 Bus-Connected Devices May Be in Opposite Low Impedance States Simultaneously	∞

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am8831, Am8832	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am7831, Am7832	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −40 mA	1.8	2.8		Volts
			Am7831, 32 I_{OH} = −2 mA	2.4	3.1		
			Am8831, 32 I_{OH} = −5.2 mA				
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 40 mA		0.29	0.5	Volts
			I_{OL} = 32 mA		0.2	0.4	
V_{IH}	Input HIGH Level Voltage	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level Voltage	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_L	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{LK}	Output Leakage Current	V_{CC} = MAX., $\overline{E}$ = 2.4 V, V_{OUT} = 2.4 V			5	40	µA
		V_{CC} = MAX., $\overline{E}$ = 2.4 V, V_{OUT} = 0.4 V			−5	−40	
V_I	Input Clamp Diode Voltage	V_{CC} = 5.0 V, I_I = −12 mA, T_A = 25°C				−1.5	Volts
V_O	Output Clamp Diode Voltage	V_{CC} = 5.0 V, I_I = 12 mA, T_A = 25°C Am78/8831 Only				V_{CC} + 1.5V	Volts
V_O	Output Substrate Diode Voltage	V_{CC} = 5.0 V, I_I = −12 mA, T_A = 25°C				−1.5	Volts
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V, T_A = MAX.		−40		−120	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			57	90	mA

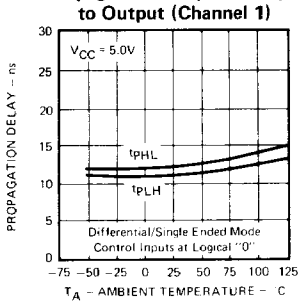
Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. Only one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°)

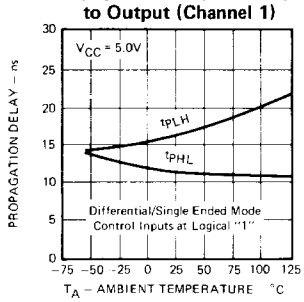
Parameters	Description	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Inputs A_1, A_2, B_1, B_2 and Single-Ended/ Diff. Control to Output		13	25	ns
t_{PHL}			13	25	ns
t_{HZ}	Delay from Output Enable to Output		6	12	ns
t_{LZ}			14	22	ns
t_{ZH}	Delay from Output Enable to Output		14	22	ns
t_{ZL}			18	27	ns

TYPICAL PERFORMANCE CHARACTERISTICS

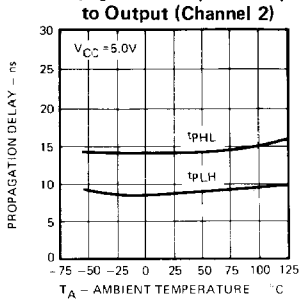
Propagation Delay from Input to Output (Channel 1)



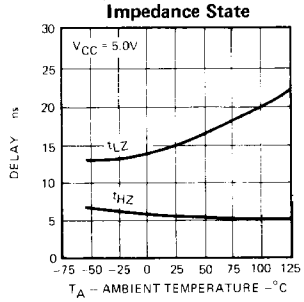
Propagation Delay from Input to Output (Channel 1)



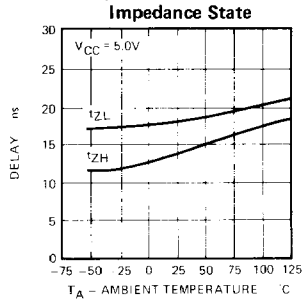
Propagation Delay from Input to Output (Channel 2)



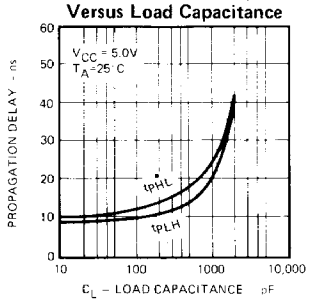
Delay from Disable to High Impedance State



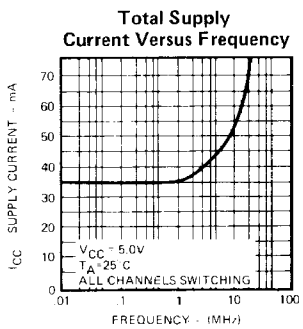
Delay from Disable to Low Impedance State



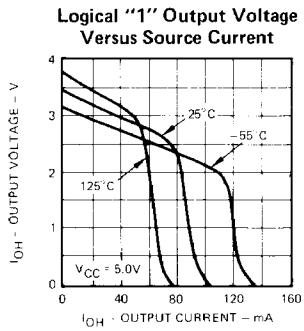
Propagation Delay Versus Load Capacitance



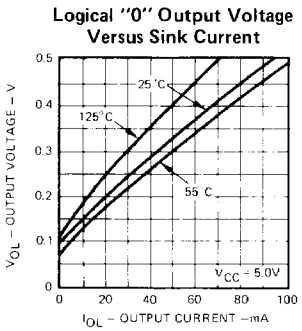
Total Supply Current Versus Frequency



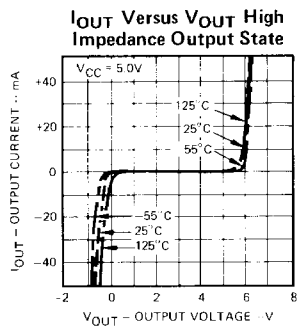
Logical "1" Output Voltage Versus Source Current



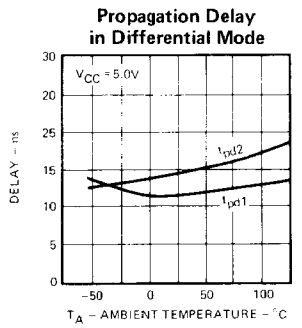
Logical "0" Output Voltage Versus Sink Current

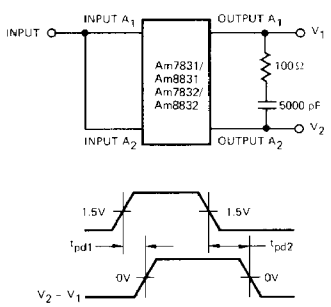


I_{OUT} Versus V_{OUT} High Impedance Output State



Propagation Delay in Differential Mode





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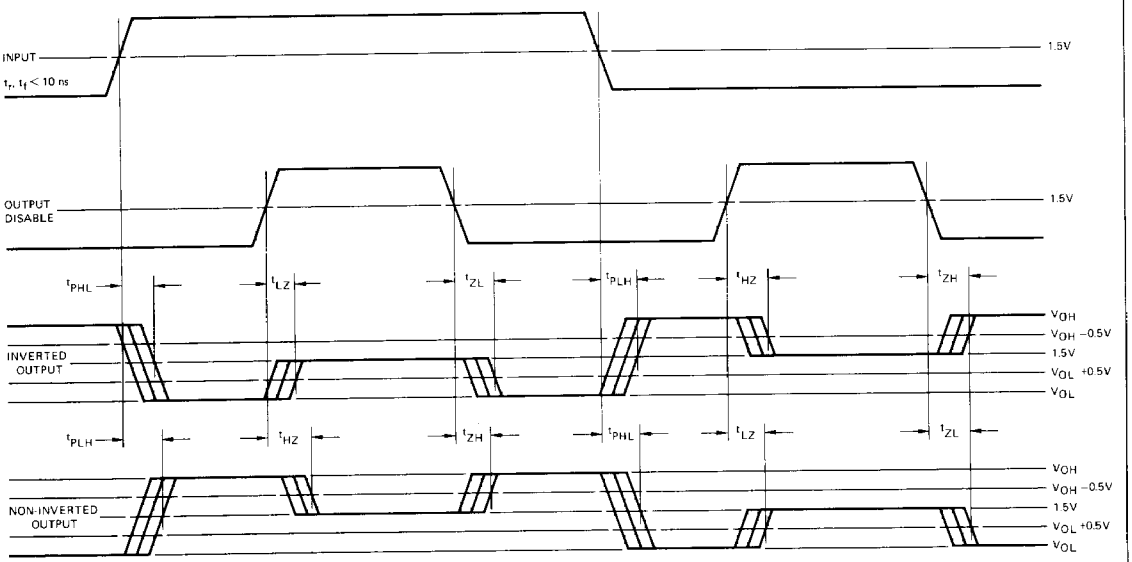
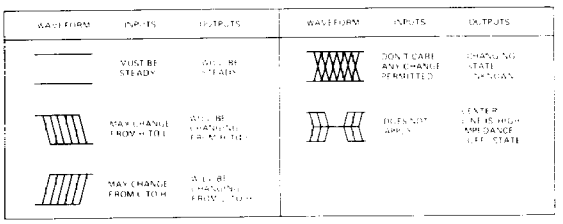
SWITCHING TIME WAVEFORMS AND TEST CIRCUIT



NOTE: V_{OL} and V_{OH} refer to actual voltages on output LOW and HIGH states.

KEY TO TIMING DIAGRAM



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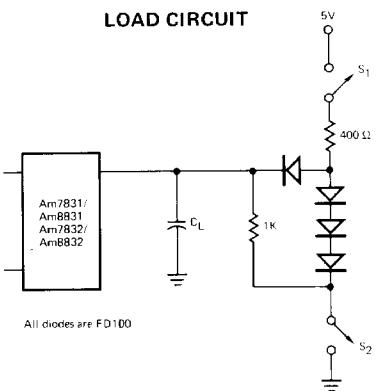
LOAD CIRCUIT



	Switch S_1	Switch S_2	C_L
t_{PLH}	closed	closed	50 pF
t_{PHL}	closed	closed	50 pF
t_{HZ}	closed	closed	* 5 pF
t_{LZ}	closed	closed	* 5 pF
t_{ZL}	closed	open	50 pF
t_{ZH}	open	closed	50 pF

*Jig Capacitance

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TRUTH TABLE
(Shown for A Channels Only)

SINGLE-ENDED/ DIFF CONTROL		A ENABLE		IN A_1	OUT A_1	IN A_2	OUT A_2
L	L	L	L	A_1	A_1	A_2	A_2
H	X	L	L	A_1	$\bar{A}_1$	A_2	A_2
X	H	L	L	A_1	$\bar{A}_1$	A_2	A_2
X	X	H	X	X	F	X	F
X	X	X	H	X	F	X	F

H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
F = Floating Output

TABLE I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TABLE III

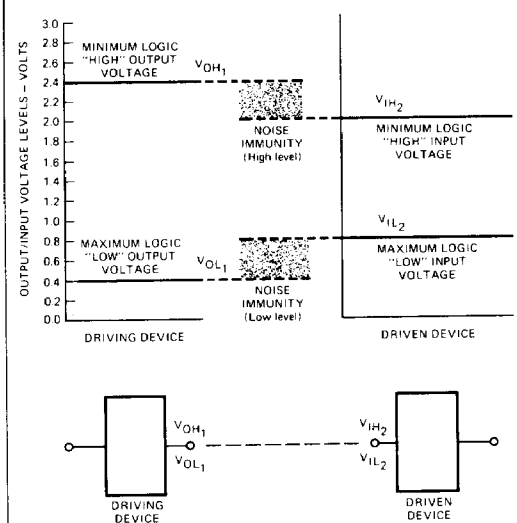
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{\text{Enable B}}$	1	1	–	–
Enable B	2	1	–	–
B_2 Out	3	–	1000	25
B_2 In	4	1	–	–
B_1 Out	5	–	1000	25
B_1 In	6	1	–	–
$\overline{\text{SE}}$/Diff	7	1	–	–
GND	8	–	–	–
$\overline{\text{SE}}$/Diff	9	1	–	–
A_1 In	10	1	–	–
A_1 Out	11	–	1000	25
A_2 In	12	1	–	–
A_2 Out	13	–	1000	25
$\overline{\text{Enable A}}$	14	1	–	–
Enable A	15	1	–	–
V_{CC}	16	–	–	–

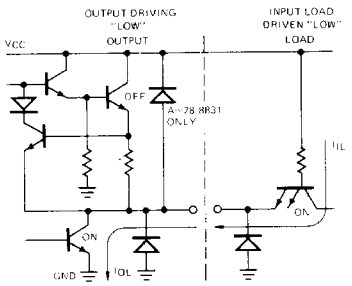
TABLE II

INPUT/OUTPUT INTERFACE CONDITIONS

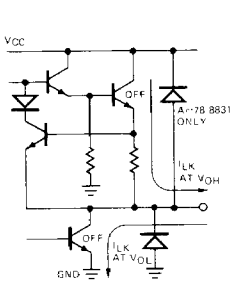
Voltage Interface Conditions – LOW & HIGH



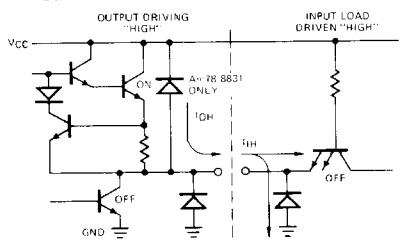
Current Interface Conditions – LOW



Current Interface Conditions – FLOATING



Current Interface Conditions – HIGH



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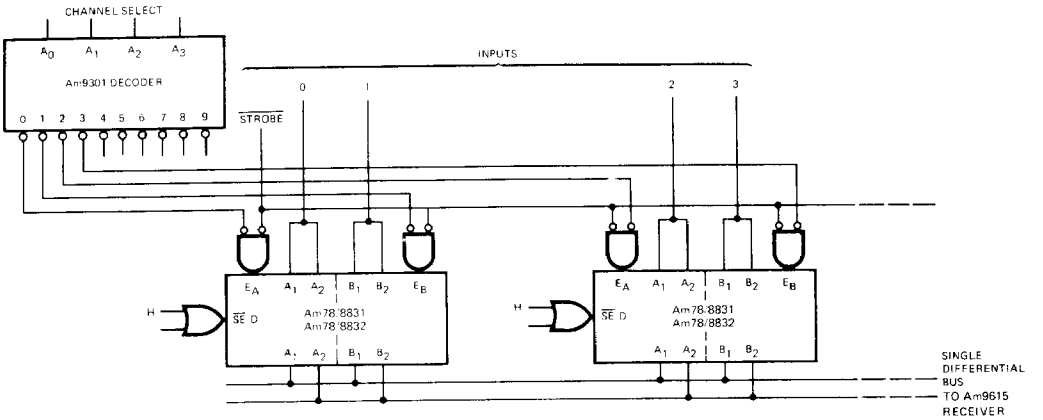
APPLICATIONS



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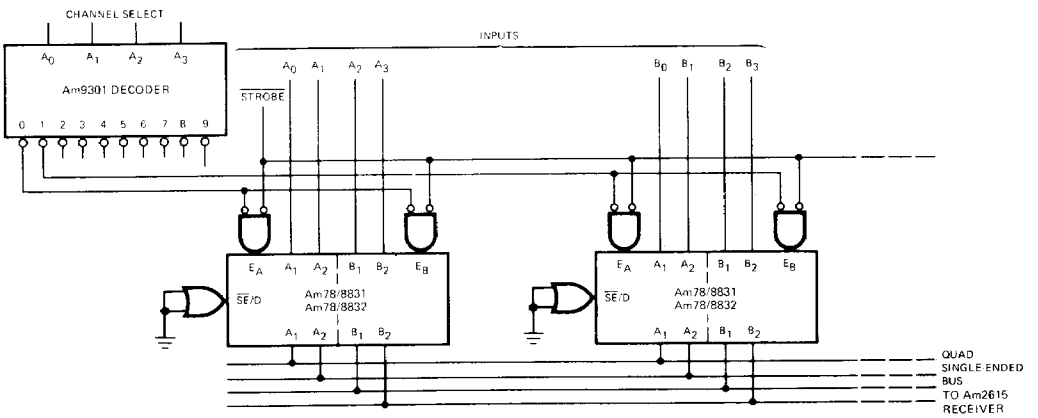
PARTY LINE DIFFERENTIAL OPERATION



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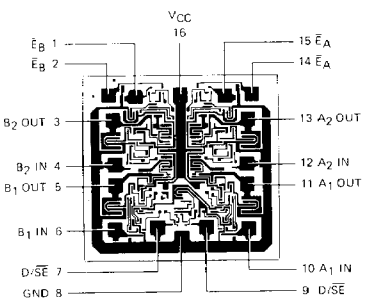
PARTY LINE SINGLE-ENDED OPERATION

Metallization and Pad Layout



DIE SIZE 0.057" X 0.058"