

650V 4A Advanced N-Ch Power MOSFET

FEATURES

- Low drain-source On resistance : $R_{DS(on)} = 2.4\Omega$ (Typ.)
- Low gate charge : $Q_g = 12nC$ (Typ.)
- Low reverse transfer capacitance : $C_{rss} = 12pF$ (Typ.)
- Lower EMI Noise
- RoHS compliant device
- 100% avalanche tested

Marking Information

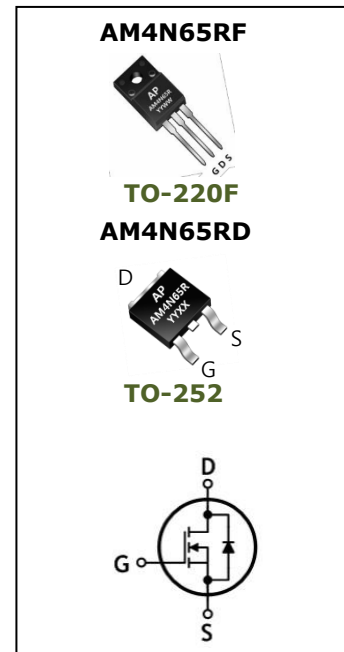
Row 1 : AP

Row 2 : Product Information

Row 3 : Date Code

- YY : Year Code

- WW : Week Code



Ordering Information

Part No.	Package	Packing	Finish	Halogen	Packing Unit
AM4N65RF	TO-220F	Tube	Sn	Free	5,000ea
AM4N65RD	TO-252	Tape & Reel	Sn	Free	2,500ea

Maximum Ratings (T_c=25 °C, unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V _{DSS}	650	V
Gate-source voltage	V _{GSS}	±30	V
Drain current (DC)*	I _D	T _c = 25°C	4
		T _c = 100°C	2.53
Drain current (Pulsed)*	I _{DM}	16	A
Power Dissipation	P _D	TO-220F	32
		TO-252	48
Single pulsed avalanche energy (Note 2)	E _{AS}	173	mJ
Avalanche current (Repetitive) (Note 1)	I _{AR}	4	A
Repetitive avalanche energy (Note 1)	E _{AR}	3.2	mJ
Junction temperature	T _J	150	°C
Storage temperature range	T _{stg}	-55~150	

*Limited only maximum junction temperature

Thermal Characteristic

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 3.9	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_C=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D = 250\mu\text{A}$, $V_{DS} = V_{GS}$	3	-	5	V
Drain-source cut-off current	I_{DSS}	$V_{DS} = 650\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 650\text{V}$, $T_C = 150^{\circ}\text{C}$	-	-	100	
Gate leakage current	I_{GSS}	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{V}$, $I_D = 2\text{A}$	-	2.4	3	Ω
Forward transfer conductance (Note 3)	g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 2\text{A}$	-	4.4	-	S
Input capacitance	C_{iss}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$	-	711	-	pF
Output capacitance	C_{oss}		-	57	-	
Reverse transfer capacitance	C_{rss}		-	12	-	
Turn-on delay time (Note 3,4)	$T_{d(on)}$	$V_{DS} = 325\text{V}$, $I_D = 4\text{A}$, $R_G = 25\Omega$	-	62	-	ns
Rise time (Note 3,4)	T_r		-	81	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	109	-	
Fall time (Note 3,4)	t_f		-	46	-	
Total gate charge (Note 3,4)	Q_g	$V_{DS} = 520\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 4\text{A}$	-	12	16	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	5	-	
Gate-drain charge (Note 3,4)	Q_g		-	2.5	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	4	A
Source current (Pulsed)	I_{SM}		-	-	16	A
Forward voltage	V_{SD}	$V_{GS} = 0\text{V}$, $I_S = 2\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S = 4\text{A}$, $V_{GS} = 0\text{V}$ $dI_F/dt = 100\text{A}/\mu\text{s}$	-	487	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	1.27	-	μC

Note :

1. Repetitive rating : Pulse width limited by maximum junction temperature.
2. $L=20\text{mH}$, $I_{AS}=4\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
3. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature



Typical Electrical Characteristic

Fig. 1 Typical Output Characteristics

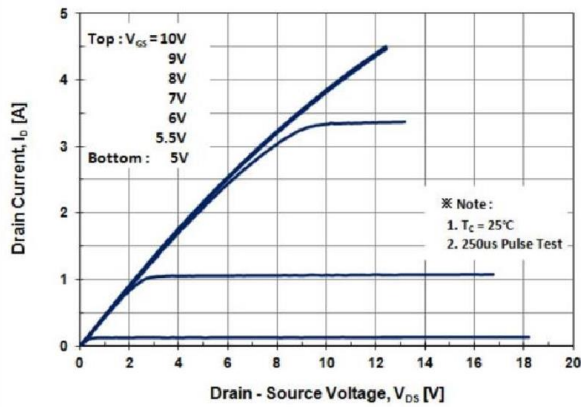


Fig. 2 Typical Output Characteristics

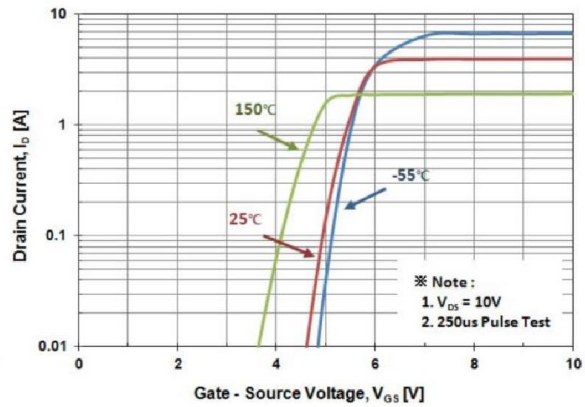


Fig. 3 On-Resistance Variation with Drain Current and Gate Voltage

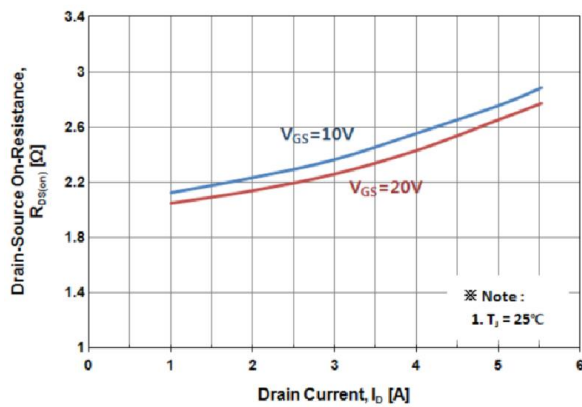


Fig. 4 Body Diode Forward Voltage Variation with Source Current

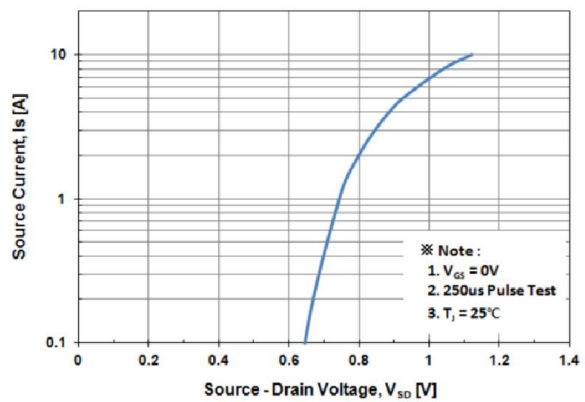


Fig. 5 Typical Capacitance Characteristics

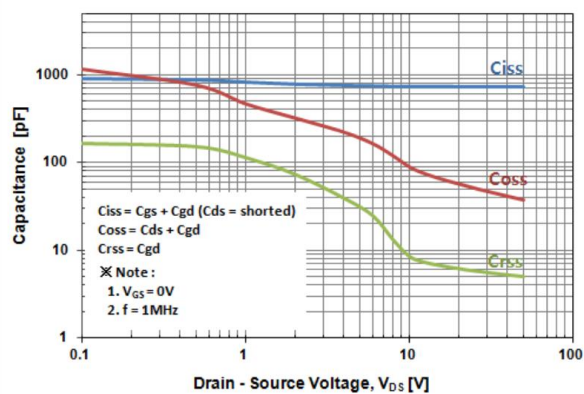
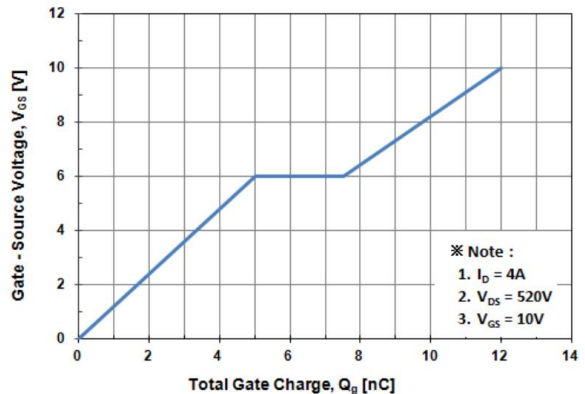


Fig. 6 Typical Total Gate Charge Characteristics





Typical Electrical Characteristic

Fig. 7 Breakdown Voltage Variation vs. Temperature

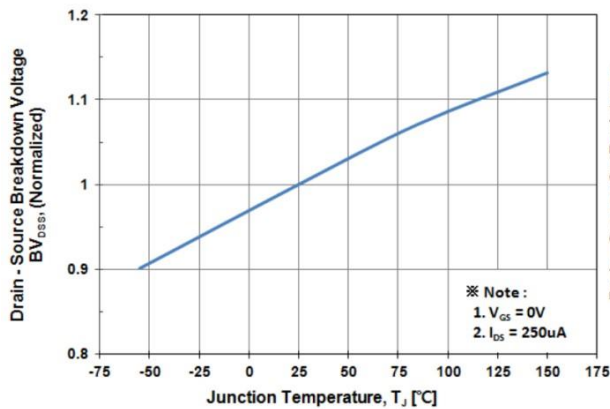


Fig. 8 On-Resistance Variation vs. Temperature

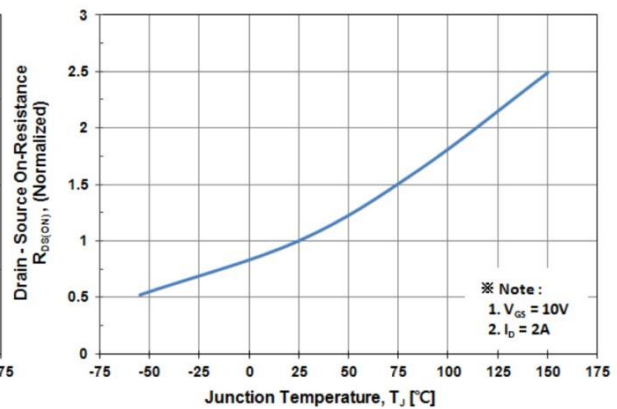


Fig. 9 Maximum Drain Current vs. Case Temperature

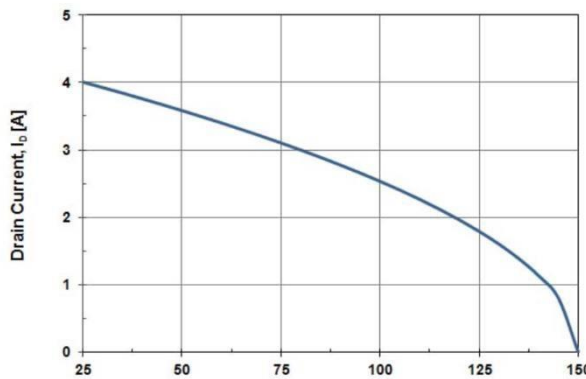


Fig. 10 Maximum Safe Operating Area

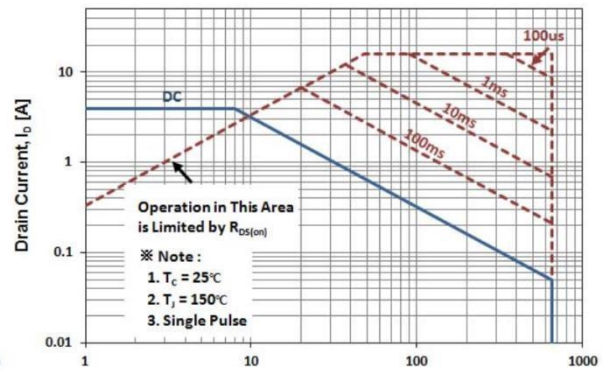


Fig. 11 Transient Thermal Impedance

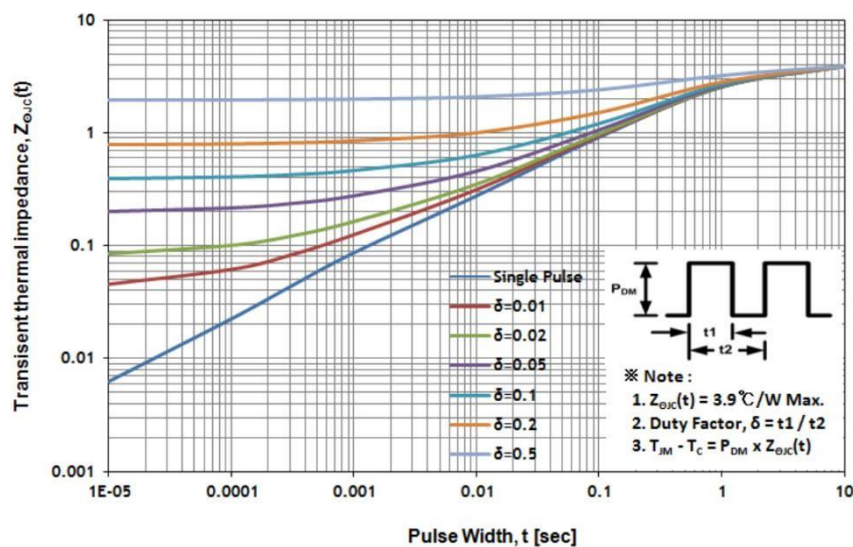


Fig. 12 Gate Charge Test Circuit & Waveform

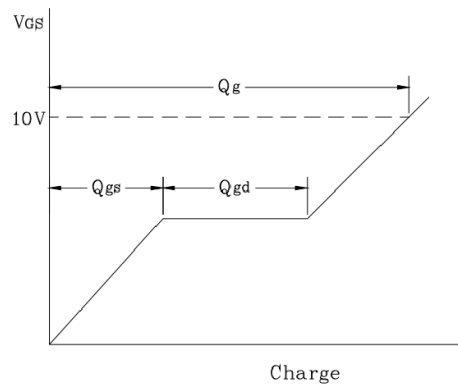
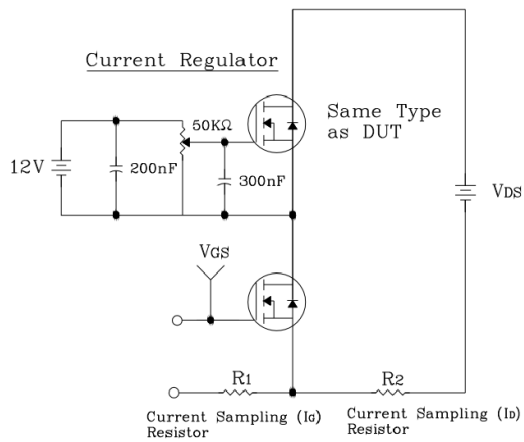


Fig. 13 Resistive Switching Test Circuit & Waveform

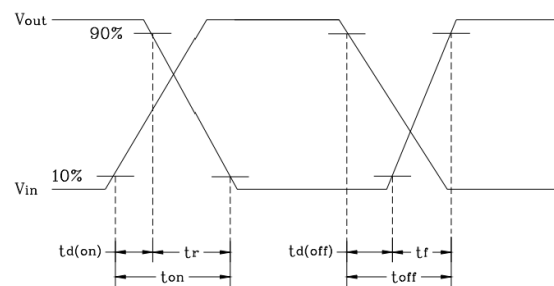
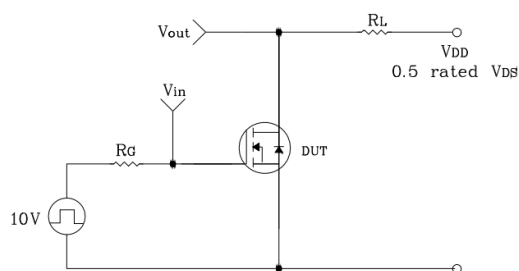


Fig. 14 E_{AS} Test Circuit & Waveform

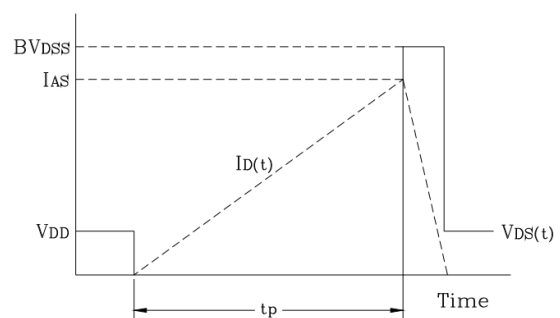
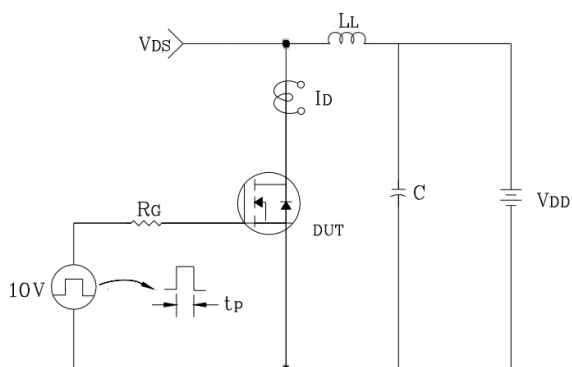
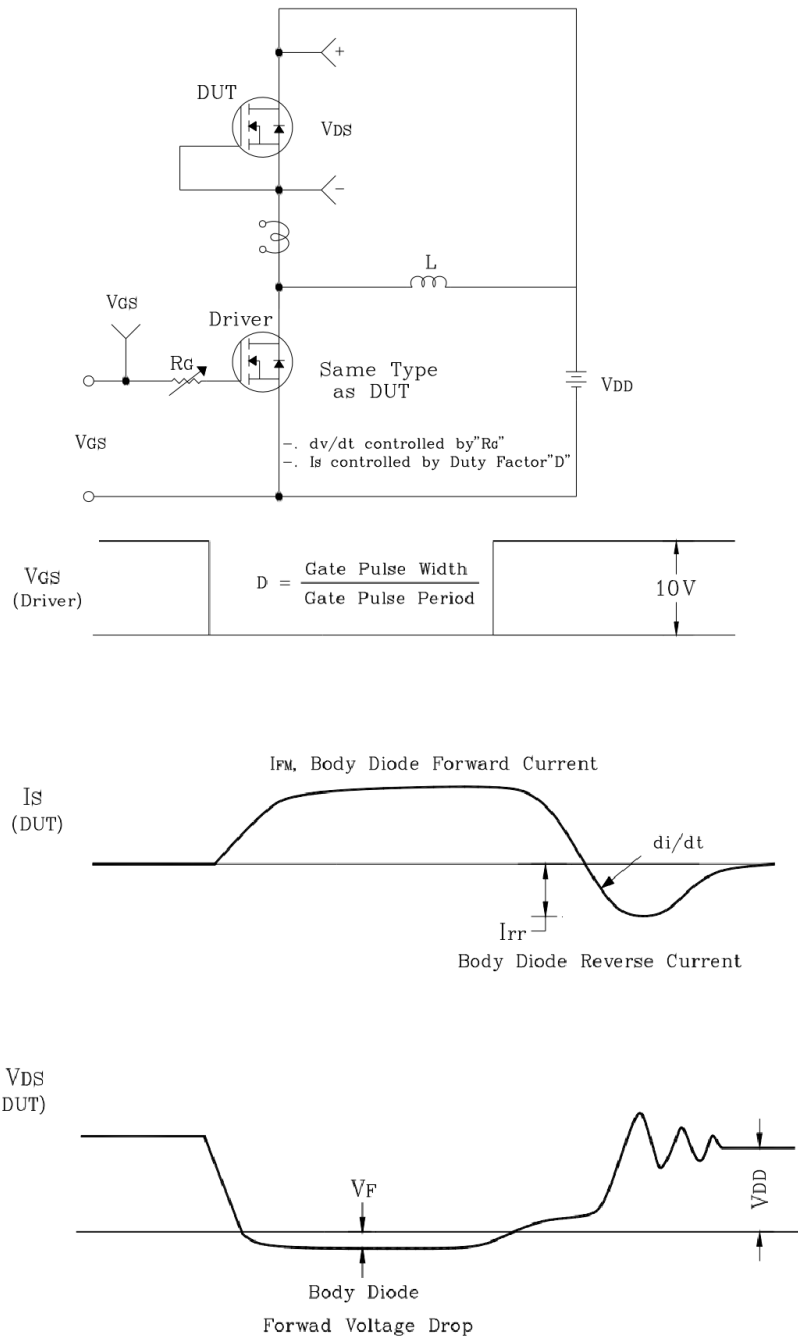




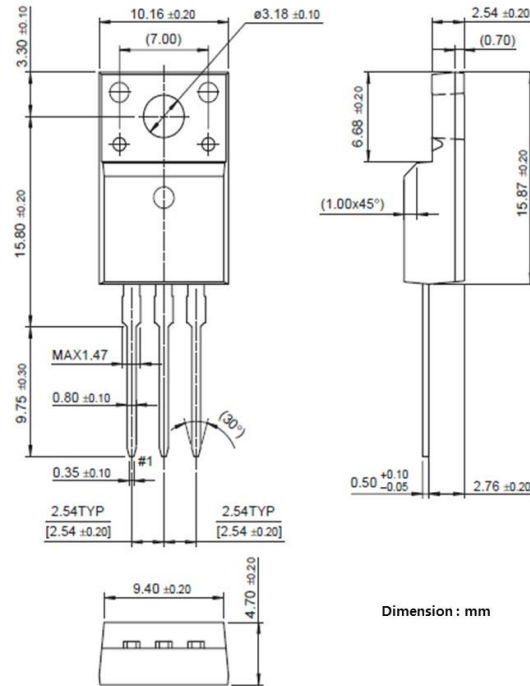
Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



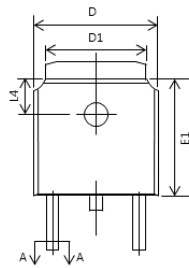
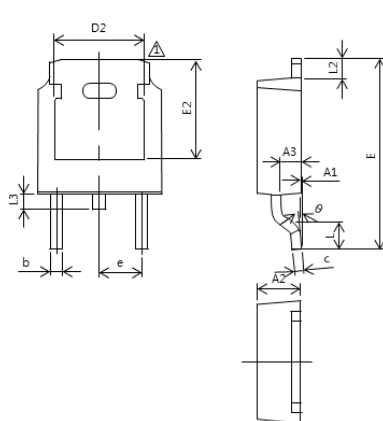


Package Dimensions

TO-220F



TO-252



TO-252-3L unit : mm			
DIM	MIN	NOM	MAX
A1	0	—	0.10
A2	2.2	2.3	2.4
A3	1.02	1.067	1.12
D	6.50	6.60	6.70
D1	5.334REF		
D2	4.70	4.826	4.92
E	9.90	10.10	10.30
E1	6.00	6.10	6.20
E2	5.30REF		
e	2.286BSC		
L	1.40	1.50	1.60
L2	0.90	—	1.25
L3	0.60	0.80	1.00
L4	1.70	1.80	1.90
Ø	0	—	8°
L/F	198×133		

Revision History

No	Date	Contents
0	2016-09-17	Initial Brief Datasheet Release

<http://www.apsemi.com>

IMPORTANT NOTICE

AP Semiconductor co, Ltd reserves the right to make changes without further notice to any products or specifications herein. AP Semiconductor co, Ltd does not assume any responsibility for use of any its products for any particular purpose, nor does AP Semiconductor co, Ltd assume any liability arising out of the application or use of any its products or circuits. AP Semiconductor co, Ltd does not convey any license under its patent rights or other rights nor the rights of others.

AP Semiconductor Co., Ltd

Contact. **Tel** 82.70.4693.2299 **FAX** 82.70.4000.4009

E-mail: sales@apsemi.com

© 2015 AP semiconductor Co., Ltd. –Printed in KOREA –All Rights Reserved.