Analog Power AM4994N

Dual N-Channel 100-V (D-S) MOSFET

Key Features:

- Low r_{DS(on)} trench technology
- · Low thermal impedance
- · Fast switching speed

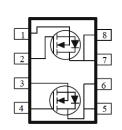
Typical Applications:

- LED Inverter Circuits
- DC/DC Conversion Circuits
- Motor drives

PRODUCT SUMMARY				
V _{DS} (V)	$r_{DS(on)}(m\Omega)$	I _D (A)		
100	80 @ V _{GS} = 10V	4.2		
	95 @ V _{GS} = 4.5V	3.9		







ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}$ C UNLESS OTHERWISE NOTED)						
Parameter		Symbol	Limit	Units		
Drain-Source Voltage	V_{DS}	100	V			
Gate-Source Voltage	V_{GS}	±20	V			
Continuous Drain Current ^a	T _A =25°C	· I _D	4.2			
Continuous Drain Current	T _A =70°C	'D	3.3	Α		
Pulsed Drain Current ^b	I _{DM}	15				
Continuous Source Current (Diode Conduction) a	I _S	2.8	Α			
Power Dissipation ^a	T _A =25°C	P_{D}	2.1	W		
Power dissipation	T _A =70°C	ľВ	1.3	VV		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Maximum	Units		
Maximum Junction-to-Ambient ^a	t <= 10 sec	$R_{\theta JA}$	62.5	°C/W		
Maximum Junction-to-Ambient	Steady State	IΛθJA	110			

1

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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Electrical Characteristics

Parameter	Symbol	Symbol Test Conditions		Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \text{ uA}$	1			V	
Gate-Body Leakage	I _{GSS}	., ., ., ., ., .,			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
Zero Gate Voltage Brain Gurrent	DSS	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	6.3			Α	
Drain-Source On-Resistance ^a	r	$V_{GS} = 10 \text{ V}, I_{D} = 2 \text{ A}$			80	mΩ	
Drain-Source On-Resistance	r _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 1.6 \text{ A}$			95	11122	
Forward Transconductance ^a	g _{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 5 \text{ A}$		14		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.4 \text{ A}, V_{GS} = 0 \text{ V}$		0.78		V	
		Dynamic ^b					
Total Gate Charge	Q_g	$V_{DS} = 50 \text{ V}, V_{GS} = 4.5 \text{ V},$		10		nC	
Gate-Source Charge	Q_gs	$I_D = 2 A$		3.8			
Gate-Drain Charge	Q_gd	10 – 2 /\		3.0			
Turn-On Delay Time	t _{d(on)}	$V_{DS} = 50 \text{ V}, R_1 = 25 \Omega,$		6			
Rise Time	t _r	$V_{DS} = 30 \text{ V}, N_L = 23 \Omega,$ $I_D = 2 \text{ A},$		6		ns	
Turn-Off Delay Time	$t_{d(off)}$	$V_{GEN} = 10 \text{ V}, R_{GEN} = 6 \Omega$		34		115	
Fall Time	t _f	VGEN = 10 V; NGEN 0 12		8			
Input Capacitance	C_{iss}			1574			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ Mhz}$		64		pF	
Reverse Transfer Capacitance	C_{rss}]		46			

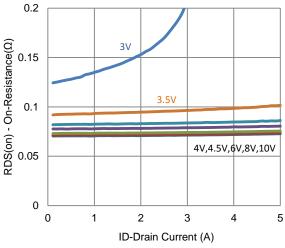
Notes

- Pulse test: PW <= 300us duty cycle <= 2%.
- Guaranteed by design, not subject to production testing. b.

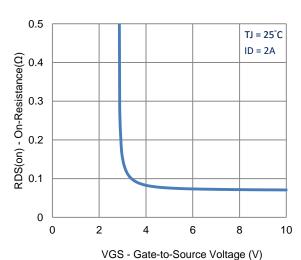
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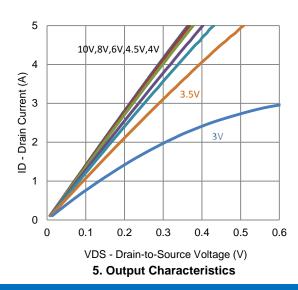
Typical Electrical Characteristics

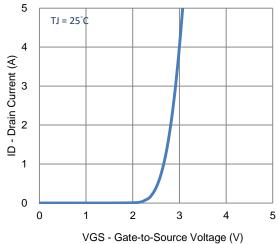


1. On-Resistance vs. Drain Current

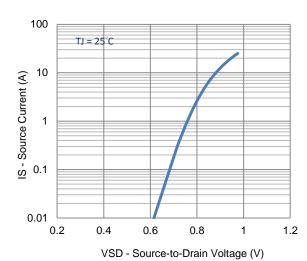


3. On-Resistance vs. Gate-to-Source Voltage

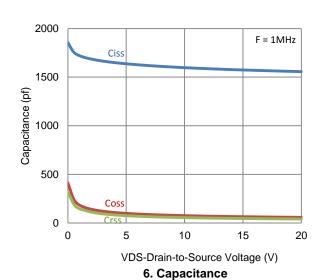




2. Transfer Characteristics

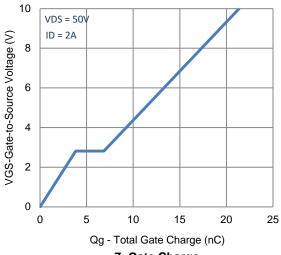


4. Drain-to-Source Forward Voltage



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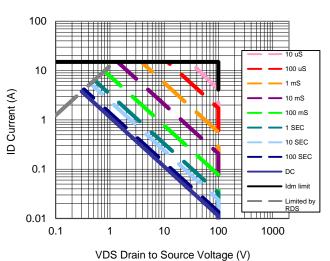
Typical Electrical Characteristics

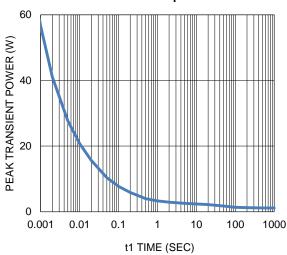


2.5 (C) 2 (D) 2 (D) 2 (D) 2 (D) 3 (D) 3 (D) 3 (D) 3 (D) 3 (D) 4 (D) 3 (D) 4 (D) 3 (D) 4 (D) 3 (D) 4 (D)

7. Gate Charge

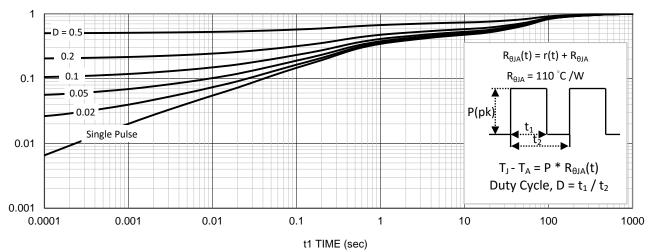






9. Safe Operating Area

10. Single Pulse Maximum Power Dissipation

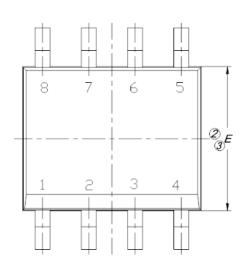


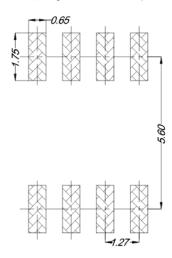
11. Normalized Thermal Transient Junction to Ambient

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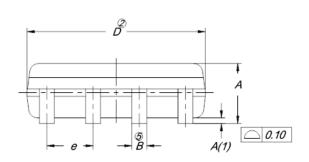
Package Information

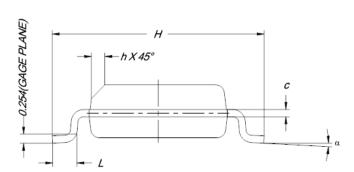
Land Pattern (Only for Reference)





5114	MILLIMETERS				
DIM.	MIN.	NOM.	MAX.		
Α	1.35	1.55	1.75		
A(1)	0.10	0.18	0.25		
В	0.38	0.45	0.51		
С	0.19	0.22	0.25		
D	4.80	4.90	5.00		
E	3.80	3.90	4.00		
е	1.27 BSC				
Н	5.80	6.00	6.20		
L	0.50	0.72	0.93		
α	0°	4°	8°		
h	0.25	0.38	0.50		





Note:

- All Dimension Are In mm.
- Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- 5. Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.