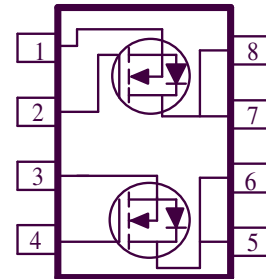


## Dual N-Channel 100-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology



### PRODUCT SUMMARY

$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
100	430 @ $V_{GS} = 10V$	1.8
	480 @ $V_{GS} = 4.5V$	1.7

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	1.8	A
	$T_A = 70^\circ\text{C}$		1.4	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	$\pm 7$	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	1.3	A
Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	2.1	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Case <sup>a</sup>	$t \leq 5 \text{ sec}$	$R_{\theta JC}$	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 5 \text{ sec}$	$R_{\theta JA}$	60	$^\circ\text{C/W}$

#### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 uA	100			V
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 uA	1			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	uA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C			25	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	3			A
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.8 A			430	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.7 A			480	
Forward Tranconductance <sup>A</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.8 A		3.6		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 2.3 A, V <sub>GS</sub> = 0 V		0.7		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 1.8 A		3		nC
Gate-Source Charge	Q <sub>gs</sub>			1.5		
Gate-Drain Charge	Q <sub>gd</sub>			2.2		
<b>Switching</b>						
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 25 V, R <sub>L</sub> = 25 Ω , I <sub>D</sub> = 1 A, V <sub>GEN</sub> = 10 V		4.8		nS
Rise Time	t <sub>r</sub>			3.9		
Turn-Off Delay Time	t <sub>d(off)</sub>			12.7		
Fall-Time	t <sub>f</sub>			3.2		

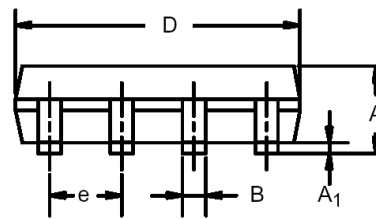
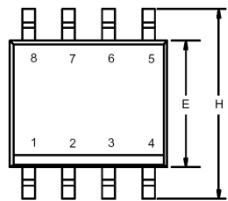
## Notes

- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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## Package Information

## SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

