

## Dual N-Channel 100-V (D-S) MOSFET

### Key Features:

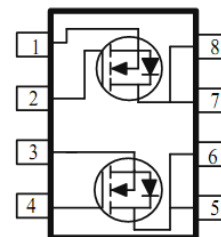
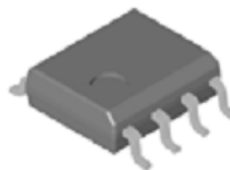
- Low  $r_{DS(on)}$  trench technology
- Low thermal impedance
- Fast switching speed

### Typical Applications:

- PoE Power Sourcing Equipment
- PoE Powered Devices
- Telecom DC/DC converters
- White LED boost converters



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



| PRODUCT SUMMARY |                            |           |
|-----------------|----------------------------|-----------|
| $V_{DS}$ (V)    | $r_{DS(on)}$ (m $\Omega$ ) | $I_D$ (A) |
| 100             | 81 @ $V_{GS} = 10V$        | 4.2       |
|                 | 92 @ $V_{GS} = 4.5V$       | 4.0       |

| ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED) |                          |                |            |                  |
|---|--------------------------|----------------|------------|------------------|
| Parameter   |                          | Symbol         | Limit      | Units            |
| Drain-Source Voltage  |                          | $V_{DS}$       | 100        | V                |
| Gate-Source Voltage   |                          | $V_{GS}$       | $\pm 20$   |                  |
| Continuous Drain Current <sup>a</sup>                                       | $T_A = 25^\circ\text{C}$ | $I_D$          | 4.2        | A                |
|   | $T_A = 70^\circ\text{C}$ |                | 3.3        |                  |
| Pulsed Drain Current <sup>b</sup>   |                          | $I_{DM}$       | 30         |                  |
| Continuous Source Current (Diode Conduction) <sup>a</sup>                   |                          | $I_S$          | 3          | A                |
| Power Dissipation <sup>a</sup>  | $T_A = 25^\circ\text{C}$ | $P_D$          | 2.1        | W                |
|   | $T_A = 70^\circ\text{C}$ |                | 1.3        |                  |
| Operating Junction and Storage Temperature Range                            |                          | $T_J, T_{stg}$ | -55 to 150 | $^\circ\text{C}$ |

| THERMAL RESISTANCE RATINGS               |                         |                 |         |                    |
|--|-------------------------|-----------------|---------|--------------------|
| Parameter                                |                         | Symbol          | Maximum | Units              |
| Maximum Junction-to-Ambient <sup>a</sup> | $t \leq 10 \text{ sec}$ | $R_{\theta JA}$ | 62.5    | $^\circ\text{C/W}$ |
|  | Steady State            |                 | 110     |                    |

### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

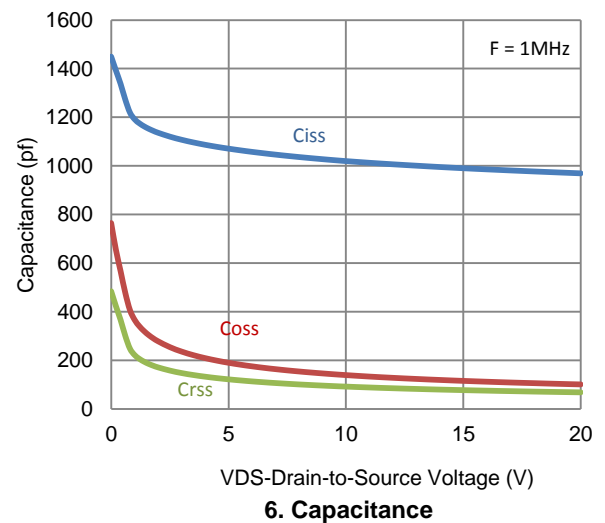
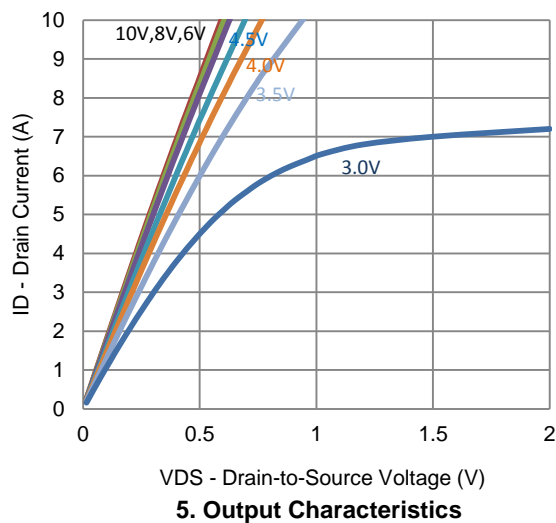
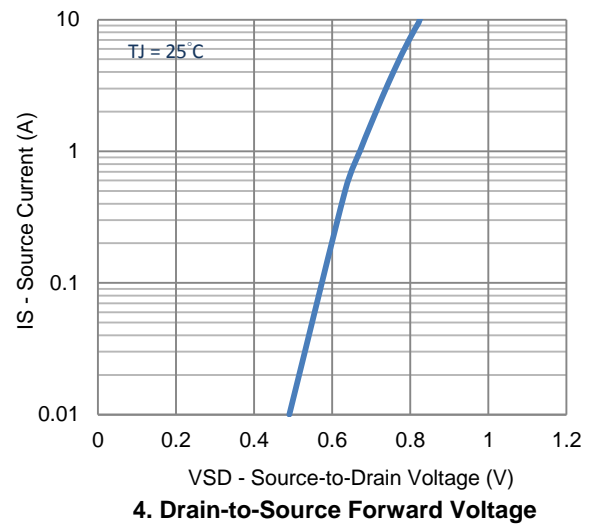
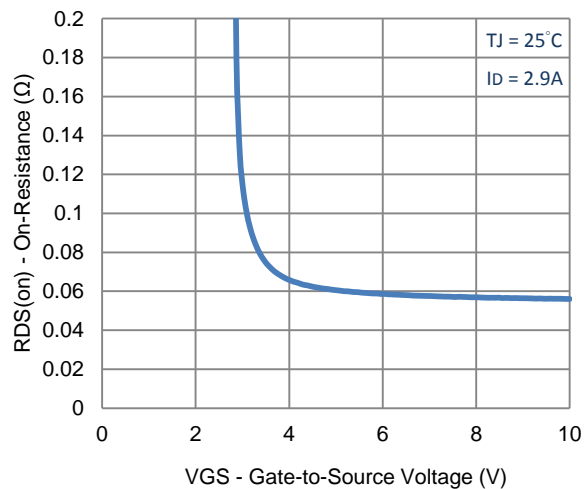
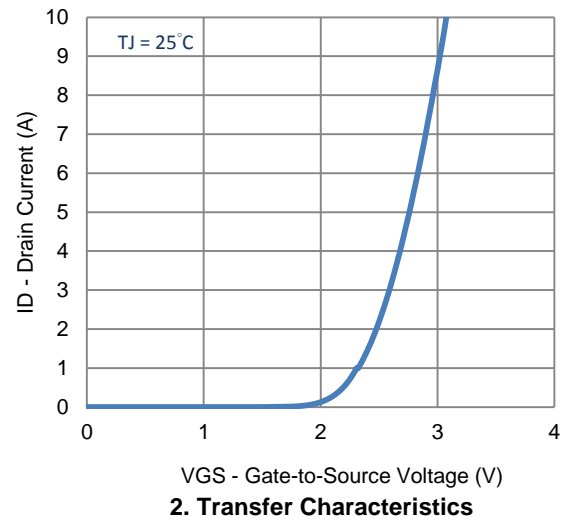
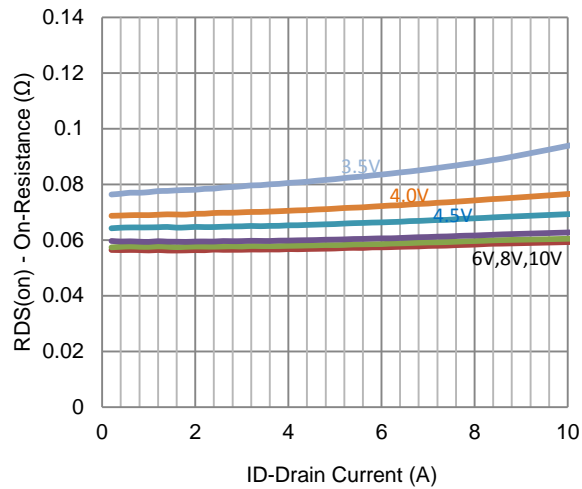
| Parameter                       | Symbol       | Test Conditions  | Min | Typ | Max       | Unit |
|---------------------------------|--------------|--|-----|-----|-----------|------|
| <b>Static</b>                   |              |  |     |     |           |      |
| Gate-Source Threshold Voltage   | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250 \mu A$   | 1   |     | 3.5       | V    |
| Gate-Body Leakage               | $I_{GSS}$    | $V_{DS} = 0 V, V_{GS} = 20 V$  |     |     | $\pm 100$ | nA   |
| Zero Gate Voltage Drain Current | $I_{DSS}$    | $V_{DS} = 80 V, V_{GS} = 0 V$  |     |     | 1         | uA   |
|                                 |              | $V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55^\circ C$  |     |     | 25        |      |
| On-State Drain Current          | $I_{D(on)}$  | $V_{DS} = 5 V, V_{GS} = 10 V$  | 20  |     |           | A    |
| Drain-Source On-Resistance      | $r_{DS(on)}$ | $V_{GS} = 10 V, I_D = 2.9 A$   |     |     | 81        | mΩ   |
|                                 |              | $V_{GS} = 4.5 V, I_D = 2.6 A$  |     |     | 92        |      |
| Forward Transconductance        | $g_{fs}$     | $V_{DS} = 15 V, I_D = 2.9 A$   |     | 20  |           | S    |
| Diode Forward Voltage           | $V_{SD}$     | $I_S = 1.5 A, V_{GS} = 0 V$  |     | 0.7 |           | V    |
| <b>Dynamic</b>                  |              |  |     |     |           |      |
| Total Gate Charge               | $Q_g$        | $V_{DS} = 50 V, V_{GS} = 4.5 V, I_D = 2.9 A$   |     | 17  |           | nC   |
| Gate-Source Charge              | $Q_{gs}$     |  |     | 3.3 |           |      |
| Gate-Drain Charge               | $Q_{gd}$     |  |     | 8.7 |           |      |
| Turn-On Delay Time              | $t_{d(on)}$  | $V_{DD} = 50 V, R_L = 15 \Omega, I_D = 2.9 A,$<br>$V_{GEN} = 10 V, R_{GEN} = 6 \Omega$ |     | 7   |           | ns   |
| Rise Time                       | $t_r$        |  |     | 6.7 |           |      |
| Turn-Off Delay Time             | $t_{d(off)}$ |  |     | 45  |           |      |
| Fall-Time                       | $t_f$        |  |     | 23  |           |      |
| Input Capacitance               | $C_{iss}$    | $V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz$   |     | 990 |           | pF   |
| Output Capacitance              | $C_{oss}$    |  |     | 115 |           |      |
| Reverse Transfer Capacitance    | $C_{rss}$    |  |     | 77  |           |      |

## Notes

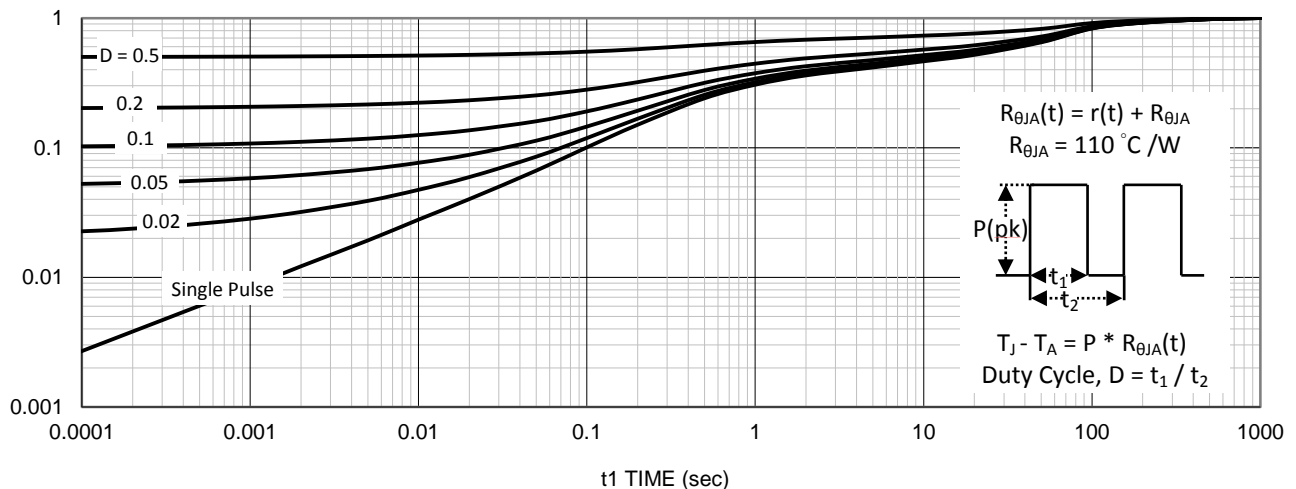
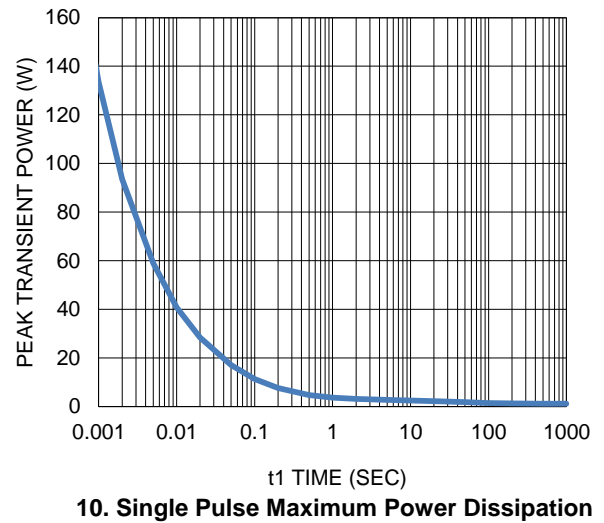
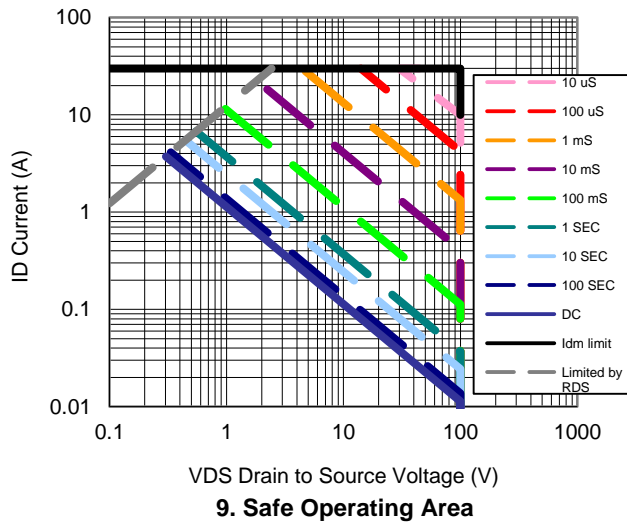
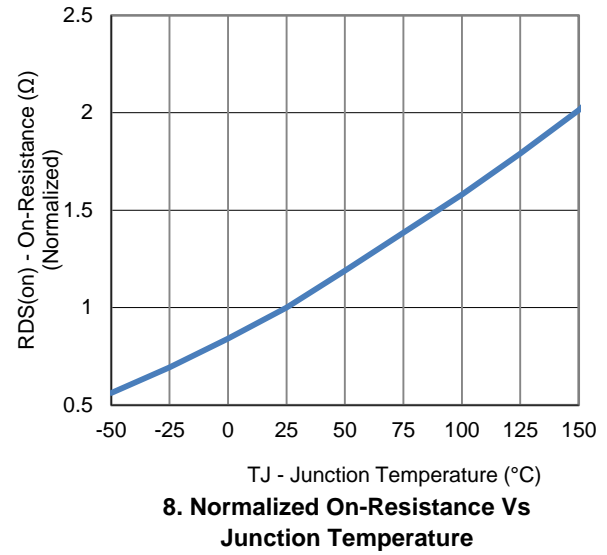
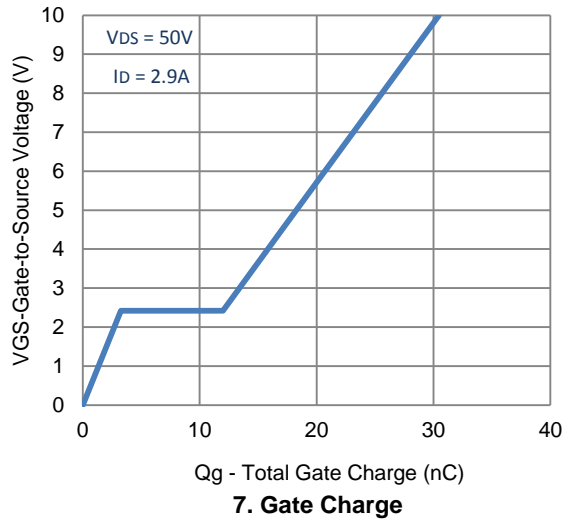
- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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## Typical Electrical Characteristics

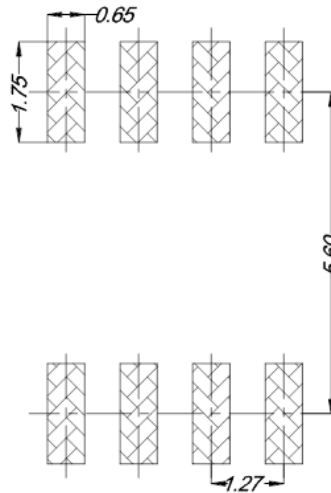
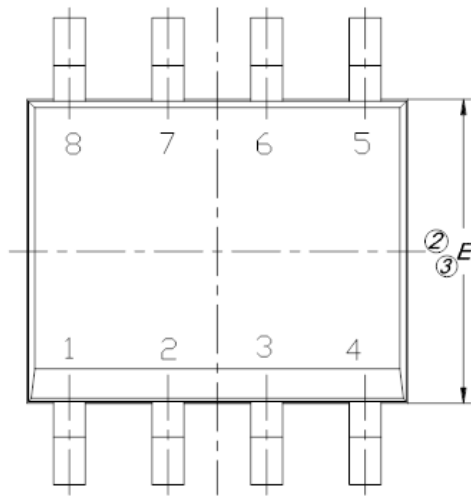


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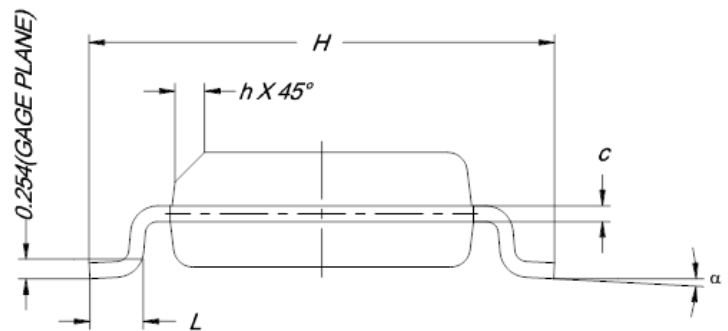
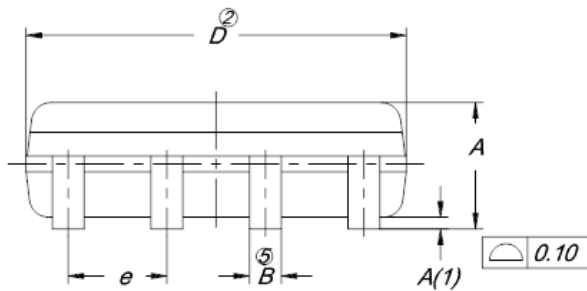


## Package Information

*Land Pattern*  
(Only for Reference)



| DIM.     | MILLIMETERS |      |      |
|----------|-------------|------|------|
|          | MIN.        | NOM. | MAX. |
| A        | 1.35        | 1.55 | 1.75 |
| A(1)     | 0.10        | 0.18 | 0.25 |
| B        | 0.38        | 0.45 | 0.51 |
| C        | 0.19        | 0.22 | 0.25 |
| D        | 4.80        | 4.90 | 5.00 |
| E        | 3.80        | 3.90 | 4.00 |
| e        | 1.27 BSC    |      |      |
| H        | 5.80        | 6.00 | 6.20 |
| L        | 0.50        | 0.72 | 0.93 |
| $\alpha$ | 0°          | 4°   | 8°   |
| h        | 0.25        | 0.38 | 0.50 |



## Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.
5. Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.