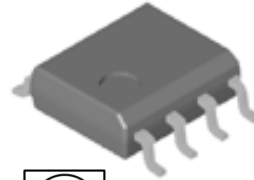


**Dual N-Channel 30-V (D-S) MOSFET**

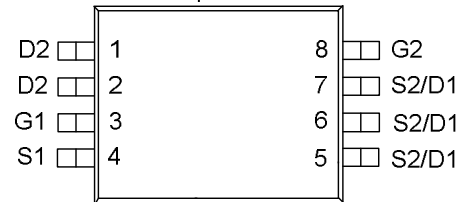
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low  $r_{DS(on)}$  provides higher efficiency extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

SOIC8  
Top View



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	FET#1	FET#1	Units
Drain-Source Voltage	$V_{DS}$	30	30	V
Gate-Source Voltage	$V_{GS}$	20	20	
Continuous Drain Current <sup>a</sup>	$T_A=25^\circ\text{C}$	$I_D$	9.5	A
	$T_A=70^\circ\text{C}$		7.7	
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	40	40	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	4.5	4.5	A
Power Dissipation <sup>a</sup>	$T_A=25^\circ\text{C}$	$P_D$	2.1	W
	$T_A=70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

**THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10 \text{ sec}$	62.5	$^\circ\text{C/W}$
	Steady-State	110	$^\circ\text{C/W}$

## Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

**SPECIFICATIONS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Conditions	Limits				Unit
			FET#	Min	Typ	Max	
Static							
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 uA	1	1			V
		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 uA	2	1			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	1			±100	nA
		V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	2			±100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	1			1	uA
		V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	2			1	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	1	40			A
		V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -10 V	2	40			
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2 A	1			15	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2 A				19	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2 A	2			15	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2 A				23	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 2A	1		0.8		V
		I <sub>S</sub> = -2A	2		0.8		
Forward Tranconductance <sup>A</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2 A	1		64		S
		V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2 A	2		64		
Dynamic							
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =2A	1		3		nC
			2		3		
Gate-Source Charge	Q <sub>gs</sub>		1		1		
			2		1		
Gate-Drain Charge	Q <sub>gd</sub>		1		1		
			2		1		
Turn-On Delay Time	t <sub>d(on)</sub>	N-Chaneel V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, ID=1A , R <sub>GEN</sub> =25Ω, P-Channel V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V, ID=-1A R <sub>GEN</sub> =15Ω	1		5		nS
			2		5		
Rise Time	t <sub>r</sub>		1		5		
			2		5		
Turn-Off Delay Time	t <sub>d(off)</sub>		1		16		
			2		16		
Fall-Time	t <sub>f</sub>		1		7		
			2		7		

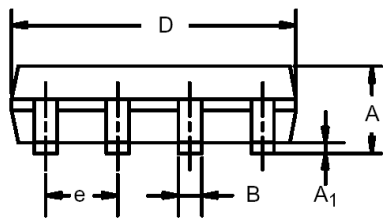
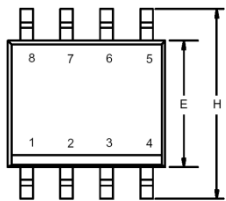
## Notes

- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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Package Information

SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

