P-Channel 20-V (D-S) MOSFET

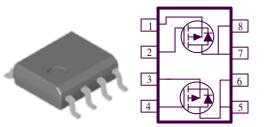
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY				
V _{DS} (V)	$r_{DS(on)} m(\Omega)$ I_D (
	$52 @ V_{GS} = -4.5V$	-4.9		
-20	89 @ $V_{GS} = -2.5V$	-4.0		
	124 @ Vgs = -1.8V	-3.6		

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology







ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)						
Parameter			Maximum	Units		
Drain-Source Voltage		V_{DS}	-20	V		
Gate-Source Voltage		V_{GS}	±12	V		
	T _A =25°C	т	-5.2			
Continuous Drain Current ^a	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	ID	-4.1	A		
Pulsed Drain Current ^b			±50			
Continuous Source Current (Diode Conduction) ^a		I_S	-2.1	A		
D	T _A =25°C	D	2.1	W		
Power Dissipation ^a	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	$P_{\rm D}$	1.3			
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Maximum	Units			
Maximum Junction-to-Case ^a	t <= 5 sec	$R_{ heta JC}$	40	°C/W		
Maximum Junction-to-Ambient ^a	t <= 5 sec	$R_{ heta JA}$	60	°C/W		

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

D 4	G 1.1	T C. 111	Limits			T	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \text{ uA}$	-0.7				
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			±100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA	
Zero Gate Voltage Drain Current	1DSS	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			-5	uA	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = -4.5 \text{ V}, V_{GS} = -10 \text{ V}$	-20			A	
		$V_{GS} = -4.5 \text{ V}, I_D = -4.9 \text{ A}$			52		
Drain-Source On-Resistance ^A	r _{DS(on)}	$V_{GS} = -2.5 \text{ V}, I_D = -4.0 \text{ A}$			89	mΩ	
		$V_{GS} = -1.8 \text{ V}, I_D = -3.6 \text{ A}$			124		
Forward Tranconductance ^A	g_{fs}	$V_{DS} = -15 \text{ V}, I_{D} = -4.9 \text{ A}$		20		S	
Diode Forward Voltage	V_{SD}	$I_S = 2.5 \text{ A}, V_{GS} = 0 \text{ V}$		-0.6		V	
Dynamic ^b							
Total Gate Charge	Q_{g}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$		16.7			
Gate-Source Charge	Q_{gs}	$I_{DS} = -4.9 \text{ A}$		1.8		nC	
Gate-Drain Charge	Q_{gd}			1.9			
Turn-On Delay Time	$t_{d(on)}$			7			
Rise Time	t_r	$V_{DD} = -10 \text{ V}, R_L = 6 \Omega, ID = -1 \text{ A},$		13		nS	
Turn-Off Delay Time	$t_{d(off)}$	VGEN = -4.5 V		14		113	
Fall-Time	t_{f}			9			

Notes

a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.

b. Guaranteed by design, not subject to production testing.

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Typical Electrical Characteristics (P-Channel)

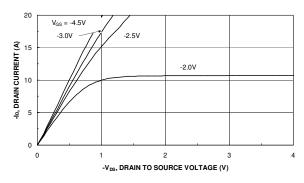


Figure 1. Output Characteristics

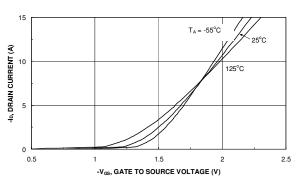


Figure 2. Transfer Characteristics

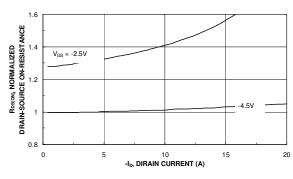


Figure 3. On-Resistance vs. Drain Current

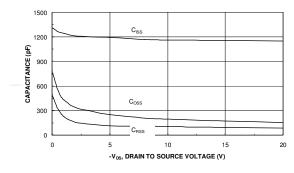


Figure 4. Capacitance

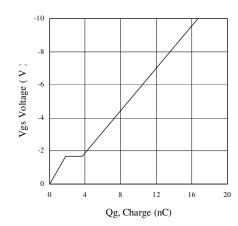


Figure 5. Gate Charge

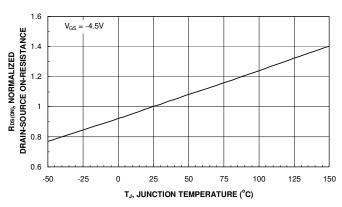
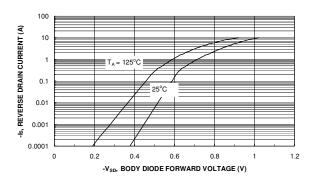


Figure 6. On-Resistance vs. Junction Temperature

Typical Electrical Characteristics (P-Channel)



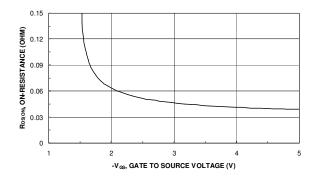


Figure 7. Source-Drain Diode Forward Voltage

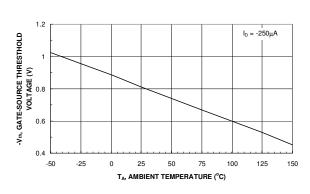


Figure 8. On-Resistance with Gate to Source Voltage

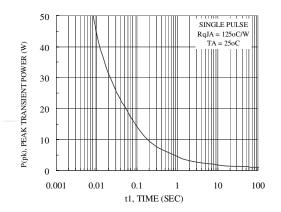


Figure 9. Vth Gate to Source Voltage Vs Temperature

Figure 10. Single Pulse Maximum Power Dissipation

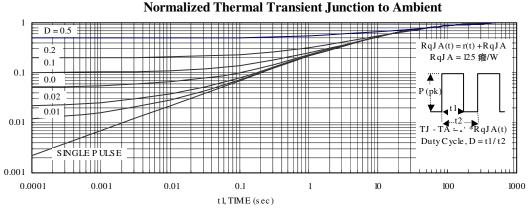
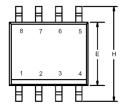
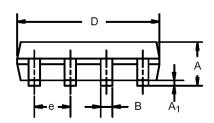


Figure 11. Transient Thermal Response Curve

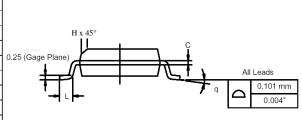
Package Information

SO-8: 8LEAD





	MILLIMETERS I		INC	INCHES	
Dim	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
Е	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	



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