# P-Channel 30-V (D-S) MOSFET

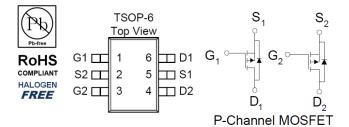
### **Key Features:**

- Low r<sub>DS(on)</sub> trench technology
- · Low thermal impedance
- Fast switching speed

<b>Typical</b>	An	plica	ation	is:
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- · Load Switches
- DC/DC Conversion
- Motor Drives

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$r_{DS(on)}(m\Omega)$	I□ (A)		
-30	58 @ V <sub>GS</sub> = -10V	-3.7		
	97 @ V <sub>GS</sub> = -4.5V	-2.9		



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage		$V_{DS}$	-30	V	
Gate-Source Voltage	$V_{GS}$	±20	V		
Continuous Drain Current a	T <sub>A</sub> =25°C		-3.7		
Continuous Drain Current	T <sub>A</sub> =70°C	i <sub>D</sub>	-2.9	Α	
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	-15	'		
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	-1.3	Α		
Devices Discipation a	T <sub>A</sub> =25°C	P <sub>D</sub>	1.15	W	
Power Dissipation <sup>a</sup>	T <sub>A</sub> =70°C	L.D	0.7	VV	
Operating Junction and Storage Temperature Range		$T_J$ , $T_{stq}$	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter			Maximum	Units	
Maximum Junction-to-Ambient <sup>a</sup>	t <= 10 sec	$R_{\theta JA}$	110	°C/W	
IMAXIMUM Sunction-to-Ambient	Steady State	IΛθJA	150	C/VV	

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#### Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

### **Electrical Characteristics**

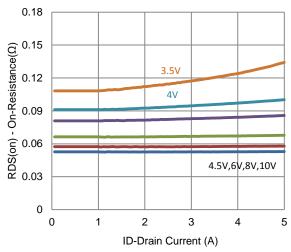
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \text{ uA}$	-1			V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA	
Zara Cata Valtara Duain Comment	1	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			-10	uA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-5			Α	
Drain Cauras On Basistanas a	r	$V_{GS} = -10 \text{ V}, I_D = -3.1 \text{ A}$			58	mΩ	
Drain-Source On-Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS} = -4.5 \text{ V}, I_D = -2.5 \text{ A}$			97	11122	
Forward Transconductance a	g <sub>fs</sub>	$V_{DS} = -15 \text{ V}, I_{D} = -3.1 \text{ A}$		3		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -0.65 \text{ A}, V_{GS} = 0 \text{ V}$		-0.81		V	
		Dynamic <sup>b</sup>					
Total Gate Charge	$Q_g$	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V},$		7.5			
Gate-Source Charge	$Q_{gs}$	$I_{DS} = -13 \text{ V}, \text{ V}_{GS} = -4.3 \text{ V},$ $I_{D} = -3.1 \text{ A}$		2.6		nC	
Gate-Drain Charge	$Q_gd$	10 = 0.1 A		2.7			
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DS} = -15 \text{ V}, R_1 = 4.8 \Omega,$		5			
Rise Time	t <sub>r</sub>	$V_{DS} = -13 \text{ V}, K_L - 4.6 \Omega,$ $I_D = -3.1 \text{ A},$		7		no	
Turn-Off Delay Time	$t_{d(off)}$	$V_{GEN} = -10 \text{ V}, R_{GEN} = 6 \Omega$		25		ns	
Fall Time	t <sub>f</sub>	VGEN = 10 V, NGEN = 0 12		10			
Input Capacitance	C <sub>iss</sub>			684			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ Mhz}$		66		pF	
Reverse Transfer Capacitance	$C_{rss}$			54			

#### Notes

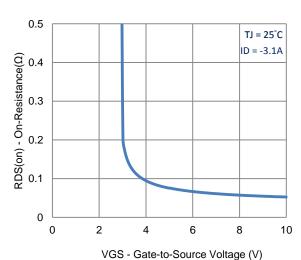
- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

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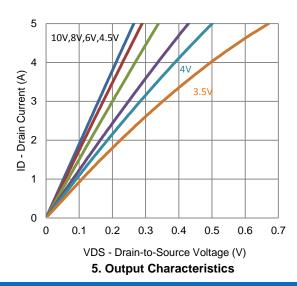
## **Typical Electrical Characteristics**



#### 1. On-Resistance vs. Drain Current

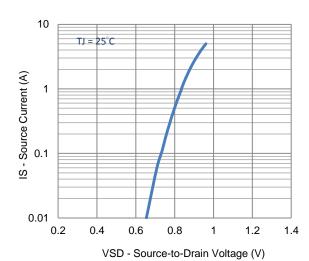


3. On-Resistance vs. Gate-to-Source Voltage

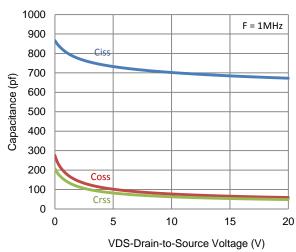


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TJ = 25°C
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(Y)
Tu
auno vieu
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1
0
1
2
3
4
5
VGS - Gate-to-Source Voltage (V)

2. Transfer Characteristics



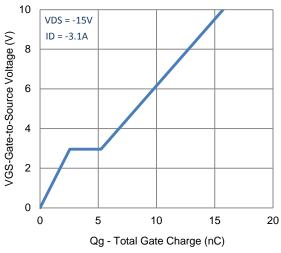
4. Drain-to-Source Forward Voltage

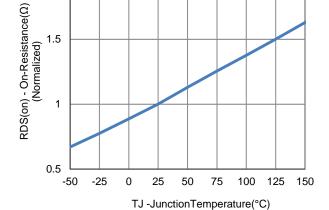


6. Capacitance

### **Typical Electrical Characteristics**

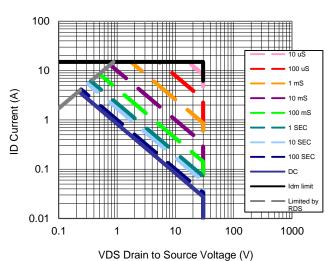
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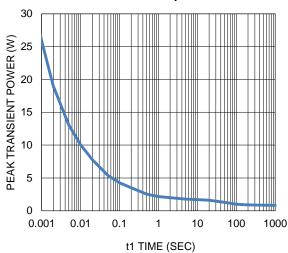




7. Gate Charge

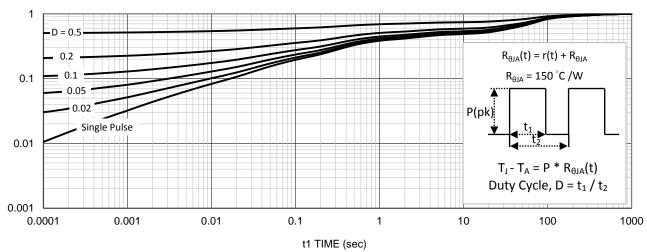






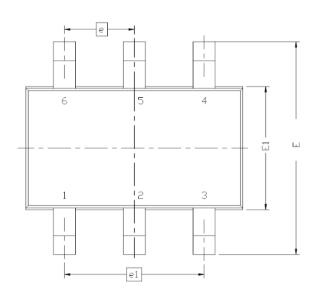
9. Safe Operating Area

10. Single Pulse Maximum Power Dissipation

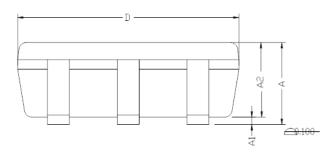


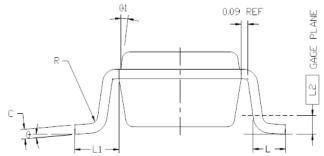
11. Normalized Thermal Transient Junction to Ambient

### **Package Information**



DIM.	MILLIMETERS					
DIN.	MIN	NDM	MAX			
Α	0.935		1.10			
A1	0.01		0.10			
A2	0.70		1.00			
b	0.25	0.32	0.40			
C	0.10	0.15	0.20			
D	2.95	3.05	3.10			
Ε	2.70	2.85	2.98			
E1	1.55	1.65	1.70			
6	0.95 BSC					
L	0.30		0.60			
L1	0.60REF					
L2	0.25BSC					
R	0.10					
θ	0?	4?	8?			
θ1	7? N□M					





#### Note:

- 1. All Dimension Are In mm.
- 2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.