Highly Integration Single Phase Full-Wave H-Bridge For AM2936

● Features and Benefits

1). Wide supply voltage range up to 18V
2). Max Output current up to 4.1A
3). Low $R_{DS(ON)}$ 75 mΩ for high efficient H-bridge output
4). Built-in precise LDO Regulator 5.0V±3%
5). QFN4X4 package for small size PCB layout
6). Rotating speed pulse signal (FG) output.
7). Halogen-Free Green Product & RoHS compliant package.
8). Over Voltage Protection
9). Thermal Shut Down Protection

● Application

1). Server Fan
2). Industrial Fan
3). Any relevant DC motor application

● Description

The AM2936 is a highly integrated driver optimized for one channel H-Bridge driver. The IC has a built-in precise low dropout regulator (LDO) and provides integrated motor-driver solution for high current power motion control applications. The output driver block consists of N-channel and P-channel power MOSFETs configured as an H-Bridge to driver DC motor.

AM2936 is design for servo fan application which could efficiently design-in time to market and save the whole fan cost.

The AM2936 maximum operation voltage is 18V. It can supply up to 4.1A of output peak current.

Package material is Halogen-Free Green Product & RoHS compliant for the purpose of environmental protection and for sustainable development of the Earth

● Absolute Maximum Ratings (T_A=25℃)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	30	V
Drain-Source Voltage(Power MOS)	Vdss	30	V
Gate-Source Voltage(Power MOS)	Vgss	±20	V
Output current (Duty cycle = 100%)	Iout	4.1	A
FG single output current	I_{FG}	10	mA
FG single output voltage	V_{FG}	18	V
Power dissipation (JEDEC 2S2P PCB)	Pd	3080	mW
Operate temperature range	T_{opr}	-40～+105	℃
Storage temperature range	T_{stg}	-40～+150	℃
Junction temperature	Tjmax	150	℃

* Pd de-rated by 28 mW/°C over 25℃ (based on JEDEC 2S2P board)

Those are stress rating only and functional operating at those conditions for extended periods may damage to the device.

● Ordering Information

Orderable Part Number	Package	Marking
AM2936	QFN 4X4	AM2936

● Recommended operating conditions (T_A =25℃)

(Set the power supply voltage taking allowable dissipation into considering)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply voltage for H-Bridge	PVCC	5.5	12	18	V
Power Supply voltage	VCC	5.5	12	18	V
Input signal voltage PWM_x	V_{IN}	-0.3	5	5.2	V
Externally applied PWM frequency	F_{PWM}	20		100	KHz

Note: The LDO 5.0V operation range should be considered in choosing VCC.

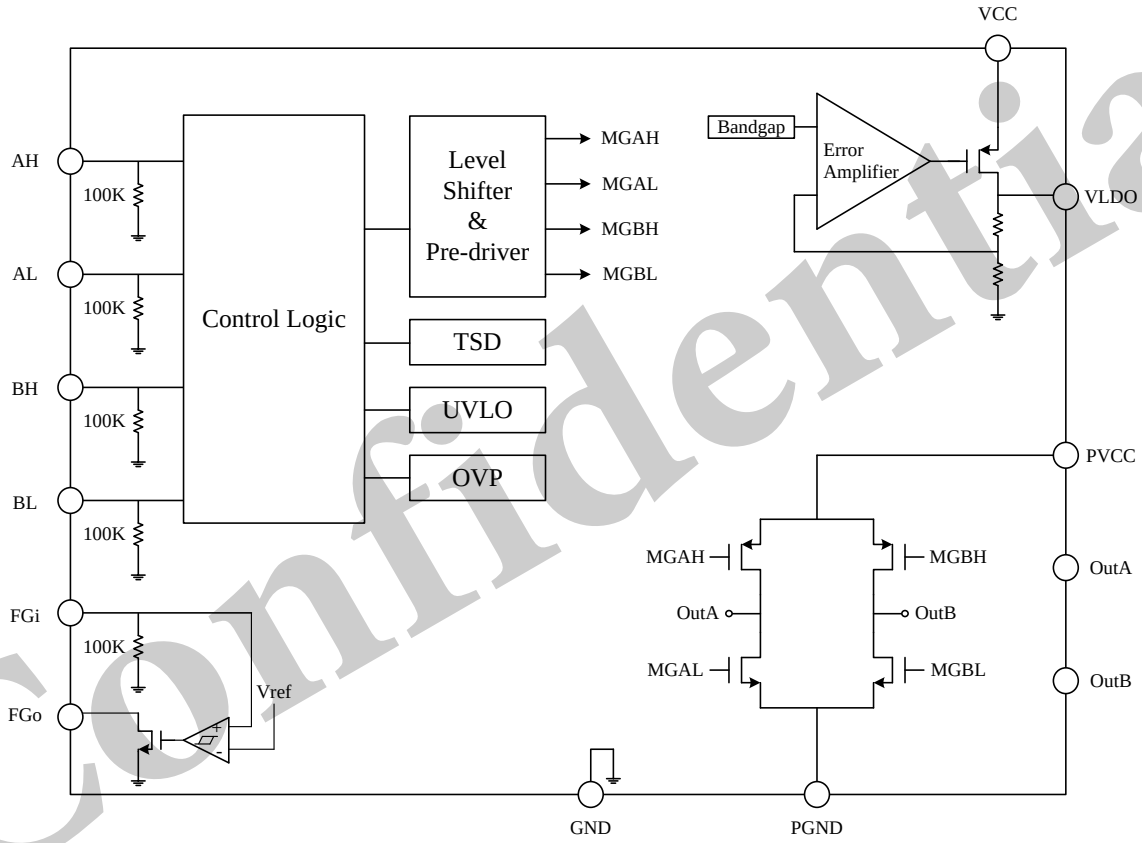
● Electrical Characteristics (Unless otherwise specified, TA = 25℃,PVCC=VCC=12V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Power Supplies						
Supply current	I_{CC}		0.5		mA	Input Signal： LDO & Output=No Loading
PWM_x Inputs						
Input H level voltage	V_{IN_xH}	2.5		5.2	V	
Input L level voltage	V_{IN_xL}	0		1.0	V	
Input frequency	F_{IN_x}	20		100	KHz	
Input pull down resistance	Ripd		100		KΩ	
H-bridge FETs						
On-resistance	$R_{ds(on)}$		75	95	mΩ	I_O = 1A Upper + Lower FET
FG Input						
FG high Voltage	V_{FGH}	2.5	—	—	V	
FG low voltage	V_{FGL}	—	—	1.0	V	
FG output driving capability	V_{FGout}		0.4			5mA
FG output leakage current	I_{FGL}	—	—	10.0	μA	V_{FG} = 12V
LDO parameter						
LDO output voltage	V_{LDO}	4.85	5	5.15	V	I_{LDO} = 5mA, VCC = 12V
Dropout voltage	V_{DO}	—	300	400	mV	I_{LDO} =100mA

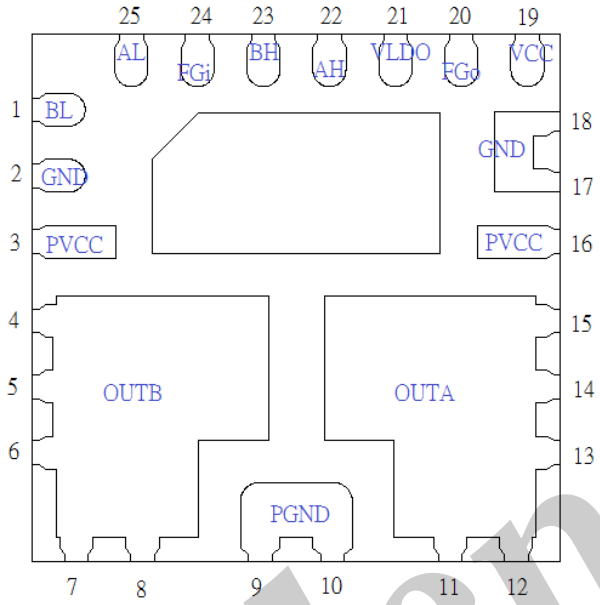
Truth table

	AH	AL	BH	BL	OUTA	OUTB
Phase A	0	1	1	0	L	H
	0	0	1	0	Z	H
Phase B	1	0	0	1	H	L
	1	0	0	0	H	Z

Block Diagram



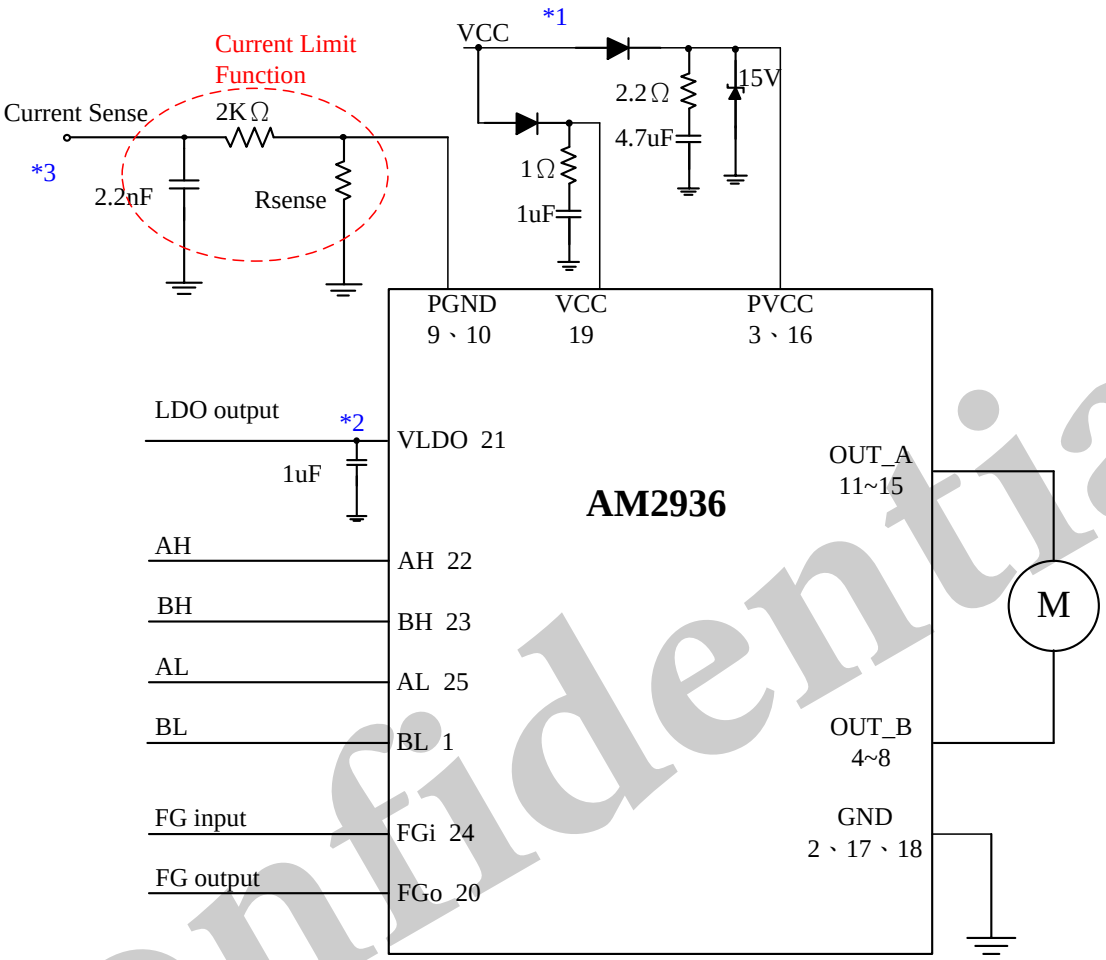
● Pin configuration QFN 4X4-25L



● Pin Descriptions

Pin Number	Pin Name	I/O	Description
1	BL	I	Input BL
2、17、18	GND	-	Ground
3、16	PVCC	I	Power supply for Power MOS
4~8	OUT_B	O	Motor output B terminal
9~10	PGND	-	Power Ground
11~15	OUT_A	O	Motor output A terminal
19	VCC	I	Power supply terminal
20	FGo	O	FG output
21	VLDO	O	LDO Output
22	AH	I	Input AH
23	BH	I	Input BH
24	FGi	I	FG input
25	AL	I	Input AL

Application Circuit



Description:

1. PVCC is for IC MOS FET Power. It must put a Schottky diode and a Zener diode for protection. Vcc is for IC control circuit. It must put a Schottky diode for protection.
2. Two of PVCC Pin (Pin3 and Pin16) must all connect to PVCC.
3. LDO is for MCU Power. It should put a capacitor for power stability.
4. If fan need a current limit function, it could add the circuit above and connect to MCU current sense pin.

● Thermal Information

Θja	junction-to-ambient thermal resistance	35.7 ℃/W
Ψjt	junction-to-top characterization parameter	0.31 ℃/W

- **Θja** is obtained in a simulation on a JEDEC-standard 2s2p board as specified in JESD-51.
- The **Θja** number listed above gives an estimate of how much temperature rise is expected if the device was mounted on a standard JEDEC board.
- When mounted on the actual PCB, the **Θja** value of JEDEC board is totally different than the **Θja** value of actual PCB.
- **Ψjt** is extracted from the simulation data to obtain **Θja** using a procedure described in JESD-51, which estimates the junction temperature of a device in an actual PCB.
- The thermal characterization parameter, **Ψjt**, is proportional to the temperature difference between the top of the package and the junction temperature. Hence, it is useful value for an engineer verifying device temperature in an actual PCB environment as described in JEDEC JESD-51-12.
- When Greek letters are not available, **Ψjt** is written Psi-jt.
- Definition:

$$\text{DFEINITION:}\Psi_{jt} = (T_j - T_t) / P_d$$

Where :

Ψjt (Psi-jt) = Junction-to-Top(of the package) °C/W
Tj= Die Junction Temp. °C
Tt= Top of package Temp at center. °C
Pd= Power dissipation. Watts

- Practically, most of the device heat goes into the PCB, there is a very low heat flow through top of the package, So the temperature difference between **Tj** and **Tt** shall be small, that is any error caused by PCB variation is small.
- This constant represents that **Ψjt** is completely PCB independent and could be used to predict the **Tj** in the environment of the actual PCB if **Tt** is measured properly.

- **How to predict Tj in the environment of the actual PCB**

Step 1 : Used the simulated **Ψjt** value listed above.

Step 2 : Measure **Tt** value by using

- **Thermocouple Method**

  We recommend use of a small ~40 gauge(3.15mil diameter) thermocouple. The bead and thermocouples wires should touch the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires should be heat-insulated to prevent cooling of the bead due to heat loss into wires. This is important towards preventing “too cool” **Tt** measurements, which would lead to the calculated **Tj** also being too cool.

- **IR Spot Method**

  An IR Spot method should be utilized only when using a tool with a small enough spot area to acquire the true top center “hot spot”.
  Many so-called “small spot size” tools still have a measurement area of 0~100+mils at “zero” distance of the tool from the surface. This spot area is too big for many smaller packages and likely would result in cooler readings than the small thermocouple method.
  Consequently, to match between spot area and package surface size is important while measuring **Tt** with IR sport method.

Step 3 : calculating power dissipation by

$$P \cong (VCC - |Vo_{\_Hi} - Vo_{\_Lo}|) \times I_{out} + VCC \times Icc$$

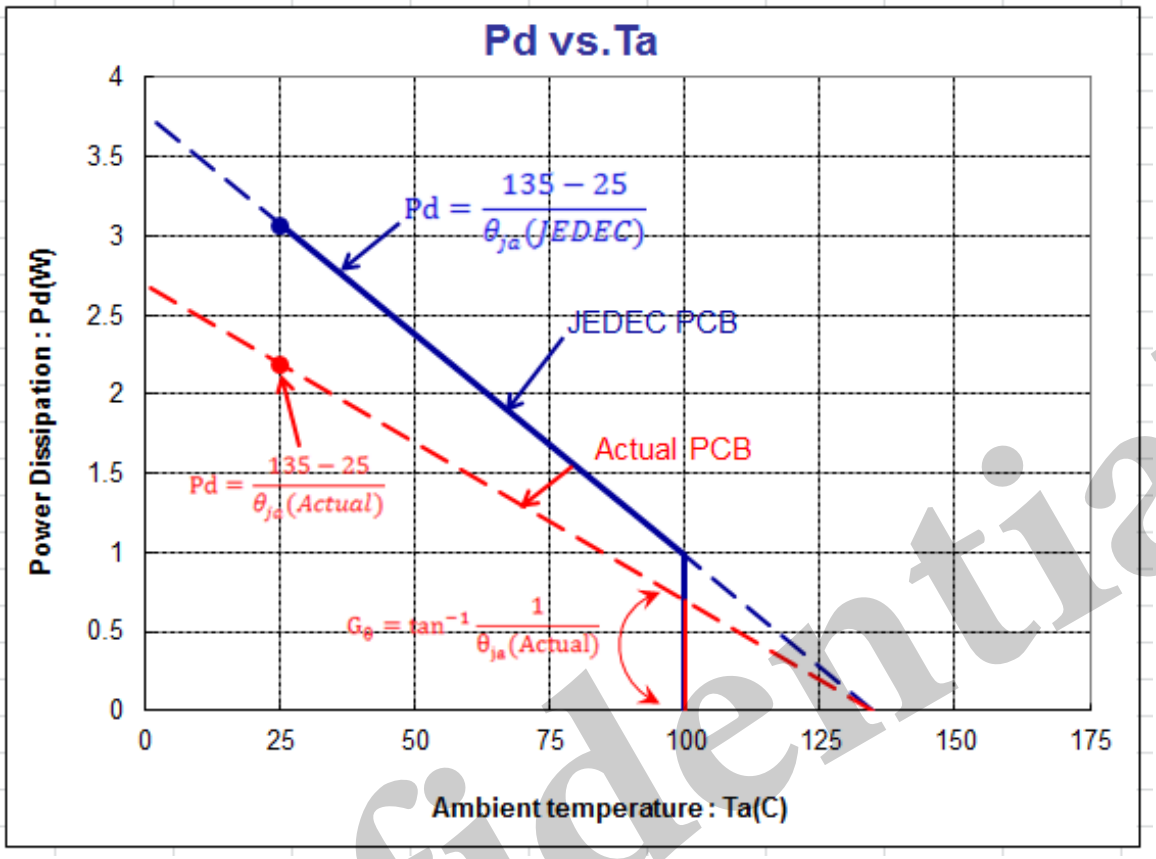
Step 4 : Estimate **Tj** value by

$$Tj = \Psi jt \times P + Tt$$

Step 5: Calculated Θja value of actual PCB by the known **Tj**

$$\Theta ja(actual) = (Tj - Ta)/P$$

Maximum Power Dissipation (de-rating curve) under JEDEC PCB & actual PCB



● Application Notes

1) PVCC bypass capacitor

The PVCC bypass capacitor not only can reduce the PVCC voltage variation but also can bypass the energy from loading motor. The capacitor value depends on the value of the PVCC and motor loading. In general, a 4.7uF capacitor is recommended for normal application. If the large voltage power or a heavy loading motor is used, a larger capacitor should be chosen.

The user must place a bypass capacitor rated for PVCC as close as possible to the PVCC and PG_A / PG_B pin.

2) LDO bypass capacitor

Suggest connecting a 1.0uF between LDO and GND. It may reduce the voltage variation during loading change or supply voltage change. For PCB design consideration, the capacitor should be put near LDO pin as close as possible.

3) FG function

This FG pin is made up with an open drain output. Recommend connect a resistance of 10k ohm to supply.

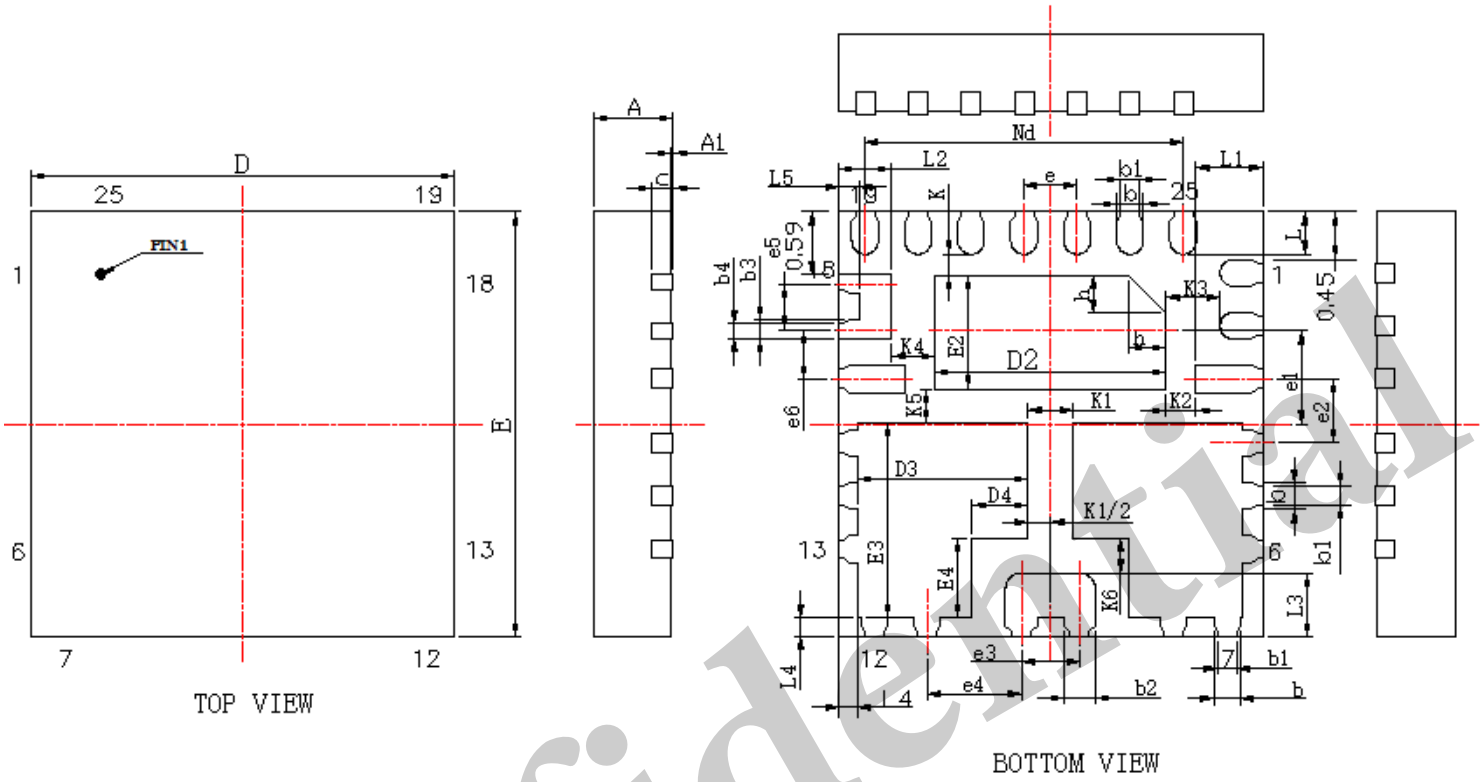
4) Thermal design and Thermal shutdown

The thermal design should allow enough margins for actual power dissipation. In case the IC is left running over the allowable loss, the junction temperature rises, and the thermal-shutdown circuit works at the junction temperature of 150°C (typ.) (output high side P-MOS turn off). When the junction temperature drops to 105°C (typ.), the IC start operating again.

5) OVP (Over Voltage Protection)

Over Voltage Protection is setting at 25V(typ.). Hysteresis setting 1V.

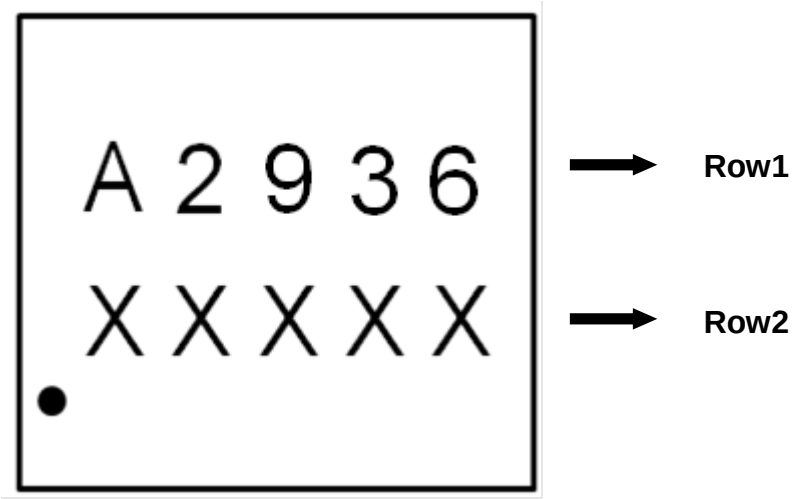
● **Packaging outline --- QFN 4x4** **Unit : mm**



SYMBOL	MILLIMETERS			INCHES		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	--	0.05	0.000	--	0.002
c	0.20 REF			0.008 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.18 REF			0.007 REF		
b2	0.25	0.30	0.35	0.010	0.012	0.014
b3	0.13	0.18	0.23	0.005	0.007	0.009
b4	0.10	0.15	0.20	0.004	0.006	0.008
D	3.90	4.00	4.10	0.154	0.157	0.161
D2	2.08	2.18	2.28	0.082	0.086	0.090
D3	1.505	1.605	1.705	0.059	0.063	0.067
D4	0.43	0.53	0.63	0.017	0.021	0.025
E	3.90	4.00	4.10	0.154	0.157	0.161
E2	0.97	1.07	1.17	0.038	0.042	0.046
E3	1.73	1.83	1.93	0.068	0.072	0.076
E4	0.635	0.735	0.835	0.025	0.029	0.033
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.578	0.628	0.678	0.023	0.025	0.027
L2	0.45	0.50	0.55	0.018	0.020	0.022

L3	**0.55**	**0.60**	**0.65**	**0.022**	**0.024**	**0.026**
L4	**0.135**	**0.185**	**0.235**	**0.005**	**0.007**	**0.009**
L5	**0.15**	**0.20**	**0.25**	**0.006**	**0.008**	**0.010**
e	**0.50 BSC**			**0.002 BSC**		
e1	**0.880 BSC**			**0.035 BSC**		
e2	**0.60 BSC**			**0.024 BSC**		
e3	**0.55 BSC**			**0.022 BSC**		
e4	**0.89 BSC**			**0.035 BSC**		
e5	**0.43 BSC**			**0.017 BSC**		
e6	**0.465 BSC**			**0.018 BSC**		
Nd	**3.00 BSC**			**0.118 BSC**		
K	**0.20 REF**			**0.008 REF**		
K1	**0.42 REF**			**0.017 REF**		
K2	**0.282 REF**			**0.011 REF**		
K3	**0.51 REF**			**0.020 REF**		
K4	**0.41 REF**			**0.016 REF**		
K5	**0.315 REF**			**0.012 REF**		
K6	**0.320 REF**			**0.013 REF**		
h	**0.30**	**0.35**	**0.40**	**0.012**	**0.014**	**0.016**

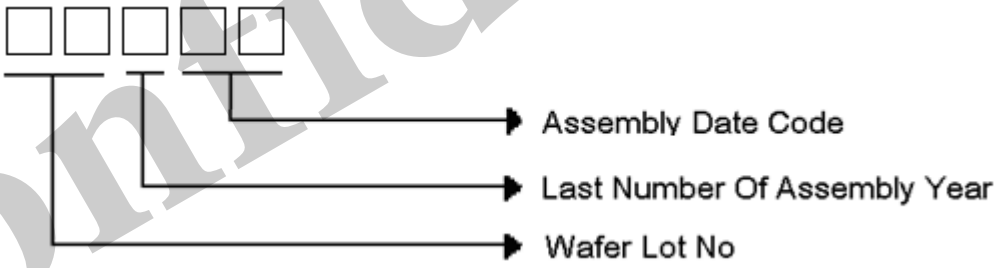
● **Marking Identification**



NOTE:

Row1 ：Device Name

Row2 ：Wafer Lot No use two codes、Assembly Year use one code、Assembly Week use two codes



Example: Wafer lot no is AF + Year 2017 is H + Week 29 is 29，we type〝AFH29〞
The last code of assembly year, explanation as below:
(Year： A=0,B=1,C=2,D=3,E=4,F=5,G=6,H=7,I=8,J=9. For example: year 2017=H)