Am2533/2833

1024-Bit Static Shift Registers

Complex Digital Integrated Circuits

Distinctive Characteristics

- Second source to Signetics 2533
- All inputs are low-level DTL/TTL compatible
- Static operation with single clock input.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- DC to 2.0MHz operation with Am2833

FUNCTIONAL DESCRIPTION

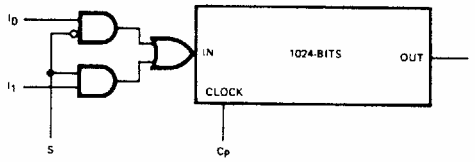
The Am2533/2833 is a quasi-static 1024-bit MOS shift register using low-threshold P-channel silicon gate technology.

The device has a single TTL/DTL compatible clock input, Cp. Data in the register is stored in static, cross-coupled latches while the clock is LOW, so that the clock may be stopped indefinitely in the LOW state. When the clock shifts from LOW to HIGH to LOW a dynamic transfer of data occurs from one static latch to the next. The input of the register is a two-input multiplexer with both data inputs available. A select line, S, determines whether data will be accepted from the I_0 input (S = LOW) or the I_1 input (S = HIGH). The register can be placed in the recirculate mode by tying the output, O, to one of the data inputs, and using the select line as a write/recirculate control. The Am2833 is functionally identical to the Am2533 but has superior performance over an extended temperature range.

LOGIC SYMBOL

V_{CC} = Pin 8
V_{GG} = Pin 2
V_{DD} = Pin 4

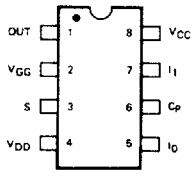
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am2533 Order Number	Am2833 Order Number
Molded DIP	0°C to +70°C	AM2533V	AM2833PC
Hermetic DIP	0°C to +70°C	AM2533DC	AM2833DC
Hermetic DIP	−55°C to +125°C		AM2833DM

CONNECTION DIAGRAM
Top View



Note: Pin 1 marked for orientation

MAXIMUM RATING (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −20V to V_{SS} +0.3V

OPERATING RANGE

Part No.	Temperature	V_{CC}	V_{GG}
Am2533PC/Am2833PC Am2533DC/Am2833DC	0°C to 70°C	5.0V ±5%	−12.0V ±5%
Am2833DM	−55°C to +125°C	5.0V ±5%	−12.0V ±5%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −100μA		2.4	3.5		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 1.6mA			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	Am2533	V_{CC}−1.8		V_{CC}+0.3	Volts
			Am2833 (Note 3)	2.0		V_{CC}+0.3	
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		V_{GG}		0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0V, T_A = 25°C			10	500	nA
I_{IH}	Input HIGH Current	T_A = 25°C, V_{IN} = V_{CC} −1.0 (Note 3)		−150	−300	−500	μA
I_{IT}	Peak input transition current (Note 3)	2.5 ≤ V −V_{IN} ≤ 4.0, T_A = 25°C				−1.6	mA
V_{Imax}	Voltage at maximum input current	T_A = 25°C		V_{SS}−4.0	V_{SS}−3.0	V_{SS}−2.5	V
I_{CC}	V_{CC} Power Supply Current	f = 1.5MHz	Am2533		16	30	mA
		f = 2.0MHz	Am2833PC, DC		16	54	
			Am2833DM		20	70	
I_{GG}	V_{GG} Power Supply Current	f = 1.5MHz	Am2533		−5.0	−7.5	mA
		f = 2.0MHz	Am2833PC, DC		−5.0	−14	
			Am2833DM		−7.0	−18	

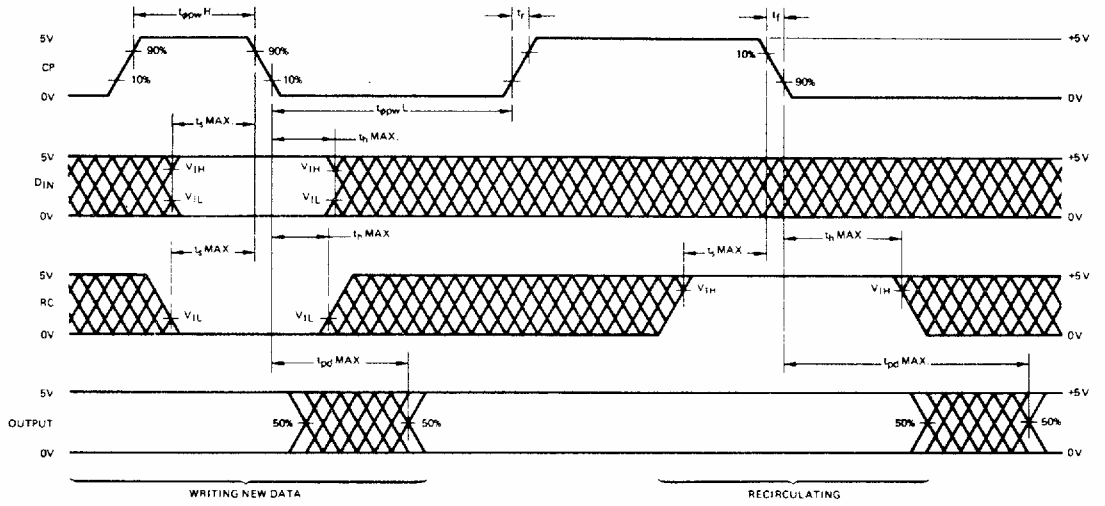
Notes: 1. Typical limits are at V_{CC} = 5.0V, V_{GG} = −12V, 25°C ambient.
2. Power supply currents are with inputs and outputs open.
3. A special input pull-up circuit becomes active at V_{IN} = V_{SS} −3.5V to pull the internal input node up to the MOS threshold. To return the internal node to the LOW state, current must be drawn from the MOS input. This current is maximum at approximately 2.0V.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

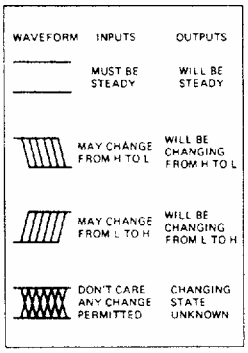
Parameters	Description	Test Conditions	Am2533 Min.	Am2533 Typ. (Note 1)	Am2533 Max.	Am2833 Min.	Am2833 Typ. (Note 1)	Am2833 Max.	Units
f_{max}	Maximum Clock Frequency		1.5	2.0		2.0	3.0		MHz
$t_{\phi pw}L$	Clock LOW Time		0.250		∞	0.200		∞	μs
$t_{\phi pw}H$	Clock HIGH Time		0.350		100	0.250		100	μs
t_r, t_f	Clock Rise and Fall Times				1			1	μs
$t_s(I)$	Set-up Time, I_0 or I_1 Input (see definitions)	t_r = t_f ≤ 25ns			50			50	ns
$t_h(I)$	Hold Time, I_0 or I_1 Input (see definitions)				50			50	ns
$t_s(S)$	Set-up Time, S Input (see definitions)				80			80	ns
$t_h(S)$	Hold Time, S Input (see definitions)				50			50	ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 2.9k, C_L = 20pF			300			300	ns
t_{pr}, t_{pf}	Output Rise and Fall Times	10% to 90%			150			150	ns
C_{in}	Capacitance, Any Input (Note 2)	f = 1MHz, V_{IN} = V_{CC}		3	5		3	5	pF

Notes: 1. Typical limits are at V_{CC} = 5.0V, V_{GG} = −12.0V and T_A = 25°C
2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

TIMING DIAGRAM

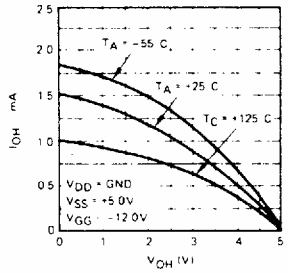


KEY TO TIMING DIAGRAM

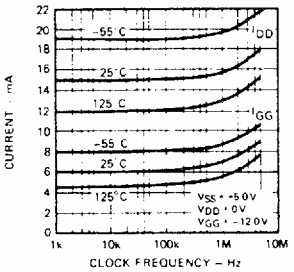


PERFORMANCE CURVES

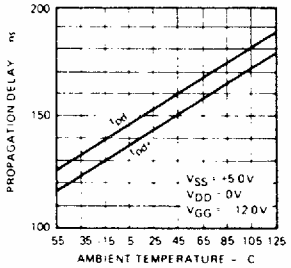
Typical Data Output HIGH Current Versus Data Output Voltage



Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature



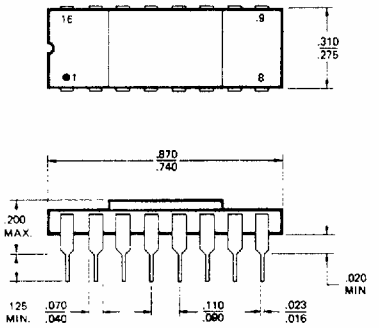
DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

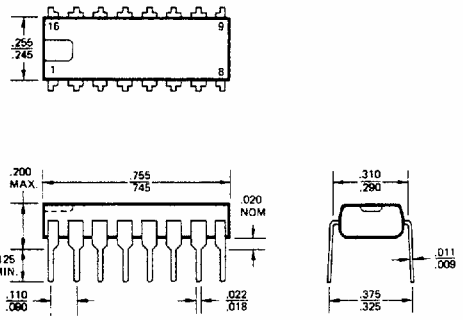
SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Side Brazed

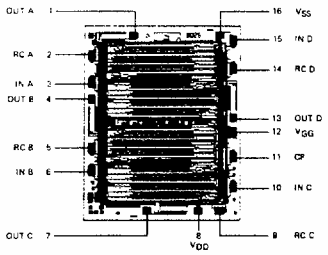


16-Pin Molded



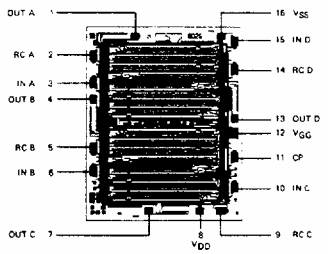
Metallization and Pad Layouts

Am2847



DIE SIZE 0.106" X 0.128"

Am2896



DIE SIZE 0.106" X 0.128"