4096-Bit (1024 x 4) Bipolar Registered PROM with SSR TM Diagnostics Capability

#### DISTINCTIVE CHARACTERISTICS

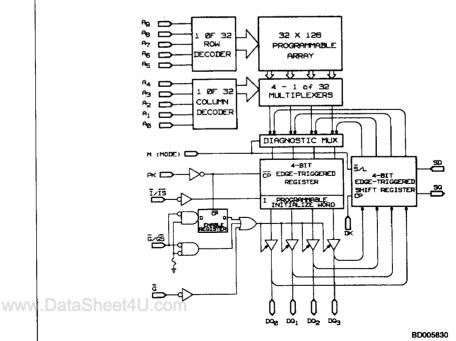
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable Enable Pin for Asynchronous or Synchronous Enable operation
- User-programmable Initialization Pin for Asynchronous or Synchronous Initialize operation
- Slim, 24-pin, 300-mil lateral center package permits a reduction in board space over standard discrete PROM and registers
- Consumes approximately ½2 the power of separate PROM/register combination for improved system reliability
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%)
- Increased drive capability, 24 mA lor

#### GENERAL DESCRIPTION

This device contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies, the shadow register is intended to operate in the background of the normal output data register. This shadow register can be used in a systematic way to control and observe the output data register to exercise desired system functions during a diagnostic test mode.

To offer the system designer maximum flexibility, this device contains user-programmable architecture for Enable and Initialize. The unprogrammed state of these pins operates as Asynchronous inputs (G) and (I), respectively. An architecture word permits the programming of the functionality of these pins to Synchronous Enable (GS) and Synchronous Initialize (IS). A non-programmable Asynchronous Enable (G) is also provided.





SSR is a trademark of Advanced Micro Devices, Inc.

Publication # Rey. Amendment 05271 C /0 Issue Date: May 1988

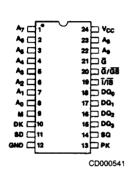
# /

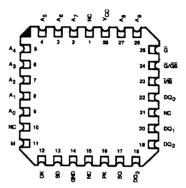
## PRODUCT SELECTOR GUIDE

Part Number	27S65A	27\$65	27S65A	27S65
Address Set-up Time	23 ns	30 ns	27 ns	35 ns
Clock-to-Output Delay	10 ns	15 ns	13 ns	20 ns
Operating Range	С	С	М	М

## **CONNECTION DIAGRAMS**

**Top View** 

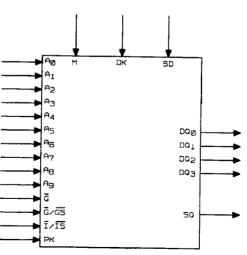




CD004901

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



www.DataSheet4U.com

LS002100