Am27S43/27S43A

32,768-Bit (4096x8) Bipolar PROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Ultra-fast access time
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 96%)

GENERAL DESCRIPTION

The Am27S43 (4096 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs compatible with lowpower Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls.



BLOCK DIAGRAM

PRODUCT SELECTOR GUIDE

Part Number	Am27	'S43A	Am27\$43	
Address Access Time	40 ns	55 ns	55 ns	65 n:
Operating Range	с	м	с	м
Limiña				
A.				
0				



*Also available in 24-Pin Flatpack. Pinout identical to DIPs.

Note: Pin 1 is marked for orientation.





ORDERING INFORMATION

Standard Products



Valid Co	mbinations					
AM27S43	DC, DCB, PC, PCB,					
AM27S43A	LC, LCB, LC-S, LCB-S					

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: a. Device Number



Valid Combinations							
AM27S43	/BJA, /BKA,						
AM27S43A	/BUA, /B3A						

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

A₀-A₁₁ Address (inputs)

The 12-bit field presented at the address inputs selects one of 4,096 memory locations to be read from.

Q0-Q7 Data Output Port

The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which when disabled are in a floating or highimpedance state.

G1,G2 Output Enable (Input)

Provides direct control of the Q-output, three-state buffers. Outputs disabled forces all outputs to to a floating or highimpedance state.

Enable =
$$\overline{G_1 \cdot G_2}$$

Disable = $\overline{G_1 \cdot G_2}$
= $G_1 \cdot \overline{G_2}$

V_{CC} Device Power Supply Pin The most positive of the logic power supply pins.

Device Power Supply Pin GND

The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature65 to +150°C
Ambient Temperature with
Power Applied55 to +125°C
Supply Voltage0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming)0.5 V to +Voc Max.
DC Voltage Applied to Outputs
During Programming 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec)
DC Input Voltage0.5 V to +5.5 V
DC Input Current30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_{C} = +25°C, +125°C, and -55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Тур.	Max.	Uni
Voн	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 m V _{IN} = V _{IH} or V _{IL}	2.4			v	
VOL	Output LOW Voltage	V _{CC} = Min., I _{OL} = 16 mA V _{IN} = V _{IH} or V _{IL}	1		0.50	٧	
VIH	Input HIGH Level	Guaranteed input logical voltage for all inputs (No	2.0			v	
VIL	Input LOW Level	Guaranteed input logical voltage for all inputs (No	<u> </u>		0.8	v	
ht	Input LOW Current	VCC = Max., VIN = 0.45 V			<u> </u>	-0.250	mА
Чн	Input HIGH Current	VCC = Max., VIN = VCC	<u> </u>		40	μA	
Isc	Output Short-Circuit Current	V _{CC} = Max., V _{OUT} = 0.0	- 15		-100	mA	
ICC	Power Supply Current	All inputs = GND,	COM'L	1		185	
	· end copply callent	VCC = Max. MIL				185	mA
VI	Input Clamp Voltage	V _{CC} = Min., I _{IN} = -18 mA	·····	· · · · ·	-1.2	v	
ICEX	Output Leakage Current	V _{CC} = Max.	$V_0 = V_{CC}$	1		40	μA
-062		VG1 = 2.4 V		r	-40		
CłN	Input Capacitance	VIN = 2.0 V @ f = 1 MHz VCC = 5 V, TA = 25°C		5.0			
COUT	Output Capacitance	VOUT = 2.0 V @ f = 1 MI VCC = 5 V, TA = 25°C		8.0		pF	

Notes: 1. VIL and VIH are input conditions of output tests and are not themselves directly tested. VIL and VIH are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Not more than one output should be shorted at a time. Duration of the short-circuit test should not be more than one second.
 These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*)

Parameter No. Symbol			Am27S43A				Am27S43				1
			COM'L		MIL		COM'L		MIL		1
	Parameter Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	
1	TAVQV	Address Valid to Output Valid Access Time		40		55		55		65	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		30		35		35		40	ns
з	TGVQV	Delay from Output Enable Valid to Output Valid		30		35		35		40	ns

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.

2. TGVOZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels.

*Subgroups 7 and 8 apply to functional tests.

SWITCHING TEST CIRCUIT



- Notes: 1. TAVQV is tested with Switch S₁ closed and C_L = 30 pF.
 2. For three-state outputs, TGVQV is tested with C_L = 30 pF to the 1.5 V level; S₁ is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. TGVQZ is tested with C_L = 5 pF. HIGH to high-impedance tests are made with S₁ open to an output voltage of V_{OH} -0.5 V; LOW to high-impedance tests are made with S₁ closed to the V_{OL} +0.5 V level.

SWITCHING WAVEFORMS KEY TO SWITCHING WAVEFORMS



