Am26LS38

Quad Differential Backplane Transceiver

Advanced Micro Devices

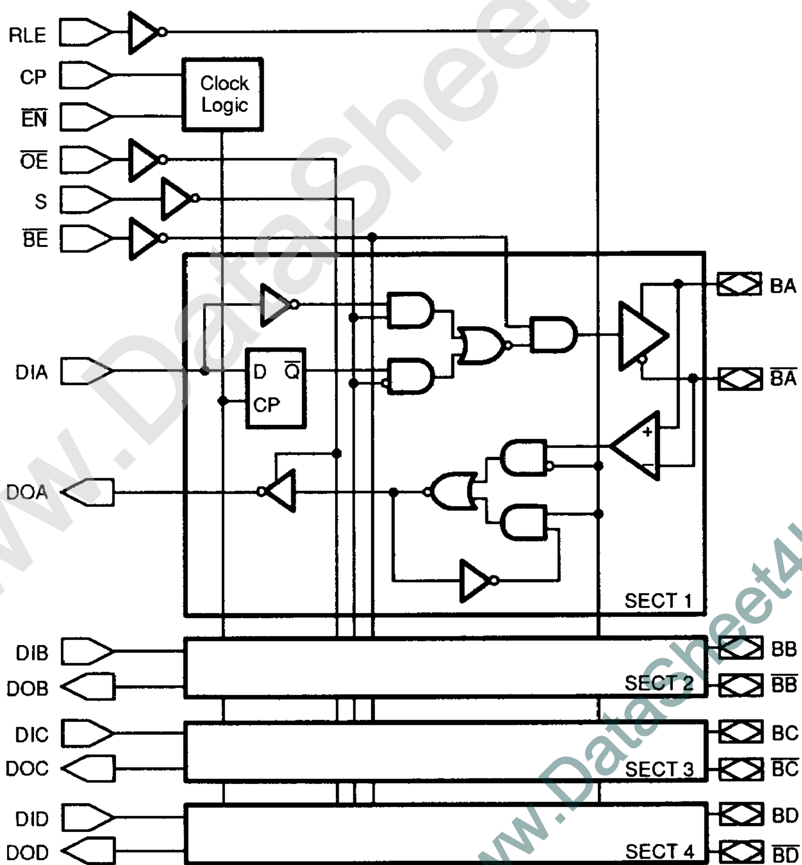
DISTINCTIVE CHARACTERISTICS

- 10 Mb data rate
- 0.45 V DC noise margin
- Biasing line terminations allow low voltage swing while maintaining high noise margin
- Pair delay 55 ns maximum
- Controlled driver skew to minimize noise
- Driver register and receiver latch with register bypass mode
- Driver output short-circuit protected to V_{CC} limits
- Outputs disabled during power-up and down
- Three-state receiver outputs maintain Hi-Z during power-up and down and over V_{CC} range

GENERAL DESCRIPTION

The Am26LS38 is a high performance backplane transceiver designed to integrate Schottky TTL performance, high noise immunity and wired logic capability into a low cost differential backplane structure. The resulting backplane can have up to 24 receiver unit loads in a party-line, wired-OR logic configuration, with a guaranteed fail-safe state, and operates from a single 5 V power supply.

BLOCK DIAGRAM



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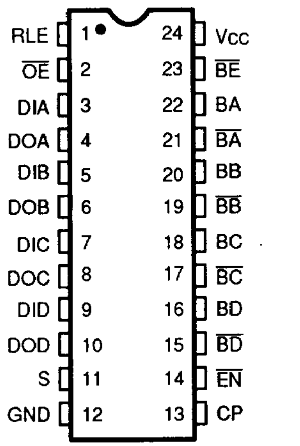
Publication# 02163 Rev. C Amendment/0
Issue Date: May 1991

CONNECTION DIAGRAM
Top View

DIP



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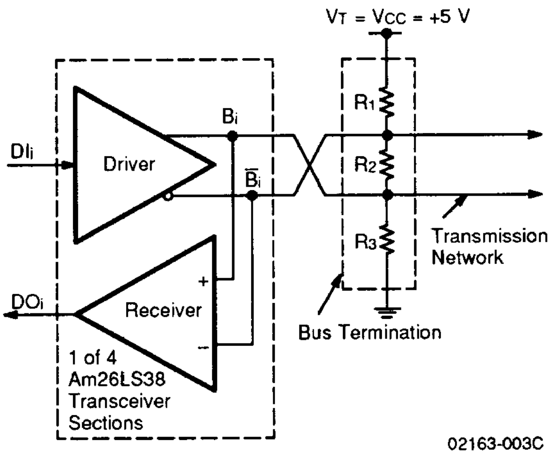
Note:
Pin 1 is marked for orientation.

SYSTEM CONFIGURATION DIAGRAM



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ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM26LS38 ___ **D** **C** **B**

OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

TEMPERATURE RANGE
C = Commercial (0 to +70°C)

PACKAGE TYPE
D = 24-Pin Ceramic DIP (CD3024)
S = 24-Pin Small Outline (SO 024)

SPEED OPTION
Not Applicable

DEVICE NUMBER/DESCRIPTION
Am26LS38
Quad Differential Backplane Transceiver

Valid Combinations	
AM26LS38	DC, DCB, SC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
22, 20 18, 16, 21, 19, 17, 15	BA, BB, BC, BD (B_i), $\overline{BA}$, $\overline{BB}$, $\overline{BC}$, $\overline{BD}$ ($\overline{B}_i$)	I/O	Paired open emitter (B_i)/ open collector ($\overline{B}_i$) driver outputs and receiver inputs. The driver outputs are either simultaneously active or simultaneously inactive. In the inactive state (DI_i = LOW) both drivers (B_i and $\overline{B}_i$) are turned off and the voltage differential representing the OFF state is determined by the line terminating resistor networks. In the active state (DI_i = HIGH), both drivers are driven on and act to reverse the voltage differential across the line to produce the ON state. The open-emitter/open-collector outputs are always connected in a wried-OR (or wired-AND) configuration. A driver is disabled by making its outputs inactive.
23	$\overline{BE}$	I	Bus Enable operates to enable or disable all output drivers by making them inactive when $\overline{BE}$ = HIGH and controlled by data input when $\overline{BE}$ = LOW.
13	CP	I	Clock Pulse input to the driver register enters data on the LOW-to-HIGH transition.
3, 5, 7, 9	DIA, DIB, DIC, DID (DI_i)	I	Data inputs each driver's buffer or register. A HIGH input to DI_i will result in an active (ON) output. A LOW input will cause an inactive (OFF) output.
4, 6, 8, 10	DOA, DOB, DOC, DOD (DO_i)	O	Receiver data latch outputs. An inactive bus (OFF state) will produce a LOW DO_i output and an active bus (ON state) will produce a HIGH DO_i output.
14	$\overline{EN}$	I	Clock Enable for the driver registers. $\overline{EN}$ = LOW enables DI_i data to be clocked into the respective register. $\overline{EN}$ = HIGH acts to hold previous data in each register regardless of the state of CP.
2	$\overline{OE}$	I	Output Enable for the receiver latch output buffer. When $\overline{OE}$ is LOW the outputs are enabled. When $\overline{OE}$ is HIGH all receiver outputs are in the high impedance state.
1	RLE	I	Receiver Latch Enable for the receiver latches. When RLE is HIGH the latches are transparent. When RLE is LOW received data meeting the setup and hold requirements relative to the HIGH-to-LOW transition of RLE will be stored.
11	S	I	Select input control for the drivers. When S is HIGH driver data from the registers will be selected (Register Mode). When S is LOW (Buffer Mode) the drivers respond to the DI_i inputs directly, bypassing the driver registers.

Inputs									Outputs			
RLE	CP	$\overline{EN}$	$\overline{OE}$	S	$\overline{BE}$	DI_i	B_i	$\overline{B}_i$	B_i	$\overline{B}_i$	DO_i	Function
H	X	X	L	L	L	L	NA	NA	L	H	L	Driver buffer mode (loop test)
H	X	X	L	L	L	H	NA	NA	H	L	H	
H	↑	L	L	H	L	L	NA	NA	L	H	L	Driver register mode
H	↑	L	L	H	L	H	NA	NA	H	L	H	
H	X	X	L	X	H	X	L	H	NA	NA	L	Receiver latch mode
H	X	X	L	X	H	X	H	L	NA	NA	H	
L	X	X	L	X	H	X	X	X	X	X	DO_{in-1}	Receiver in circulation
X	X	X	H	X	H	X	X	X	X	X	Z	Receiver output in high impedance state

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition of clock
DO_{in-1} = Previous state of DO_i
Z = High impedance
X = Don't care
NA = Not applicable

FUNCTIONAL DESCRIPTION

The Am26LS38 represents a new approach in backplane transceiver design. Its unipolar differential signaling scheme minimizes problems associated with crosstalk and the loss of noise immunity due to common mode voltage while providing high speed, party line and wired logic capabilities.

A good ground system and shielding are the best methods for limiting noise on the backplane. Ground planes can significantly reduce inductive ground voltage ringing. Where multilayer PC backplane are not a reasonable choice, a differential bus can be created using the Am26LS38 and twisted pair or any balanced transmission medium.

A backplane designed with an Am26LS38 has 3 main elements; 1) a driver section, 2) a receiver section, 3) and a controlled impedance differential line with a prebiasing line termination. The scheme for driver, receiver, and termination resistors is shown in Figure A.

System Operation

The system has two operational states.

1. Active – driver outputs on
2. Passive – driver outputs off

This 2-state (active/passive) operation makes passive or wired logic functions possible. In the passive state, the lines assume a known polarity and voltage (pre-biased bus). The passive bus state may be assigned either the false (wired-OR) or true (wired-AND) sense, potentially reducing the number of backplane signal lines.

The 2-state driver employs active pull-down (open collector) and active pull-up (open emitter) output stages (Figure A). When a driver is active, both output stages turn on. This impresses a 0.5 V minimum voltage differential on the bus, reversing the voltage across R_2. In the passive mode both output stages are off. The voltage levels and polarities return to the conditions set by the pre-biasing resistive network. In either state the voltage across the differential lines are symmetrical about $V_{CC}/2$. The system achieves high speeds because the voltage levels required to change state are very close together.

The receiver is designed with a ±50 mV threshold voltage. This low threshold level combined with a driver output greater than 500 mV provides a high degree of tolerance to attenuation and reflection effects in the cable. Receiver hysteresis provides differential noise immunity. Without hysteresis, a small amount of noise around the switching threshold could cause errors.

Propagation delay skew ($t_{PHL} - t_{PLH}$) is controlled. The system allows up to 1.5 V of common mode voltage.

Terminating the Transmission Line or Bus

Common mode reflections in the line can be reduced significantly by symmetrically terminating the bus. This increases the tolerance to common mode noise. Centering the network at $V_{CC}/2$ ($R_1 = R_3$) further improves the performance by causing all induced noise and reflections to appear as a common mode signal (Figure B).

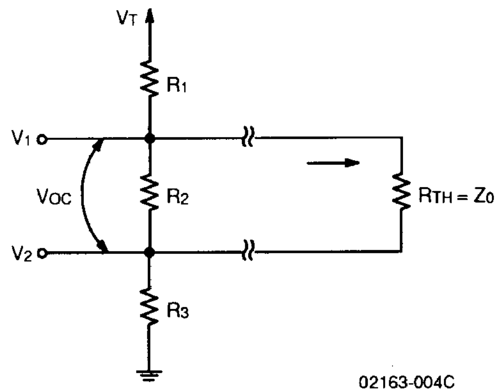


Figure B. Termination Circuit

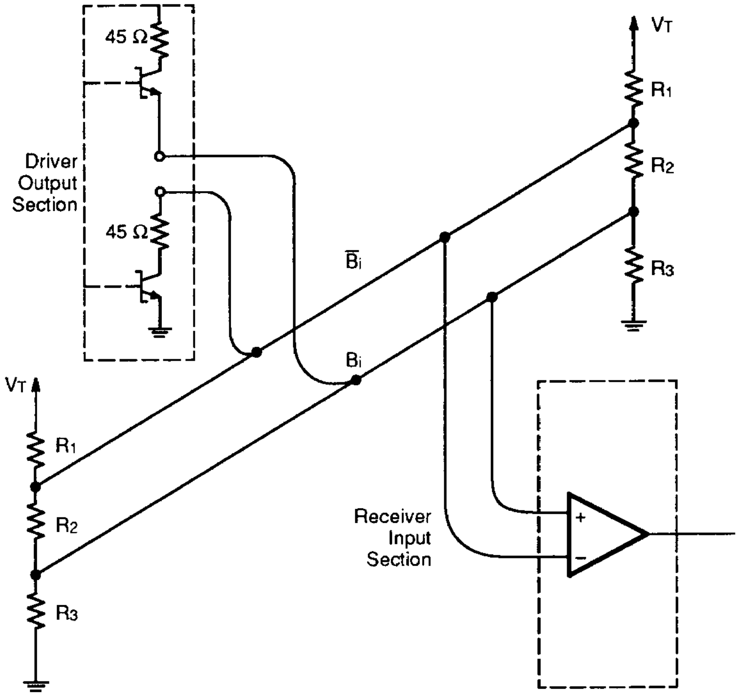


Figure A. The Scheme for Driver, Receiver, and Termination Resistors

A first order approximation of resistor values may be developed by letting the ratio of R_1 to R_2 be 2:1, and the Thevenin equivalent resistance of the termination equal the characteristic impedance of the line (Z_0).

Then:

(1) $V_{OC} = V_T \dfrac{R_2}{R_2 + 2R_1}$

(2) $R_{TH} = \dfrac{2R_1R_2}{2R_1 + R_2}$

From equation (1) and (2),

(3) $R_1 = \dfrac{V_T R_{TH}}{2V_{OC}}$

(4) $R_2 = \dfrac{V_T R_{TH}}{V_T - V_{OC}}$

If $V_T = 5$ V, $V_{OC} = 1.0$ V, and $R_{TH} = 90\Omega = Z_0$, we can derive that R_1 ~220Ω, R_2 ~110Ω.

Second order adjustments require attention to unit loading factors (receiver differential input resistance is in parallel with R_2), transmission rates and a host of other factors.

Data Path

Figure C shows the data path from one driver to another receiver for one bit of the bus interface.

The transmit register or buffer and receiver latch are configured to provide two modes of operation. The register and latch can provide local storage for output and input data. In the non-storage mode the buffer input to the driver can be selected and the receiver can be wired transparent. Incorporating storage on-chip provides improved speed and lower package count without significant penalty in the non-storage mode.

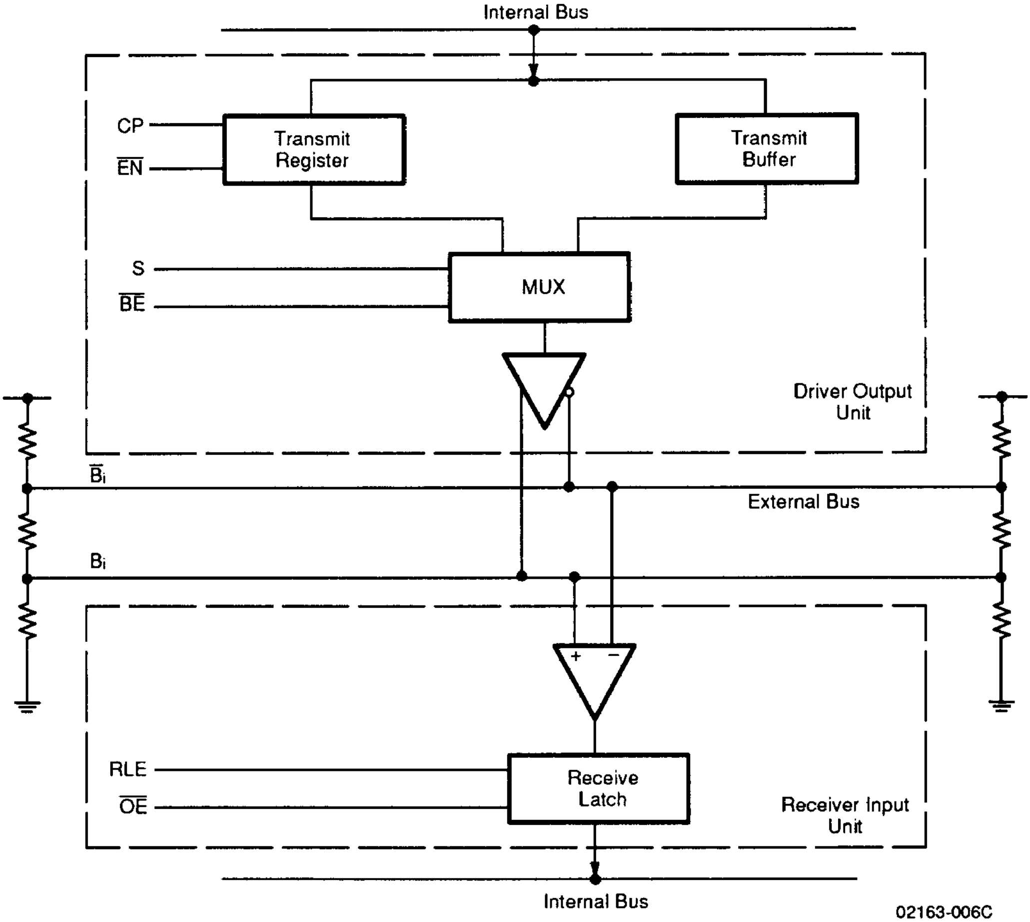
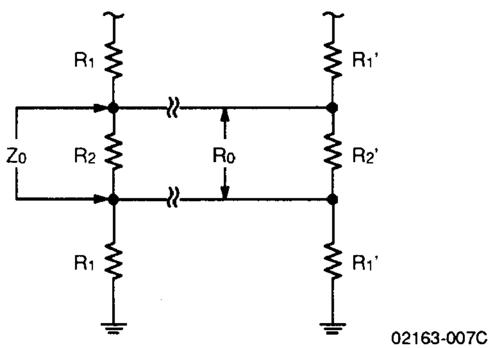


Figure C. The Data Path for One Bit of the Bus Interface



Equivalent Circuit Recommended Termination

Termination Resistors and Equivalent Impedance

Z_O	$R_1 = R_1'$	$R_2 = R_2'$
90Ω	220Ω	110Ω
120Ω	300Ω	150Ω

Minimum line V_O (differential voltage) = 0.5 V

Equivalent Termination Versus DC Resistance

Z_O	R_O
88.0Ω	44.0Ω
120.0Ω	60.0Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0 V
Common Mode Range	0 to Vcc
Differential Mode Range (REC)	0 to Vcc
Logic Inputs	5.5 V
Storage Temperature Range	−65 to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature	0 to +70°C
Supply Voltage	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
Bus Driver Output							
V_O	Output Differential Voltage (Driver Active) $V_{Bi} - \overline{V}_{Bi}$	$\overline{BE}$ = LOW DI_i = HIGH Test Circuit #1		0.5			V
I_{SS}	Output Current	DI_i = HIGH Test Circuit #2 $\overline{BE}$ = LOW	Ia	−22.5	−55	−115	mA
			Ib	+22.5	+55	+115	mA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.5 V		−75	−150	−250	mA
Bus Receiver Input							
V_{TH}	Differential Input Threshold Voltage	V_{CM} = 0 to V_{CC} V_{OUT} = V_{OL} or V_{OH}		−50	±10	+50	mV
R_{IN}	Input Resistance to GND	0 ≤ V_{CC} ≤ V_{CC} Max.		4	5.7		kΩ
R_{IN}	Differential Input Resistance	0 ≤ V_{CC} ≤ V_{CC} Max.		8	11.4		kΩ
V_{OS}	Center Voltage	Test Circuit #3 Active and Passive		2.0	$V_{CC}/2$	3.0	V
$\lvert V_{OS}\rvert - \lvert \overline{V_{OS}}\rvert$	Center Voltage Difference (Active vs Passive)	Test Circuit #3			90	300	mV
Non-Bus Input and Outputs							
V_{OH}	Output HIGH Voltage	ΔV_{IN} = +0.1 V	I_{OH} = −15 mA	2.4	3.4		V
			I_{OH} = −24 mA	2.0	3.3		V
V_{OL}	Output LOW Voltage	ΔV_{IN} = −0.1 V	MIL, I_{OL} = 32 mA			0.5	V
			COM'L, I_{OL} = 48 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	V
I_{IL}	Input LOW Current	V_{IN} = 0.4 V	Data		−275	−400	μA
			Control		−0.65	−1.0	mA
			Clock		−0.65	−1.0	mA
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			0.1	+50	μA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.5 V		−75	−150	−250	mA
I_I	Input Leakage Current	V_{IN} = 5.5 V				1	mA
V_{IC}	Input Clamp Voltage	I_{IN} = −18 mA			−0.75	−1.2	V
I_{OZ}	Leakage Current Passive	V_O = 2.4 V				+50	μA
		V_O = 0.4 V				−50	μA
I_{CC}	Power Supply Current	$\overline{BE}$, $\overline{OE}$ = HIGH				145	mA

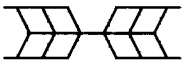
SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V)

Parameter Symbol	Parameter Description		Test Conditions		Min.	Typ.	Max.	Unit
t_{DBA}	DIi to Bi/B̅i Propagation Delay	Active	B̅E̅ = LOW	Test Circuit #1		7	10	ns
t_{DBP}		Passive	S = LOW			7	10	
t_{CBA}	CP to Bi/B̅i Propagation Delay	Active	B̅E̅ = LOW	Test Circuit #1		10.5	16	ns
t_{CBP}		Passive	S = HIGH			13	16	
t_{PA}	B̅E̅ to Bi/B̅i Propagation Delay	Active	DIi = HIGH	Test Circuit #1		8.5	12	ns
t_{PP}		Passive	S = LOW			4	8	
t_S	DIi to Clock Setup Time		B̅E̅ = LOW		5	2.5		ns
t_H	DIi to Clock Hold Time				2	0		
t_S	E̅N̅ to Clock Setup Time				8	4		
t_H	E̅N̅ to Clock Hold Time				0	–4		
t_S	Bi/B̅i to RLE Setup Time				5	2.5		
t_H	Bi/B̅i to RLE Hold Time				2	0.7		
t_{PLZ}/t_{PHZ}	O̅E̅ to DOi Disable Time		C_L = 50 pF	Test Circuit #4			20	ns
t_{PLZ}/t_{PHZ}			C_L = 5 pF	Test Circuit #4			13	
t_{PZL}	O̅E̅ to DOi Disable Time		Test Circuit #4				17	ns
t_{PZH}							17	
t_{PLH}	RLE to DOi		O̅E̅ = LOW	Test Circuit #4		11	13	ns
t_{PHL}						14	17	
t_{PRX}	Bi/B̅i to DOi		RLE = HIGH O̅E̅ = LOW	Test Circuit #4		12	17	ns
t_{PLH} t_{PHL}	B̅E̅ to DOi Propagation Delay		RLE = HIGH O̅E̅ = LOW	Test Circuits #1, #4		15	25	ns
t_{PLH} t_{PHL}	DIi to DOi (Buffer Mode)		S = LOW RLE = HIGH O̅E̅ = LOW	Test Circuits #1, #4		18	25	ns
t_{PLH} t_{PHL}	CP to DOi (Register Mode)		S = HIGH RLE = HIGH O̅E̅ = LOW	Test Circuits #1, #4		22	28	ns
t_{PWL}	Clock Pulse Width	LOW			10	3		ns
t_{PWH}		HIGH			10	5		
t_{PWH}	RLE Pulse Width	HIGH			10	6		ns
t_{SKEW}	Propagation Delay Skew (t_{PLH} – t_{PHL})		V_{CC} = 5 V C_L = 50 pF Measurement $V_{CC}/2$	Test Circuit #1		±1	±5	ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions		T_A = 0 to +70°C, V_{CC} = 5.0 V ±10% Min.	Max.	Unit
t_{DBA}	DI_i to $B_i/\overline{B}_i$ Propagation Delay	Active	$\overline{BE}$ = LOW	Test Circuit #1		12	ns
t_{DBP}		Passive	S = LOW			12	
t_{CBA}	CP to $B_i/\overline{B}_i$ Propagation Delay	Active	$\overline{BE}$ = LOW	Test Circuit #1		20	ns
t_{CBP}		Passive	S = HIGH			20	
t_{PA}	$\overline{BE}$ to $B_i/\overline{B}_i$ Propagation Delay	Active	DI_i = HIGH	Test Circuit #1		17	ns
t_{PP}		Passive	S = LOW			12	
t_S	DI_i to Clock Setup Time		$\overline{BE}$ = LOW		7		ns
t_H	DI_i to Clock Hold Time				3		
t_S	$\overline{EN}$ to Clock Setup Time				10		
t_H	$\overline{EN}$ to Clock Hold Time				0		
t_S	$B_i/\overline{B}_i$ to RLE Setup Time				7		
t_H	$B_i/\overline{B}_i$ to RLE Hold Time				3		
t_{PLZ}/t_{PHZ}	$\overline{OE}$ to DO_i Disable Time		C_L = 50 pF	Test Circuit #4		17	ns
t_{PLZ}/t_{PHZ}			C_L = 5 pF	Test Circuit #4		10	
t_{PZL}	$\overline{OE}$ to DO_i Enable Time		Test Circuit #4			15	ns
t_{PZH}						15	
t_{PLH}	RLE to DO_i		$\overline{OE}$ = LOW	Test Circuit #4		15	ns
t_{PHL}						20	
t_{PRX}	$B_i/\overline{B}_i$ to DO_i		RLE = HIGH, $\overline{OE}$ = LOW	Test Circuit #4		21	ns
t_{PLH} / t_{PHL}	$\overline{BE}$ to DO_i Propagation Delay		RLE = HIGH, $\overline{OE}$ = LOW	Test Circuits #1, #4		32	ns
t_{PLH} / t_{PHL}	DI_i to DO_i (Buffer Mode)		S = LOW, RLE = HIGH, $\overline{OE}$ = LOW	Test Circuits #1, #4		30	ns
t_{PLH} / t_{PHL}	CP to DO_i (Register Mode)		S = HIGH, RLE = HIGH, $\overline{OE}$ = LOW	Test Circuits #1, #4		35	ns
t_{PWL}	Clock Pulse Width	LOW			10		ns
t_{PWH}		HIGH			10		
t_{PWH}	RLE Pulse Width	HIGH			13		ns
t_{SKEW}	Propagation Delay Skew ($t_{PLH} - t_{PHL}$)		V_{CC} = 5 V, C_L = 50 pF, Measurement $V_{CC}/2$	Test Circuit #1		±7	ns

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

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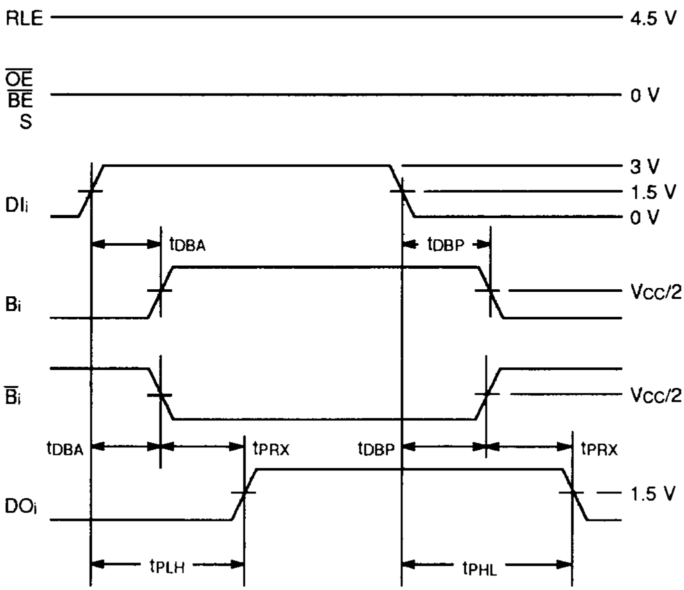

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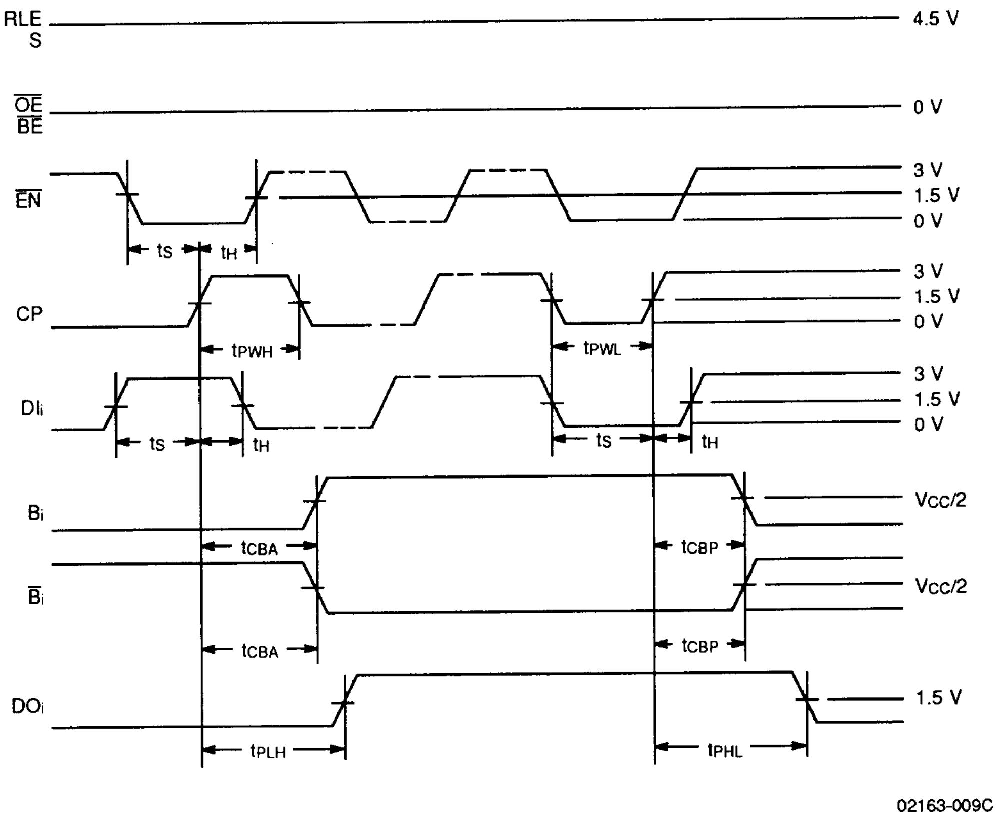
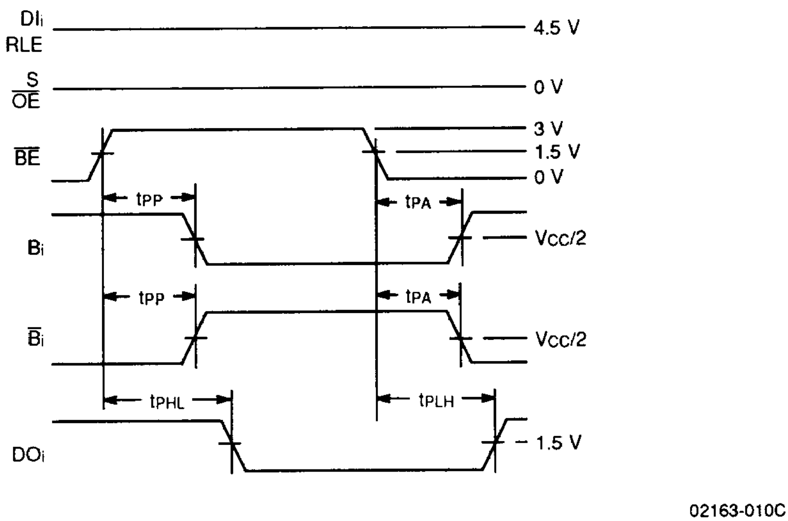
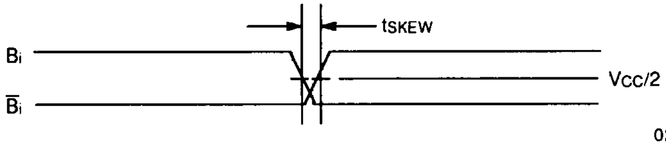
DIi to Bi,$\overline{B}$i, DOi (Buffer Mode)



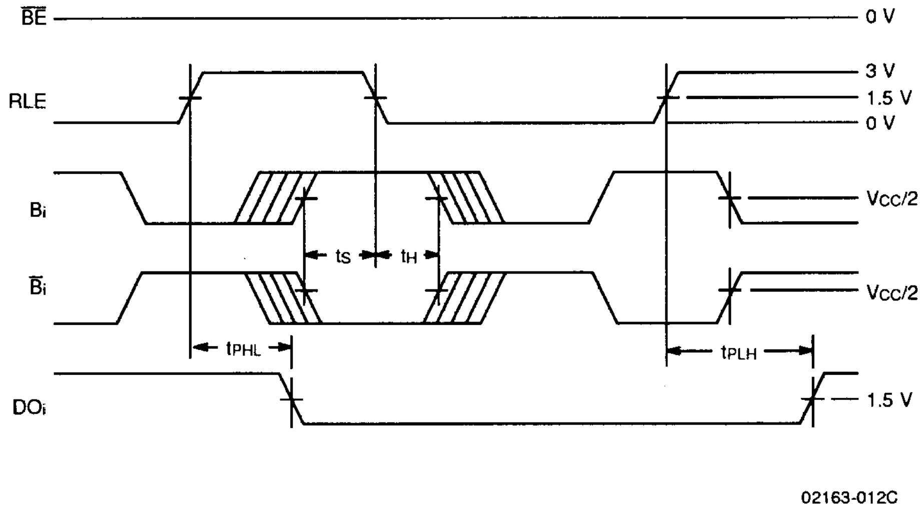
CP to Bi, B̄i, DOi (Register Mode)



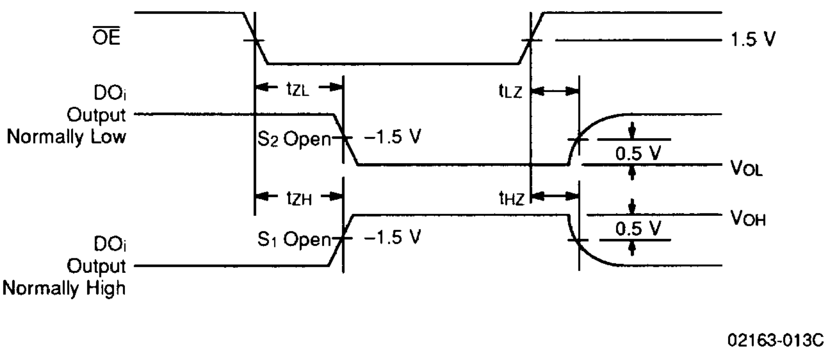
B̄Ē to Bi, B̄i, DOi (Passive and Active)



Output to Output

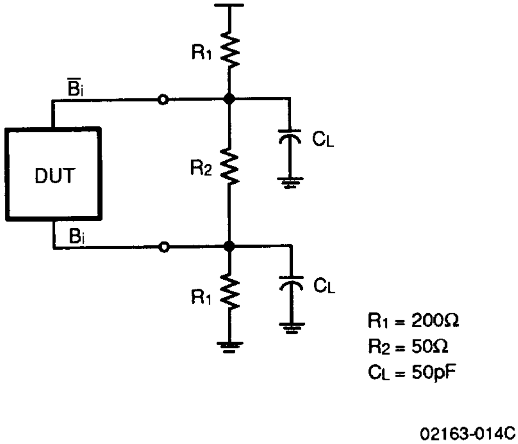


RLE to DOi

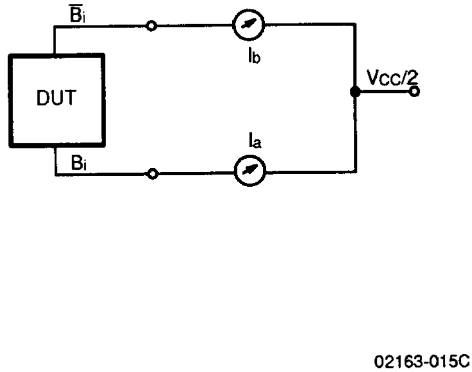


$\overline{OE}$ to DOi

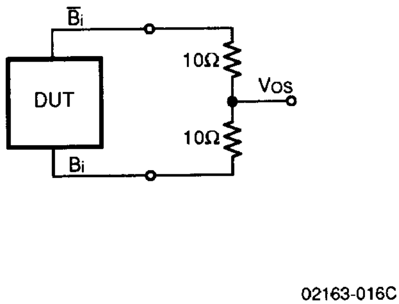
SWITCHING TEST CIRCUITS



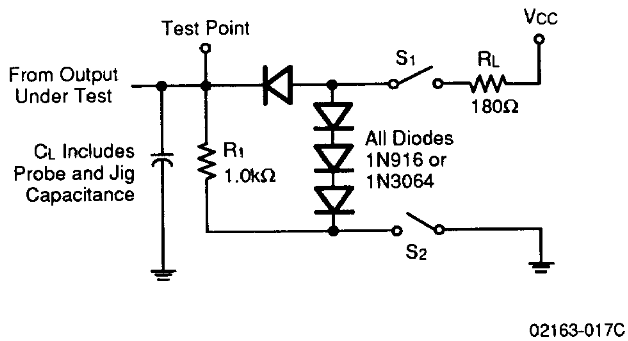
Test Circuit #1



Test Circuit #2



Test Circuit #3



Test Circuit #4

Notes:

1. C_L = 50 pF unless otherwise specified.
2. S_1 and S_2 are closed except where shown.