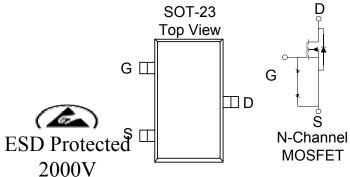
N-Channel 60V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY				
V _{DS} (V)	$r_{\mathrm{DS}(\mathrm{on})}\left(\Omega\right)$	$I_{D}(A)$		
60	$0.092 @ V_{GS} = 10 V$	3.1		
	$0.107 @ V_{GS} = 4.5V$	2.9		

- $\begin{array}{ll} \bullet & \quad \text{Low } r_{DS(on)} \text{ provides higher efficiency and} \\ \text{extends battery life} \end{array}$
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter			Maximum	Units
Drain-Source Voltage			60	V
Gate-Source Voltage			±20	V
Continuous Drain Current ^a	$T_A=25^{\circ}C$	1	2.8	
Continuous Drain Current	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	ъ	1.8	A
Pulsed Drain Current ^b			±15	
Continuous Source Current (Diode Conduction) ^a			1.7	A
D Diin-4i-u ^a	$T_A=25^{\circ}C$	D.,	1.3	W
Power Dissipation ^a	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	1 ()	0.8	• • •
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Maximum	Units	
M · I	t <= 5 sec	R _{THJA}	100	°C/W
Maximum Junction-to-Ambient ^a	Steady-State		166	

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Danamakasi	Chandral .	T (C P)	Limits			TT •4	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	VGS(th)	$V_{DS} = V_{GS}$, $I_D = 250 \text{ uA}$	1.0			V	
Cate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			±10	uA	
Zana Cata Valta an Drain Grunout	Ipss	$V_{DS}=48 V$, $V_{GS}=0 V$			1	,,,	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 48 \text{ V}, V_{CS} = 0 \text{ V}, T_J = 55^{\circ}\text{C}$			50	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			A	
Drain-Source On-Resistance ^A	*******	$V_{GS} = 10 \text{ V, ID} = 3.1 \text{ A}$			92	mΩ	
Drain-Source On-Resistance	fDS(on)	$V_{GS} = 4.5 \text{ V}, I_D = 2.9 \text{ A}$			107		
Forward Tranconductance ^A	gs	$V_{DS} = 4.5 \text{ V}, I_D = 3.1 \text{ A}$		8		S	
Diode Forward Voltage	V _{SD}	$I_S = 1.7 A, V_{GS} = 0 V$		1.10		V	
Dynamic ^b							
Total Gate Charge	Q	$V_{DS} = 30 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 3.1 \text{ A}$		3.6			
Gate-Source Charge	Qgs			1.8		пC	
Gate-Drain Charge	Qgd			1.3			
Turn-On Delay Time	td(on)			10			
Rise Time	tr	$V_{DD} = 30 \text{ V}, R_L = 30 \Omega, I_D = 1 \text{ A},$		10			
Tum-Off Delay Time	td(off)	$V_{GEN} = 10 V$		20		ns	
Fall-Time	tr			10			

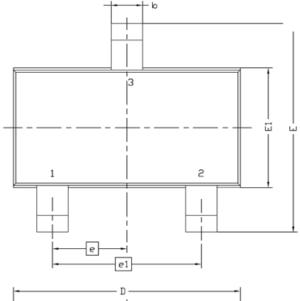
Notes

- a. Pulse test: $PW \le 300us duty cycle \le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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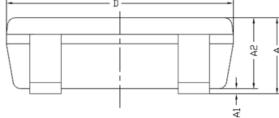
Analog Power SOT-23

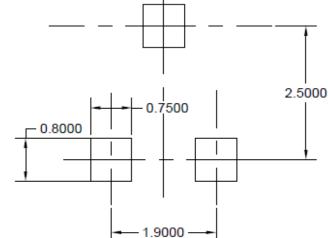
Package Information

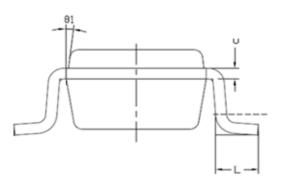


Symbol	MILLIMETERS		
Symbol	MIN	MAX	
Α	0.8	1.2	
A1	0	0.1	
A2	0.7	1.1	
b	0.3	0.5	
С	0.1	0.2	
D	2.7	3.1	
Е	2.6	3	
E1	1.4	1.8	
е	0.95 BSC		
e1	1.9 BSC		
L	0.3	0.6	
θ1	7° NOM		

Recommended Pad Layout







Note: Drain opening is recommended to be solder mask defined in a copper fill for improved thermal performance

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