

P - Channel 40V (D-S) MOSFET

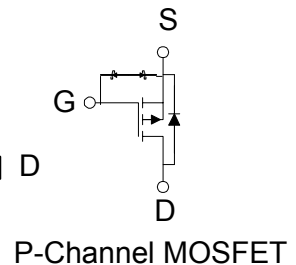
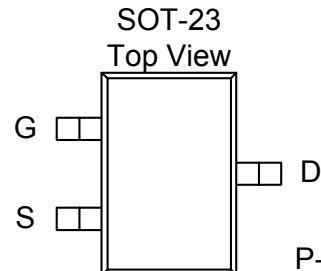
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology



ESD Protected
2000V

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-40	0.164 @ $V_{GS} = -10$ V	-3.2
	0.260 @ $V_{GS} = -4.5$ V	-2.6



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Ratings	Units
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	± 3.2	A
	$T_A = 70^\circ\text{C}$		± 2.7	
Pulsed Drain Current ^b		I_{DM}	± 10	
Continuous Source Current (Diode Conduction) ^a		I_S	0.4	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.25	W
	$T_A = 70^\circ\text{C}$		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{THJA}	100	$^\circ\text{C/W}$
	Steady-State		150	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

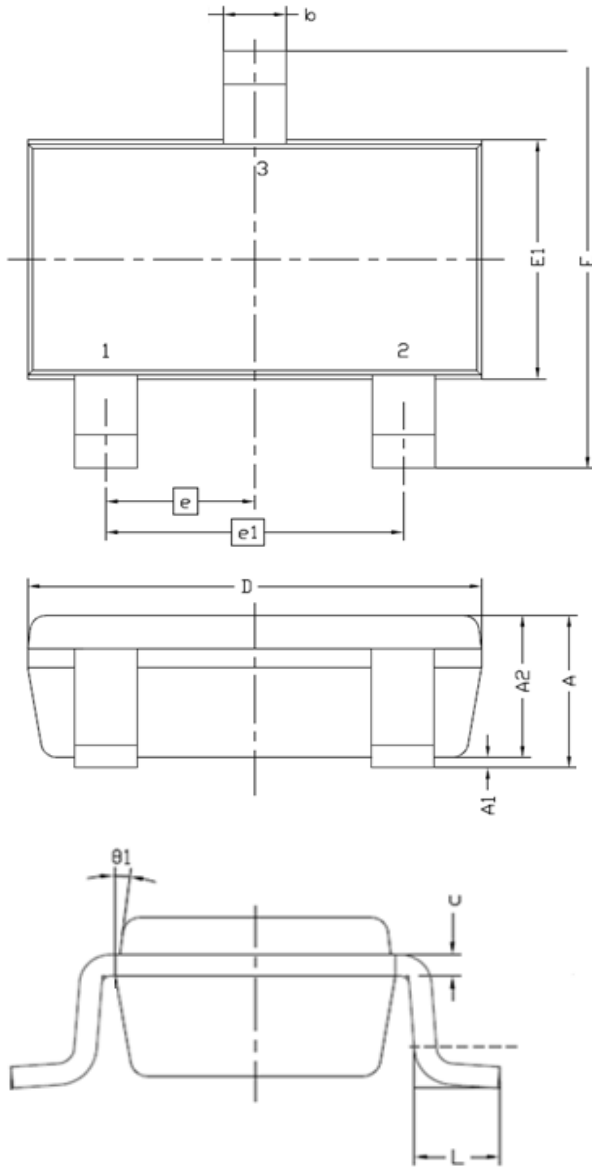
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Switch Off Characteristics						
Zero Gate Voltage Drain Current	IDSS	VDS = -32 V, VGS = 0 V			-1	μA
		VDS = -32 V, VGS = 0 V, TJ = 55°C			-10	
Gate-Body Leakage	IGSS	VDS = 0 V, VGS = ±20 V			±100	nA
Gate-Threshold Voltage	VGS(th)	VDS = VGS, ID = -250 uA	-1.0			V
On-State Drain Current ^A	ID(on)	VDS = -5 V, VGS = -4.5 V	-2			A
Drain-Source On-Resistance ^A	rDS(on)	VGS = -10 V, ID = -3.2 A			164	nΩ
		VGS = -4.5 V, ID = -2.6 A			260	
Forward Tranconductance ^A	gfs	VDS = -5 V, ID = -3.6 A		2		S
Diode Forward Voltage	VSD	IS = -0.4 A, VGS = 0 V		-0.70		V
Dynamic ^b						
Total Gate Charge	Qg	VDS = -10 V, VGS = -5 V, ID = -3.6 A		15		nC
Gate-Source Charge	Qgs			2.0		
Gate-Drain Charge	Qgd			2.0		
Turn-On Delay Time	td(on)	VDS = -15 V, ID = -1 A, RG = 50 Ω, VGEN = -10 V		10		ns
Rise Time	tr			2.8		
Turn-Off Delay Time	td(off)			53.6		
Fall Time	tf			46		

Notes

- Pulse test: $PW \leq 300\text{ }\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

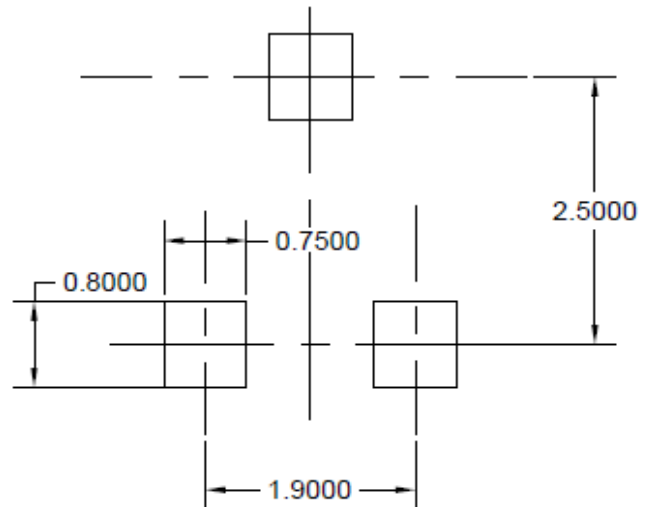
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Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.2
A1	0	0.1
A2	0.7	1.1
b	0.3	0.5
c	0.1	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.95 BSC	
e1	1.9 BSC	
L	0.3	0.6
θ1	7° NOM	

Recommended Pad Layout



Note: Drain opening is recommended to be solder mask defined in a copper fill for improved thermal performance

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