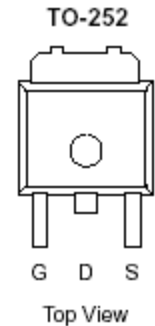
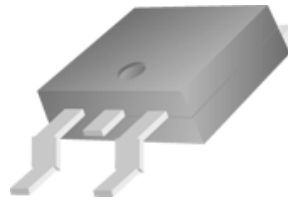


P-Channel 60-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-60	135 @ $V_{GS} = -10V$	16
	190 @ $V_{GS} = -4.5V$	14

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	16	A
Pulsed Drain Current ^b		I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a		I_S	-15	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

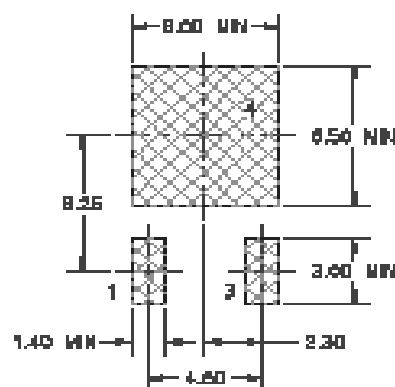
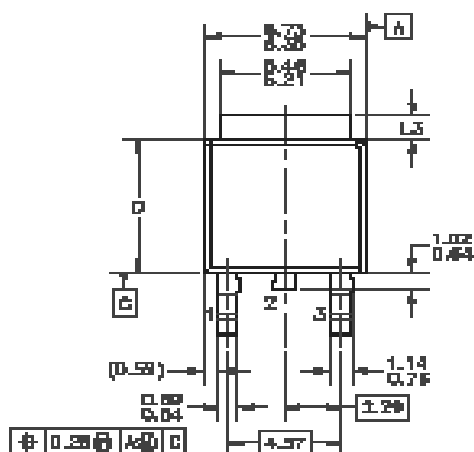
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-1			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -48\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55^\circ\text{C}$			-10	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = -5\text{ V}$, $V_{GS} = -10\text{ V}$	-20			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = -28\text{ A}$			135	m Ω
		$V_{GS} = -4.5\text{ V}$, $I_D = -14\text{ A}$			190	
Forward Transconductance ^A	g_{fs}	$V_{DS} = -15\text{ V}$, $I_D = -28\text{ A}$		8		S
Diode Forward Voltage	V_{SD}	$I_S = -2.5\text{ A}$, $V_{GS} = 0\text{ V}$			-1.2	V
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = -30\text{ V}$, $V_{GS} = -4.5\text{ V}$, $I_D = -28\text{ A}$		18		nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30\text{ V}$, $R_L = 30\text{ }\Omega$, $I_D = -1\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_G = 6\text{ }\Omega$		8		nS
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			35		
Fall Time	t_f			12		

Notes

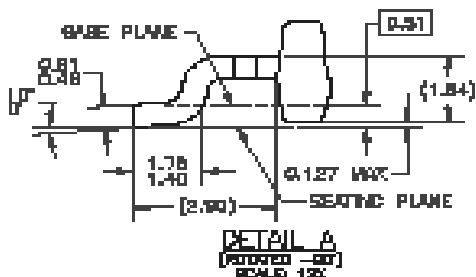
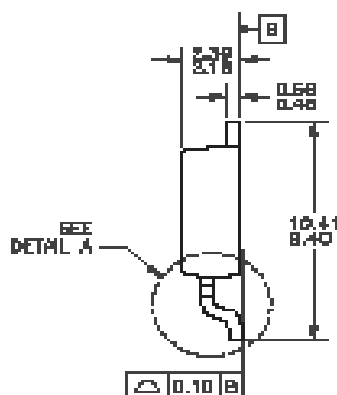
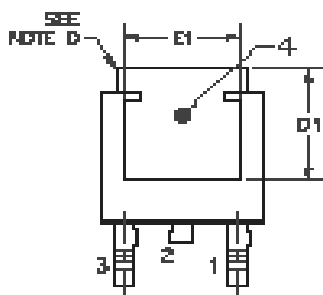
- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- ALL DIMENSIONS ARE IN MILLIMETERS.
 - THIS PACKAGE CONFORMS TO JEDEC, TO-263, ISSUE C, VARIATION AA, 30 DE, DATED NOV. 1989.
 - DIMENSIONING AND TOLERANCING PER ASME Y14.04M-1994.
 - HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - DIMENSIONS L3, D, E1 AND F1 TABLE:

	OPTION A1	OPTION A2
L3	0.88-1.27	1.62-2.59
D	8.97-9.19	8.93-9.09
E1	4.32 MIN	3.81 MIN
F1	3.81 MIN	4.37 MIN