

# REALTEK

**ALC5611**

## **AC'97 AUDIO CODEC + TOUCH PANEL CONTROLLER**

### **DATASHEET**

**Rev. 1.3**

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## **USING THIS DOCUMENT**

This document is intended for the hardware and software engineer’s general information on the Realtek ALC5611 Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## **REVISION HISTORY**

| <b>Revision</b> | <b>Release Date</b> | <b>Summary</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.0             | 2007/08/15          | First release                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 1.1             | 2008/01/11          | Revised section 1 General Description, page 1.<br>Added note in Table 4, page 8.<br>Revised section 7.5.5.1 Speaker Output, page 16.<br>Revised section 7.6 Touch Panel Control, page 18.<br>Revised Table 29, page 32.<br>Revised Table 30, page 33.<br>Revised Table 33, page 36.<br>Added note in Table 81, page 56.<br>Revised section 10 Application Circuits, page 66.<br>Revised section 12 Ordering Information, page 69.                              |
| 1.2             | 2008/07/23          | Revised section 12 Ordering Information, page 69.                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1.3             | 2009/08/07          | Revised Figure 1 Block Diagram, page 4.<br>Revised Table 3 Filter/Reference, page 8.<br>Revised Table 4 Power/Ground, page 8.<br>Revised Table 83 Analog Performance Characteristics, page 57.<br>Added section 9.3.8 I <sup>2</sup> S/PCM Interface Master Mode, page 64.<br>Added section 9.3.9 I <sup>2</sup> S/PCM Interface Slave Mode, page 65.<br>Revised section 11 Mechanical Dimensions, page 67.<br>Revised Table 93 Ordering Information, page 69. |

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# 1. General Description

The ALC5611 is a highly-integrated AC'97 interface audio codec with multiple input/output ports and a 4-wire touch panel controller.

The ALC5611 is designed for mobile computing and communications.

Stereo audio is supported via the AC'97 interface. To reduce component count, the device can connect directly to:

- A 4-wire touch panel
- MONO or stereo differential analog inputs
- Stereo headphone
- Single-ended or BTL MONO output
- MONO or Stereo Bridge-Tied Load (BTL) speaker

Multiple analog input and output pins are provided for seamless integration with analog connected wireless communication devices. Differential input/output connections efficiently reduce noise interference, providing better sound quality. Class-AB or Class-D amplifiers are easily swapped via simple register configuration, and the 1.7 Watt speaker removes the need for an additional amplifier, further cutting both cost and required board area. Additionally, a flexible hardware 5-band equalizer with configurable gain, bandwidth, and center frequency, and enriches the sound experience.

ALC5611 Digital power operates at supply voltages from 1.8V to 3.6V. Analog power operates from 2.3V to 3.6V, and Speaker power operates from 2.3V to 5V. To extend battery life, each section of the device can be powered down individually under software control. Leakage current in maximum power saving state is less than 10 $\mu$ A.

The ALC5611 is available in a 7x7mm 'Green' QFN package, making it ideal for use in handheld portable systems.

## 2. Features

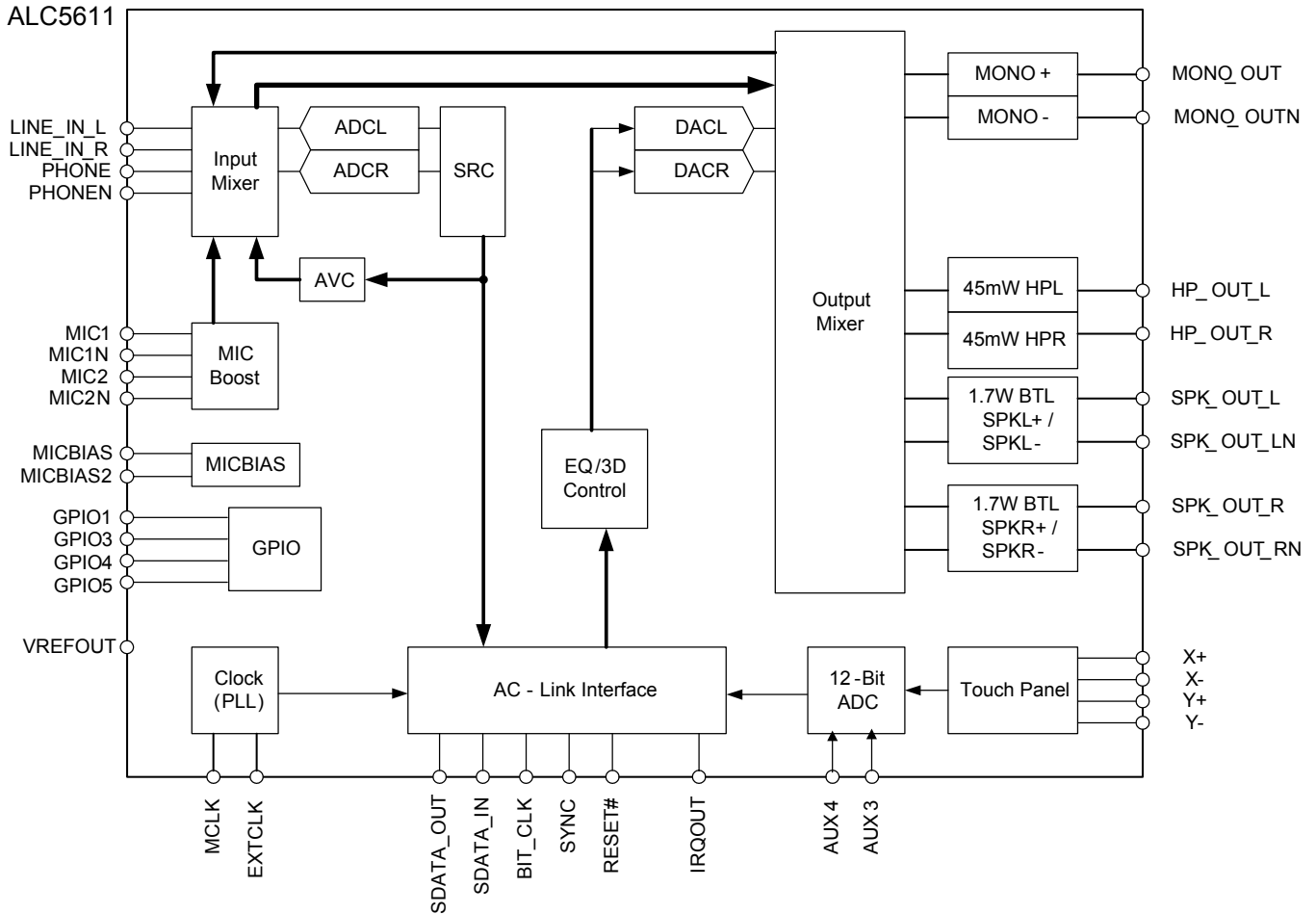
- Single-chip AC'97 Rev 2.2 compatible codec
  - ◆ 16-bit DAC SNR 90dB, THD+N -85dB
  - ◆ 16-bit ADC SNR 85dB, THD+N -80dB
  - ◆ Supports all WinCE variable rates (8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz)
- One analog stereo input (LINE-IN)
- One analog MONO single-ended or differential input (PHONE and PHONEN input)
- Stereo, single-ended MONO, or differential analog microphone inputs, with boost pre-amplifiers (+20/+30/+40dB)
- BTL (Bridge-Tied Load) Max. output with on-chip 1.7W speaker driver (SPKVDD=5V, 8Ω load, 10% THD+N)
- Stereo headphone output with on-chip 45mW headphone driver (HPVDD=3.3V, 16Ω load)
- 25mW SE or 75mW BTL MONO output support (AVDD=3.3V, 32Ω load)
- Microphone switch detection
- Power management and enhanced power saving
- Supports digital 5-band equalizer (EQ)
- Supports digital spatial sound and pseudo stereo effect
- Supports pop noise suppression
- Internal PLL can receive wide range of clock input (Digital IO power > 1.8V)
- Digital power supplies from 1.8V to 3.6V, speaker amplifier power supplies from 2.3V to 5V
- Analog power, headphone power, and touch panel power supplies from 2.3V to 3.6V
- Resistive touch panel interface
  - ◆ Supports 4-wire panel
  - ◆ X, Y axis and pressure measurement
  - ◆ 12-bit resolution AUX\_ADC for battery measurement, DNL<±1 LSB, INL<±2 LSBs
  - ◆ Supports pen-down detection in power down mode
- 48-pin QFN package

### **3. System Applications**

- Tablet PC system/Ultra-Mobile PC (UMPC)
- GPS/Personal Navigation Device (PND) or Multi-Media phone
- PDA Phone/Smartphone
- Personal Media Player (PMP)

## 4. Function Block Diagram

### 4.1. Function Block



**Figure 1. Block Diagram**

## 4.2. Audio Mixer Path

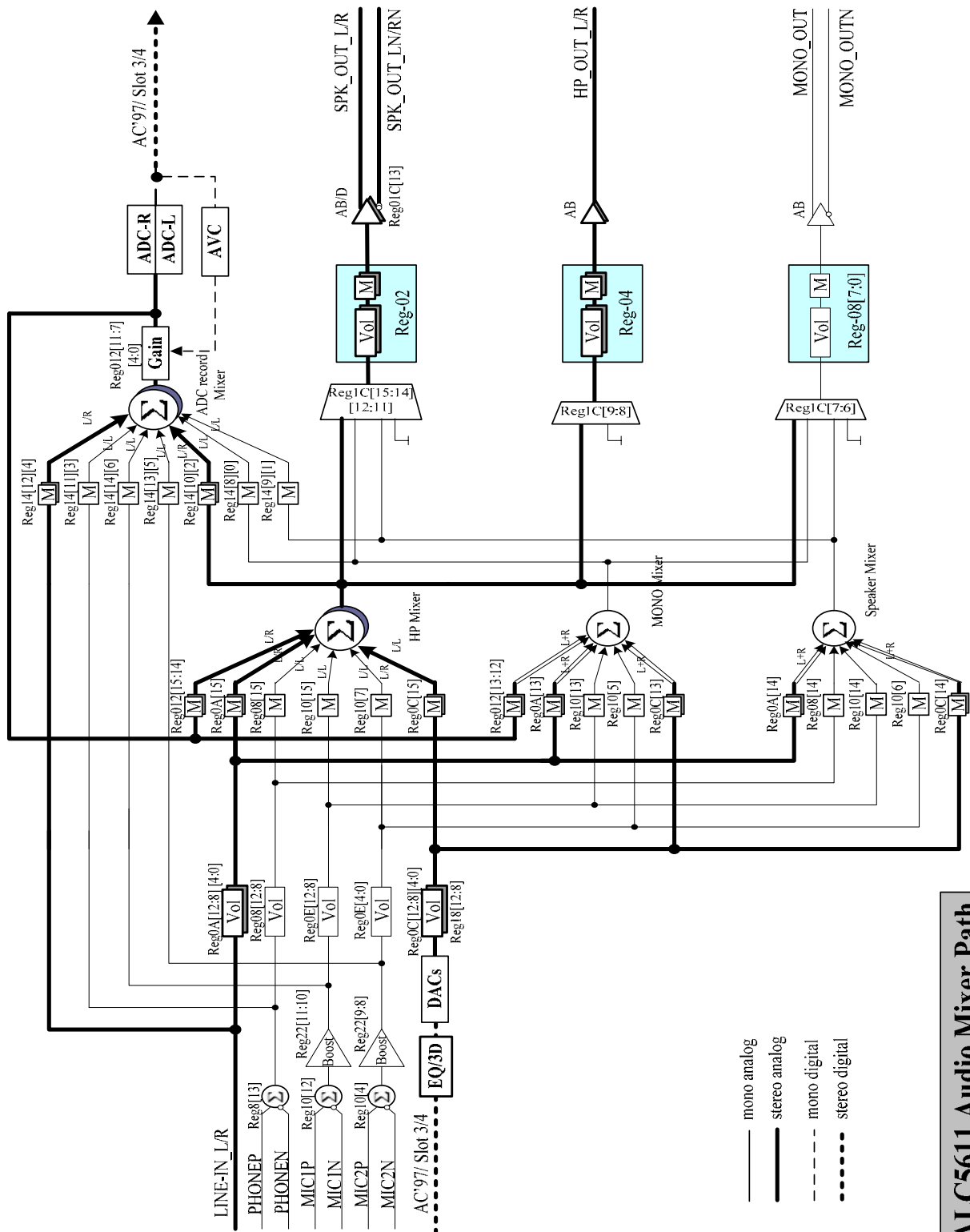


Figure 2. Audio Mixer Path

## 5. Pin Assignments

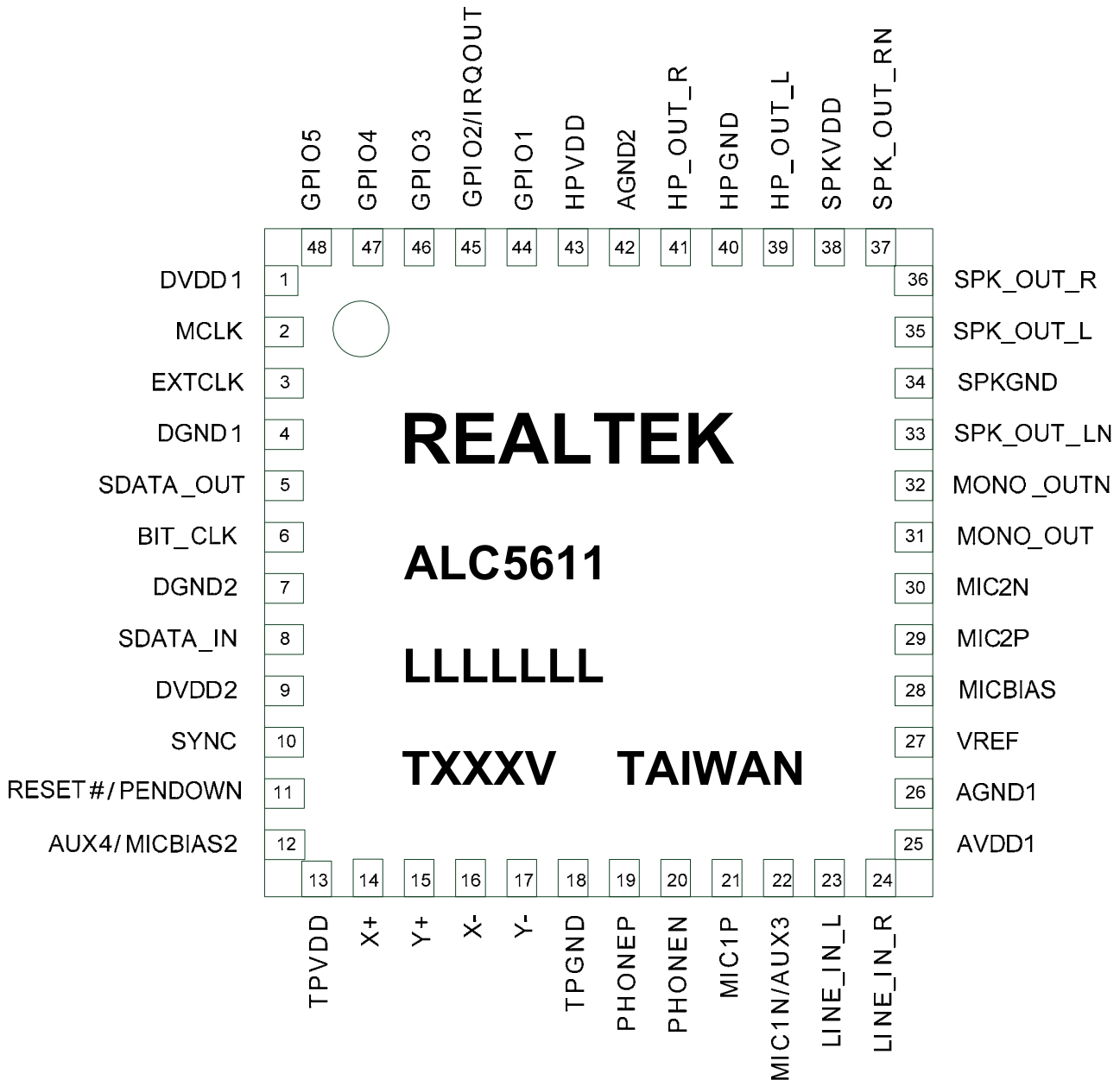


Figure 3. Pin Assignments

### 5.1. Package and Version Identification

‘Green’ package is indicated by a ‘G’ in the location marked ‘T’ in Figure 3.

## 6. Pin Descriptions

### 6.1. AC'97 Digital I/O Pins

**Table 1. AC'97 Digital I/O Pins**

| Name             | Type | Pin | Description                                             | Characteristic Definition                                               |
|------------------|------|-----|---------------------------------------------------------|-------------------------------------------------------------------------|
| MCLK             | I    | 2   | Master Clock Input                                      | Schmitt trigger                                                         |
| EXTCLK           | IO   | 3   | External Reference Clock Input/Output                   | Output: $V_{OL}=0.1*DVDD$ , $V_{OH}=0.9*DVDD$<br>Input: Schmitt trigger |
| SDATA_OUT        | I    | 5   | Serial TDM Data Input                                   | Schmitt trigger                                                         |
| BIT_CLK          | O    | 6   | Bit Clock Output                                        | $V_{OL}=0.1*DVDD$ , $V_{OH}=0.9*DVDD$                                   |
| SDATA_IN         | O    | 8   | Serial TDM Data Output                                  | $V_{OL}=0.1*DVDD$ , $V_{OH}=0.9*DVDD$                                   |
| SYNC             | I    | 10  | 48khz Synchronous Input Signal                          | Schmitt trigger                                                         |
| RESET#/PENDOWN   | I/O  | 11  | H/W Reset Input<br>Pen-down Output                      | Schmitt trigger                                                         |
| GPIO1            | IO   | 44  | General Purpose Input And Output 1                      | GPIO: Input/Output                                                      |
| GPIO2/<br>IRQOUT | IO   | 45  | General Purpose Input And Output 2/<br>Interrupt Output | GPIO: Input/Output<br>IRQOUT: Output                                    |
| GPIO3            | IO   | 46  | General Purpose Input And Output 3                      | GPIO: Input/Output                                                      |
| GPIO4            | IO   | 47  | General Purpose Input And Output 4                      | GPIO: Input/Output                                                      |
| GPIO5            | IO   | 48  | General Purpose Input And Output 5                      | GPIO: Input/Output                                                      |
|                  |      |     |                                                         | Total: 12 Pins                                                          |

### 6.2. Analog I/O Pins

**Table 2. Analog I/O Pins**

| Name              | Type | Pin | Description                                     | Characteristic Definition                                              |
|-------------------|------|-----|-------------------------------------------------|------------------------------------------------------------------------|
| AUX4/<br>MICBIAS2 | IO   | 12  | Auxiliary Input 4/<br>MIC BIAS Voltage Output 2 | Analog input (1Vrms) / Programmable<br>Analog DC Output with 3mA drive |
| X+                | IO   | 14  | Touch Panel Connect Input/Output                | X+ for 4-wire panel                                                    |
| Y+                | IO   | 15  | Touch Panel Connect Input/Output                | Y+ for 4-wire panel                                                    |
| X-                | IO   | 16  | Touch Panel Connect Input/Output                | X- for 4-wire panel                                                    |
| Y-                | IO   | 17  | Touch Panel Connect Input/Output                | Y- for 4-wire panel                                                    |
| PHONEP            | I    | 19  | Phone Positive Input                            | Analog Input (1Vrms)                                                   |
| PHONEN            | I    | 20  | Phone Negative Input                            | Analog Input (1Vrms)                                                   |
| MIC1P             | I    | 21  | First Mic Positive Input                        | Analog Input (1Vrms)                                                   |
| MIC1N/AUX3        | I    | 22  | First Mic Negative Input/<br>Auxiliary Input 3  | Analog Input (1Vrms)                                                   |
| MIC2P             | I    | 29  | Second Mic Positive Input                       | Analog Input (1Vrms)                                                   |
| MIC2N             | I    | 30  | Second Mic Negative Input                       | Analog Input (1Vrms)                                                   |
| LINE_IN_L         | I    | 23  | Line Input Left Channel                         | Analog Input (1Vrms)                                                   |
| LINE_IN_R         | I    | 24  | Line Input Right Channel                        | Analog Input (1Vrms)                                                   |
| MONO_OUT          | O    | 31  | Positive MONO Output                            | Analog Output (1Vrms)                                                  |

| Name       | Type | Pin | Description                           | Characteristic Definition            |
|------------|------|-----|---------------------------------------|--------------------------------------|
| MONO_OUTN  | O    | 32  | Negative MONO Output                  | Analog Output (1Vrms)                |
| HP_OUT_L   | O    | 39  | Headphone Output Left Channel         | Analog Output (1Vrms)                |
| HP_OUT_R   | O    | 41  | Headphone Output Right Channel        | Analog Output (1Vrms)                |
| SPK_OUT_L  | O    | 35  | Speaker Output Left Channel           | Analog Output (1.3Vrms, SPKVDD=4.2V) |
| SPK_OUT_LN | O    | 33  | Negative Speaker Output Left Channel  | Analog Output (1.3Vrms, SPKVDD=4.2V) |
| SPK_OUT_R  | O    | 36  | Speaker Output Right Channel          | Analog Output (1.3Vrms, SPKVDD=4.2V) |
| SPK_OUT_RN | O    | 37  | Negative Speaker Output Right Channel | Analog Output (1.3Vrms, SPKVDD=4.2V) |
|            |      |     |                                       | Total: 21 Pins                       |

### 6.3. Filter/Reference

**Table 3. Filter/Reference**

| Name    | Type | Pin | Description                | Characteristic Definition                    |
|---------|------|-----|----------------------------|----------------------------------------------|
| MICBIAS | O    | 28  | MIC BIAS Voltage Output    | Programmable Analog DC Output with 3mA drive |
| VREF    | O    | 27  | Internal Reference Voltage | 4.7μF capacitor to analog ground             |
|         |      |     |                            | Total: 2 Pins                                |

### 6.4. Power/Ground

**Table 4. Power/Ground**

| Name        | Type | Pin | Description                                    | Characteristic Definition                              |
|-------------|------|-----|------------------------------------------------|--------------------------------------------------------|
| DVDD1       | P    | 1   | Digital VDD                                    | 1.8V~3.6V (IO)                                         |
| DGND1       | P    | 4   | Digital GND                                    | -                                                      |
| DGND2       | P    | 7   | Digital GND                                    | -                                                      |
| DVDD2       | P    | 9   | Digital VDD                                    | 1.8V~3.6V (Core)                                       |
| TPVDD       | P    | 13  | Analog VDD for Touch Panel                     | 2.3V~3.6V                                              |
| TPGND       | P    | 18  | Analog GND for Touch Panel                     | -                                                      |
| AVDD1       | P    | 25  | Analog VDD                                     | 2.3V~3.6V                                              |
| AGND1       | P    | 26  | Analog GND                                     | -                                                      |
| SPKGND      | P    | 34  | Analog GND for Speaker Amps                    | -                                                      |
| SPKVDD      | P    | 38  | Analog VDD for Speaker Amps                    | 3.0V~5V (for ohm loading)<br>2.3V~5V (for ohm loading) |
| HPGND       | P    | 40  | Analog GND for Headphone Amps                  | -                                                      |
| AGND2       | P    | 42  | Analog GND                                     | -                                                      |
| HPVDD       | P    | 43  | Analog VDD for Headphone Amps                  | 2.3V~3.6V                                              |
| Exposed_GND | P    | 49  | Thermal Pad<br>Must be Connected to System GND | -                                                      |
|             |      |     |                                                | Total: 14 Pins                                         |

Note1: DVDD1 ≥ DVDD2, SPKVDD ≥ AVDD1, HPVDD ≥ AVDD1 ≥ DVDD2, TPVDD ≥ DVDD2.

Note2: SPDVDD connect 10μF Capacitor to SPKGND is required.

Note3: The Thermal pad must be connected to system ground.

## 7. Functional Description

### 7.1. Power

The ALC5611 has many power blocks. SPKVDD operates between 2.3V and 5V. HPVDD, TPVDD and AVDD1 operate between 2.3V and 3.6V. DVDD1 and DVDD2 operate between 1.8V and 3.6V. The power supply limit conditions are  $DVDD1 \geq DVDD2$ ,  $SPKVDD \geq AVDD1$ ,  $HPVDD \geq AVDD1 \geq DVDD2$ ,  $TPVDD \geq DVDD2$ , and  $AVDD1 = TPVDD$ .

**Table 5. Power Setting for Best Performance**

| Power   | DVDD1 | DVDD2 | HPVDD | TPVDD | AVDD1 | SPKVDD |
|---------|-------|-------|-------|-------|-------|--------|
| Setting | 3.3V  | 1.8V  | 3.3V  | 3.3V  | 3.3V  | 4.2V   |

### 7.2. Reset

There are 4 types of reset operation: Power-On Reset (POR), Cold, Warm, and Register reset.

**Table 6. Reset Operation**

| Reset Type     | Trigger Condition                                                      | CODEC Response                                                                                                     |
|----------------|------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|
| POR            | Power-On Reset. Monitor digital power supply voltage reaches $V_{POR}$ | Resets all hardware logic and all registers to default values.                                                     |
| Cold Reset     | Asserts RESET# for a specified period                                  | Resets all hardware logic and all registers to default values except some PLL related control registers and logic. |
| Register Reset | Write Reg-00h                                                          | Resets all registers to default values except some PLL related control registers and logic.                        |
| Warm Reset     | Drives SYNC high for specified period without BIT_CLK                  | Reactivates AC-Link. No change to register values.                                                                 |

#### 7.2.1. Power-On Reset (POR)

When powered on, DVDD2 passes through the  $V_{POR}$  band of the ALC5611 ( $V_{POR\_ON} \sim V_{POR\_OFF}$ ), the Power On Reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

**Table 7. Power On Reset Voltage**

| Symbol         | Min | Typical | Max | Unit |
|----------------|-----|---------|-----|------|
| $V_{POR\_ON}$  | 1.0 | -       | 1.6 | V    |
| $V_{POR\_OFF}$ | -   | 1.3     | -   | V    |

Note:  $V_{POR\_OFF}$  must be below  $V_{POR\_ON}$ .

## 7.3. Clocking

The Stereo\_SYSCLK can be selected from MCLK or PLL. This means MCLK is always provided externally, and the driver should arrange the clock of each block and setup each divider.

### 7.3.1. Phase-Locked Loop

A Phase-Locked Loop (PLL) is used to provide a flexible input clock from 2.048MHz to 40MHz. Typical choices are 2.048MHz, 4.096MHz, and 13MHz. The source of the PLL can be set to MCLK or MCLK/2 by setting PLL\_pre\_div.

The ALC5611 SYSCLK frequency is 24.576MHz. If the system cannot provide 24.576MHz to the ALC5611, the PLL of the ALC5611 can be used to generate a frequency near 24.576MHz. As the PLL parameter is configured through the AC link, the input clock to the MCLK pin must be between 2.048MHz and 80MHz. After the AC link is connected, the driver must configure the PLL in order to output a frequency close to the SYSCLK (24.576MHz). The accuracy of audio output frequency will depend on the accuracy of PLL output.

The PLL transmit formula is:

$$F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) \text{ \{Typical K=2\}}$$

**Table 8. AC-Link Clock Setting Table (Unit: MHz)**

| MCLK   | N  | M | F <sub>VCO</sub> | K | F <sub>OUT</sub> |
|--------|----|---|------------------|---|------------------|
| 13     | 66 | 7 | 98.222           | 2 | 24.555           |
| 3.6864 | 78 | 1 | 98.304           | 2 | 24.576           |
| 2.048  | 94 | 0 | 98.304           | 2 | 24.576           |
| 4.096  | 70 | 1 | 98.304           | 2 | 24.576           |

After a Cold Reset, PLL related Registers are reset to default values, however, they are not reset to default values after a soft-reset (write Reg00). Firmware should not power down the PLL when the PLL output is used as Stereo\_SYSCLK.

*Note: The ALC5611 will only be enabled after an AC-Link Warm Reset.*

### 7.3.2. AC'97 Mode

For the AC-Link controller, the BIT\_CLK driven by PLL will only be enabled after a warm reset.

The sampling rate of the stereo ADC and stereo DAC can be configured separately and is controlled by Reg2C (stereo DAC) and Reg32 (stereo ADC).

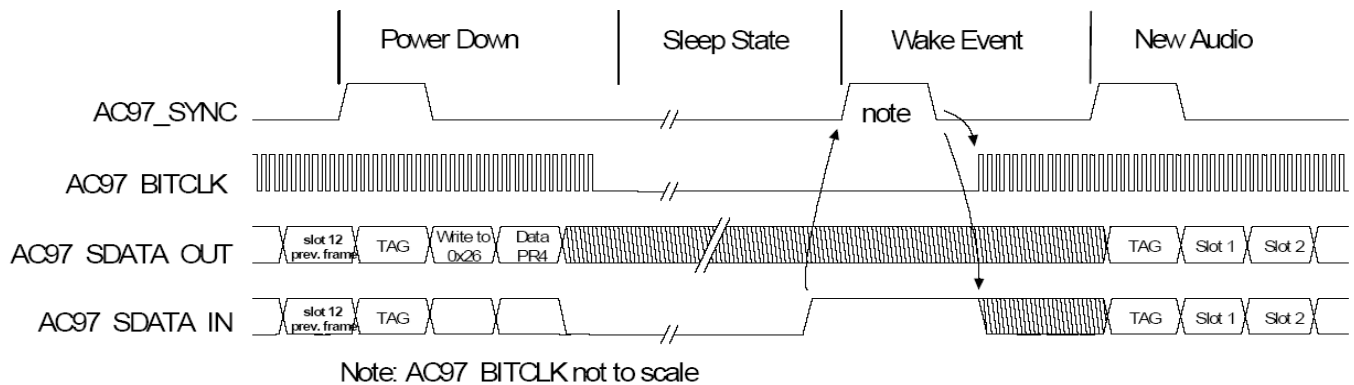
## 7.4. Digital Data Interface

### 7.4.1. AC-Link

When the ALC5611 takes serial data from the AC'97 controller, it samples SDATA\_OUT on the falling edge of BIT\_CLK. When the ALC5611 sends serial data to the AC'97 controller, it starts to drive SDATA\_IN on the rising edge of BIT\_CLK.

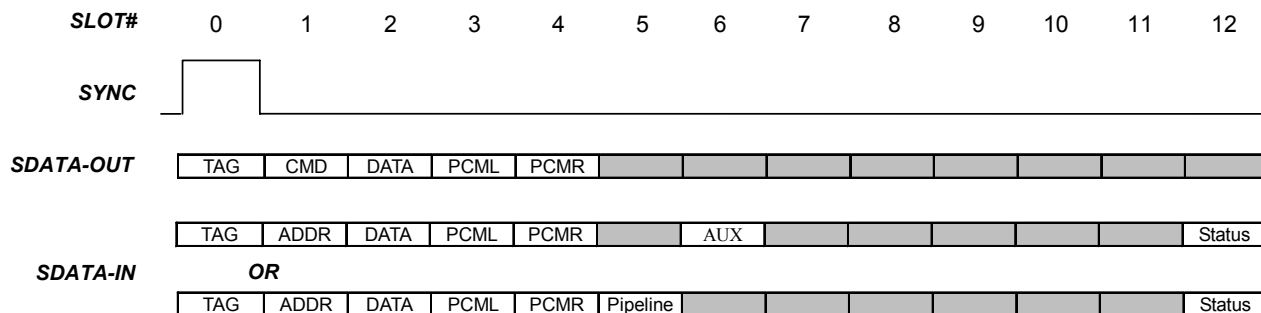
The ALC5611 will return any uninstalled bit or register read operations with 0. The ALC5611 also stuffs an unimplemented slot or bit with 0 in SDATA-IN. Note that AC-Link is MSB-justified.

See the 'Audio CODEC '97 Component Specification Revision 2.2' for detailed information.

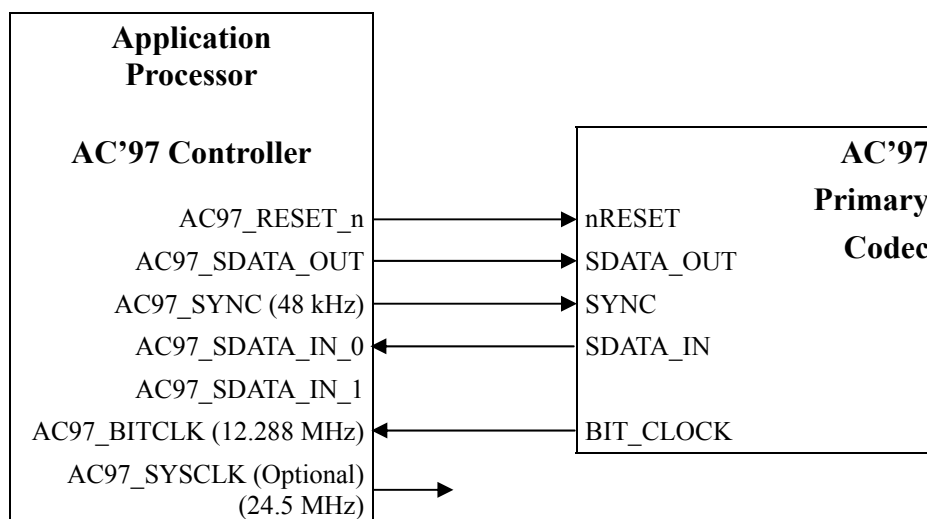


**Figure 4. AC-Link Wake Up Timing**

If wakeup control (Reg52 & Reg5E[1]) is enabled during Sleep state, the ALC5611 will assert SDATA\_IN and IRQOUT when interrupted.



**Figure 5. Default ALC5611 Slot Arrangement – CODEC ID Always 00**



**Figure 6. Controller and Codec Connection**

## **7.5. Audio Data Path**

### **7.5.1. Stereo ADC**

The stereo ADC is used for recording stereo sound.

The sample rate of the stereo ADC is independent of the stereo DAC sample rate.

In order to save power, the left and right ADC can be powered down separately by setting Reg3C [6], [7]. PR0=1 will disable both channels of the ADC.

The volume control of the stereo ADC is set via Reg12[11:7][4:0].

### **7.5.2. Stereo DAC**

The sample rate of the stereo DAC is controlled by Reg2C.

Reg0C[12:8][4:0] can be used to control the volume of DAC output.

### **7.5.3. Mixers**

The ALC5611 supports four mixers for all audio function requirements:

- Headphone mixer for 2 channels
- MONO mixer
- Speaker mixer
- ADC record mixer

#### **7.5.3.1 Headphone Mixer**

The headphone mixer is used to drive stereo output, including HP\_OUT\_L/R, SPK\_OUT\_L/R (SPK\_OUT\_LN/RN) and MONO\_OUT (MONO\_OUTN). The output of the headphone mixer can be input to the ADC record mixer.

The following signals can be mixed into the headphone mixer:

- LINE-IN\_L/R (Controlled by Reg0A)
- PHONEP/N (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)
- ADC record mixer output (Controlled by Reg12 & Reg14).

*Note: The headphone mixer can be powered down by setting Reg3C[5][4].*

### **7.5.3.2 MONO Mixer**

The MONO mixer is used to drive MONO\_OUT (MONO\_OUTN) and SPK\_OUT\_L/R (SPK\_OUT\_LN/RN). The output of the MONO mixer can be input to the ADC record mixer. The output of the MONO mixer is two channels with the same signal.

The following signals can be mixed into the MONO mixer:

- LINE-IN\_L/R (Controlled by Reg0A)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)
- ADC record mixer output (Controlled by Reg12 & Reg14).

*Note: The MONO mixer can be powered down by setting Reg3C[2].*

### **7.5.3.3 Speaker Mixer**

The speaker mixer is the same as the MONO mixer and is used to drive MONO\_OUT (MONO\_OUTN) and SPK\_OUT\_L/R (SPK\_OUT\_LN/RN). The output of the speaker mixer can be input to the ADC record mixer. The output of the speaker mixer is two channels with the same signal.

The following signals can be mixed into the speaker mixer:

- LINE-IN\_L/R (Controlled by Reg0A)
- PHONEP/N (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)

*Note: The speaker mixer can be powered down by setting Reg3C[3].*

### **7.5.3.4 ADC Record Mixer**

The ADC record mixer is used to mix analog signals as input to the Stereo ADC for recording. Output of the ADC record mixer can be input to the headphone mixer, MONO mixer, and speaker mixer.

The following signals can be mixed into the ADC record mixer:

- LINE-IN\_L/R (Controlled by Reg0A)
- PHONEP/N (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Headphone mixer output
- MONO mixer output
- Speaker mixer output

*Note: The ADC record mixer can be powered down by setting Reg3C[1][0].*

### 7.5.4. Analog Audio Input Path

The ALC5611 supports four Analog Audio Input paths:

- Line\_IN\_L/R
- PHONEP/N
- MIC1
- MIC2

#### 7.5.4.1 Line Input

Line\_In\_L and Line\_In\_R provide 2-channel stereo single-ended input that can be mixed into the MONO mixer, Headphone mixer, Speaker mixer, or the ADC record mixer.

The Line\_In\_L/R volume and mute are controlled by Reg0A. Reg3E[7:6] can be used to power down Line\_In volume control.

#### 7.5.4.2 Phone Input

PHONEP/N provides one-channel MONO differential or single-ended input configured by Reg08[13] that can be mixed into the ADC record mixer, or any analog output mixer except for the MONO mixer. PHONEP is main input when differential mode is disabled.

The PHONEP/N volume and mute are controlled by Reg08. Reg3E[5:4] can be used to power down the PHONEP/N volume control and mixer.

#### 7.5.4.3 Microphone Input

MIC1P/N and MIC2P/N provide two-channel stereo differential or single-ended input via Reg10[12], [4], that can be mixed into the ADC record mixer, or any analog output mixer. MIC1P and MIC2P are main inputs when differential mode is disabled. MIC1N is pin-shared to AUX3 input.

The ALC5611 Microphone input boost provides 20/30/40dB boost, set by Reg22[11:10] (for MIC1), and by Reg22[9:8] (for MIC2). The MIC1/2 volume and mute are controlled by Reg0E.

For detailed power management of MIC1/2, Reg3E[3][2] can be used to power down the MIC1/2 volume control. Reg3E[1][0] can be used to power down MIC1/2 boost.

#### 7.5.4.4 *MIC1N/AUX3 and MICBIAS2/AUX4 Pin Sharing*

MIC1N is pin-shared with AUX3 input of AUX\_ADC. MICBIAS2 is pin-shared with AUX4 input of AUX\_ADC. The driver must set the related register as shown in Table 9.

**Table 9. Pin Sharing Configuration Table**

| AUX3_mic1n_sharing | AUX4_micbias2_sharing | Reg76[0]:<br>Aux_measure_sel | Reg76[7]:<br>AUX_measure_en | Reg10[12]:<br>micl_diff_ctrl | Reg3A[2]:<br>pow_mic2_bias |
|--------------------|-----------------------|------------------------------|-----------------------------|------------------------------|----------------------------|
| MIC1N              | AUX4                  | AUX4 (0'b)                   | -                           | -                            | Disable (0'b)              |
| MIC1N              | MICBIAS2              | -                            | 0'b                         | -                            | -                          |
| AUX3               | AUX4                  | AUX3/AUX4<br>(1'b/0'b)       | -                           | Disable (0'b)                | Disable (0'b)              |
| AUX3               | MICBIAS2              | AUX3 (1'b)                   | -                           | Disable (0'b)                | -                          |

### 7.5.5. Analog Audio Output Data Path

The ALC5611 supports three Analog Audio output paths:

- SPK\_OUT\_L/R
- HP\_OUT\_L/R
- MONO\_OUT

#### 7.5.5.1 *Speaker Output*

SPK\_OUT\_L/R provides two-channel differential output.

The SPK\_OUT\_L source is set in Reg1C[15:14]. Sources are shown below:

- Vmid
- Headphone left mixer
- Speaker mixer
- MONO mixer

The SPK\_OUT\_R source is set in Reg1C[12:11]. Sources are shown below:

- Vmid
- Headphone right mixer
- Speaker mixer
- MONO mixer

The ALC5611 speaker supports Class-AB and Class-D type amplifiers (set in Reg1C[13]:spk\_out\_sel). As the voltage of SPKVDD is usually higher than AVDD, the driver should set the Class-AB Vmid ratio in Reg40[5:3], and the Class-D Vmid ratio in Reg40[7:6] in order to extend the output level.

In Class-AB mode, for single stereo speaker solutions, SPK\_OUT\_R can select a different signal source (SPKR Volume output or SPKL Volume output by Reg1C[14]) but SPK\_OUT\_RN only outputs SPKR Volume Negative Output.

The SPK\_OUT\_L/R volume and mute are controlled by Reg02.

Reg3E[13:12]and Reg3E[9:8] can be used to power down SPK output.

Reg3C[14]: pow\_clsab is used to power down Class-AB output.

SPK\_OUT\_L/R supports the zero-cross detect function (enabled at Reg02[6][14]: sp\_l\_dezero/sp\_r\_dezero).

### **7.5.5.2 Headphone Output**

HP\_OUT\_L/R provides two-channel single-ended output. The HP\_OUT\_L/R source is set in Reg1C[9][8]. Sources are shown below:

- Vmid
- Headphone mixer

The HP\_OUT\_L/R volume and mute are controlled by Reg04.

Reg3E[11]: pow\_hp\_l\_vol and Reg3E[10]: pow\_hp\_r\_vol can be used to power down the volume of HP output.

HP\_OUT supports the zero-cross detect function (enabled at Reg04[14][6]:hp\_l\_dezero/ hp\_r\_dezero).

### **7.5.5.3 MONO Output**

MONO\_OUT provide one-channel differential or single-ended output configured by Reg08[15]. The MONO\_OUT source is set in Reg1C[7:6]. Sources are shown below:

- Vmid
- Headphone mixer (L+R)
- Speaker mixer
- MONO mixer

The MONO\_OUT volume and mute are controlled by Reg08.

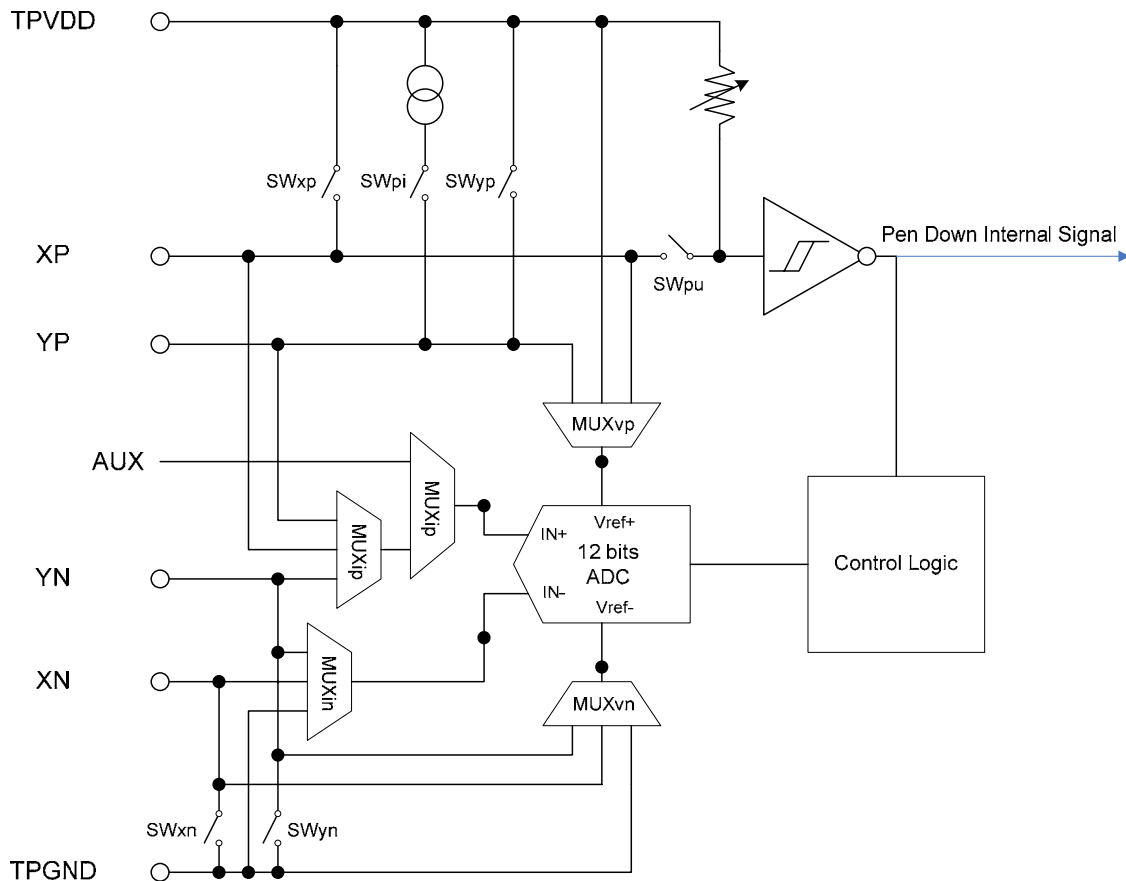
Reg3E[14]: pow\_MONO\_out\_vol can be used to power down the volume of MONO\_OUT.

MONO\_OUT supports the zero-cross detect function (enabled at Reg08[6]:MONO\_dezero).

## 7.6. Touch Panel Control

The ALC5611 provides 4-wire resistive touch panel control. X-position, Y-position, Pen-down detection, touch pressure, and AUX measurement are supported by using AUX\_ADC.

There are 2 modes within the touch panel measurement: Continuous mode (Reg76[14]=1), and polling mode (Reg76[14]=0).



**Figure 7. 4-Wire Resistive Touch Panel Circuit**

### Continuous Mode

The ALC5611 automatically initializes the measurement at the rate set in Reg74[1:0], and sends the measured data back to the AC'97 Controller. It is strongly recommended that the total measure time of one measure cycle (Delay time + measure time) not be longer than the measurement frame period (1/measurement rate).

### Polling Mode

In polling mode the AC'97 Controller starts each measurement by setting the measure item and writing Reg76[15]=1. The ALC5611 will clear the Reg76[15] after measurement is complete.

## 7.7. AVC Control

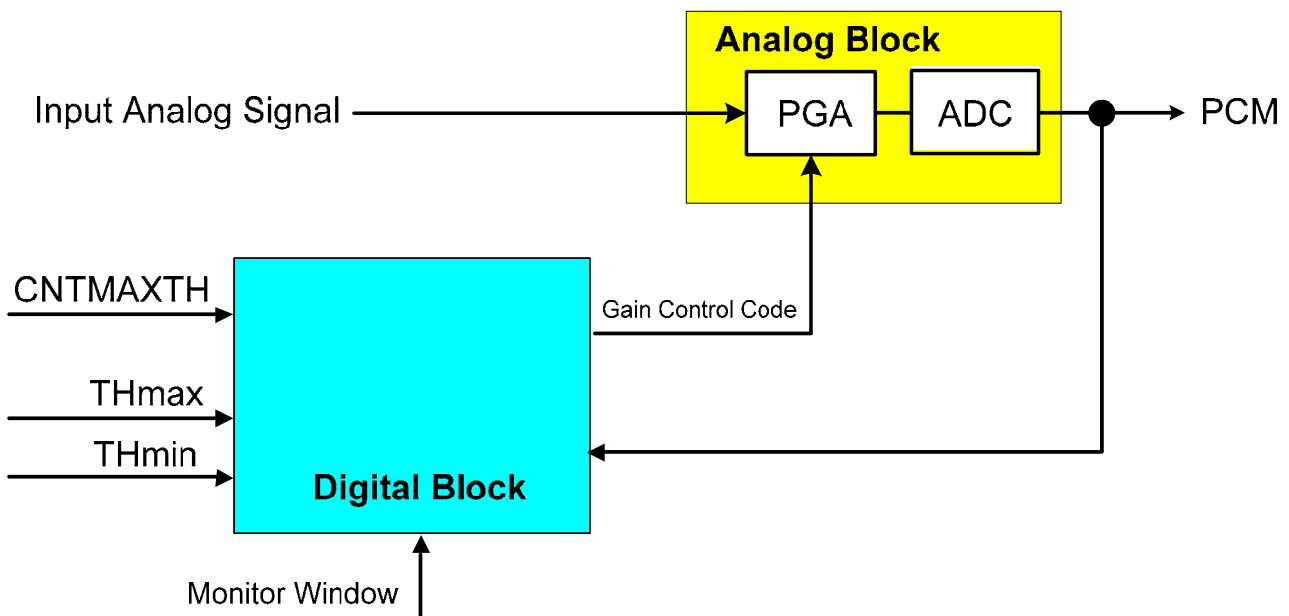
The Automatic Volume Control (AVC) function dynamically adjusts the input signal quantized by the ADC to an expected sound level by setting THmax and THmin.

When the average level of input signal is higher than THmax, the AVC will decrease the selected analog gain to attenuate the quantized Pulse Code Modulation (PCM) signal to a lower amplitude than THmax.

When the average level of input signal is lower than THmin, the AVC will increase the selected analog gain to amplify the input signal. The quantized Pulse Code Modulation (PCM) signal is then set higher than THmin. The quantized PCM has an average level between THmin and THmax.

The AVC reference source channel and target channel can be individually set by Index20[0] and Reg5E[13:12].

The AVC architecture is shown in Figure 8 below:



**Figure 8. Auto Volume Control Block Diagram**

## **7.8. Hardware Sound Effects**

The Sound Effect block is composed of Pseudo Stereo, Spatial 3D and Equalizer blocks. The Pseudo Stereo block is used to convert a MONO source into virtualized stereo output. The Spatial 3D block is a surround sound generator with adjustable amplitude (Gain) and surround depth (Ratio). The Equalizer block can be used to compensate for speaker response, or to make environment sound effects, e.g., ‘Pub’, ‘Live’, ‘Rock’,... etc..

### **7.8.1. Equalizer Block**

The Equalizer block cascades 5 bands of equalizer to compensate for speaker response and to emulate environment sound. One high-pass filter cascaded in the front end is used to drop low frequency tone, which has a larger amplitude and may damage a mini speaker.

The high-pass filter can also be used to adjust Treble strength with gain control. A low-pass filter with gain control can adjust the Bass strength. Three bands of bi-quad bandpass filters are used to emulate environment sounds.

To avoid internal PCM data sample saturation, the digital volume control has up to 18dB of attenuation before the equalizer. A 0~+18dB digital gain after the equalizer is used to correct internal PCM data output to a suitable level.

### **7.8.2. Pseudo Stereo and Spatial 3D Sound**

There are two spatial effects in post-processing; the Pseudo-Stereo Effect + Spatial Effect, and the Stereo Expansion Effect. The Pseudo-Stereo Effect + Spatial Effect converts a MONO signal to a stereo signal by changing the phase and amplitude of the original signal followed by enhancing the spatial effect. The Stereo Expansion Effect enhances the spatial effect when the input signal is Stereo.

## **7.9. Odd-Addressed Register Access**

The ALC5611 will return ‘0000h’ when odd-addressed and unimplemented registers are read.

## 7.10. Power Management

The ALC5611 supports a standard power down control register as defined in AC'97 (Reg26). More detailed Power Management control is supported in Reg 3C & 3E. Each particular block will only be active when both Reg26 and Reg3C/3E are set to 'Enable'.

### 7.10.1. Sleep Mode

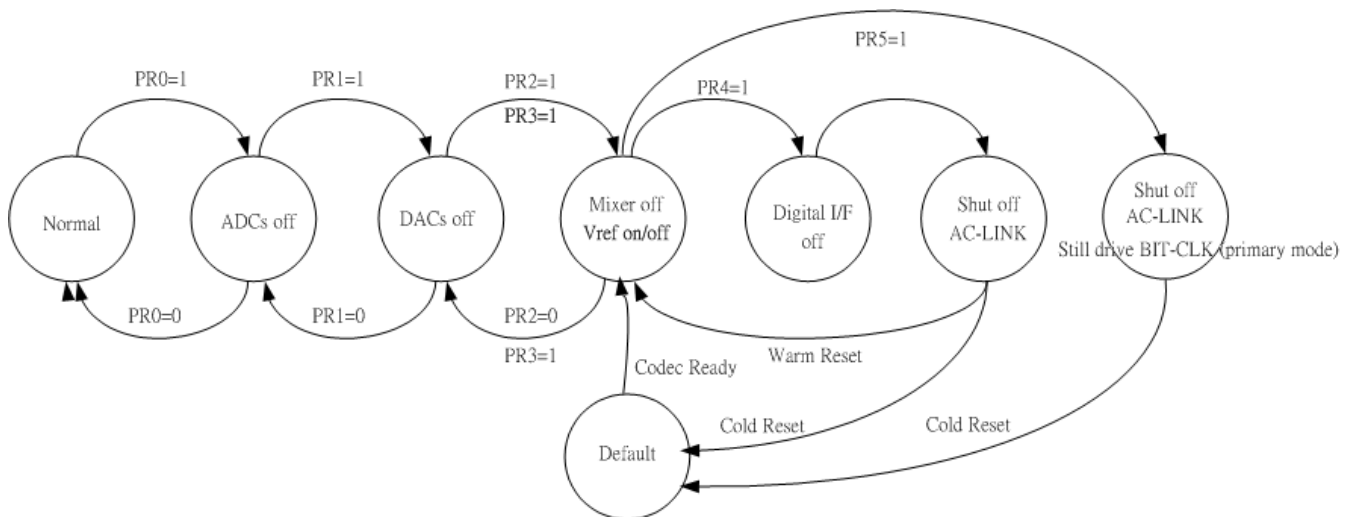
When PR4 (Reg26) is set, the ALC5611 will enter Sleep Mode. Before entering sleep mode, the driver can set other control bits to save power according to system requirements.

The following functions should be kept operating during sleep mode:

- Pen-down Detection
- GPIO and Interrupts
- Analog to analog path when control registers Reg 3C & 3E are enabled

There are two methods to wake the ALC5611 from Sleep mode

- Warm Reset and Cold Reset from AC Link
- Wake-up from GPIO (configured as Input) and Internal event signal (pen-down, over-temperature) when the wake-up bit is set at Reg52.



**Figure 9. Example of ALC5611 Power-Down/Power-Up Flow**

## 7.11. GPIO and Interrupt

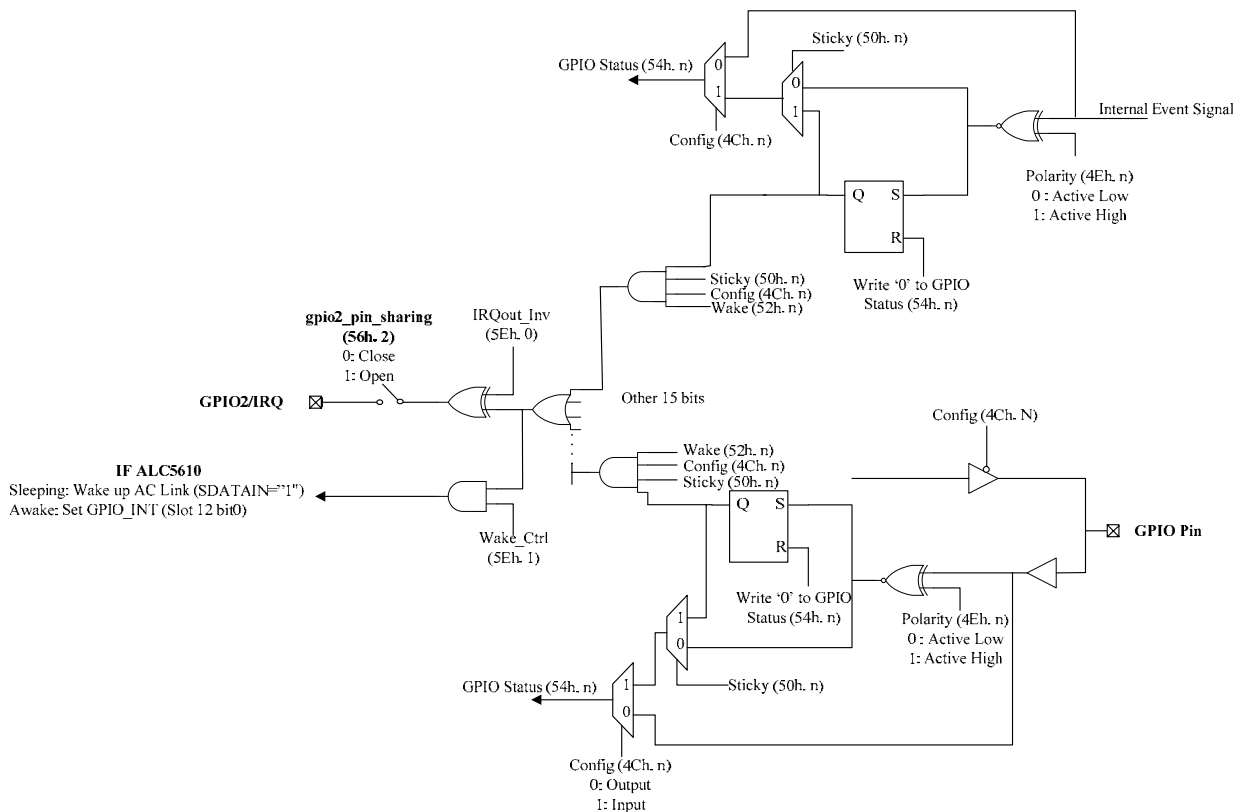
The ALC5611 supports up to five GPIOs. Each GPIO can be configured as Input/Output by Reg4C. When GPIOs are configured as Input, the status will be indicated in Reg54 and Slot 12. When GPIOs are configured as Output, Reg5C is used to drive GPIOs to High (1b) or Low (0b). The status can be read in Reg54.

Interrupt request (IRQ) function can be configured as:

- Sticky by setting Reg50
- Changed polarity by setting Reg4E
- Wake-up by setting Reg52

The wake-up function will drive SDATA\_In 'high' when the AC-Link is in sleep mode, and set GPIO\_INT (Slot12 bit0) when the AC-Link is awake. The wake up function can only be enabled when Wake-up control (Reg5E[1])=1. The driver can write each bit of Reg54=1 to clear each IRQ status flag.

GPIO pin2 can be configured and pin-shared with IRQ\_Output by setting Reg56.



**Figure 10. GPIO Implementation**

There are some internal events (pen-down, over-temperature, MICBIAS short detect) where GPIOs can be an interrupt source. GPIO Internal event application is located in Reg4C, Reg4E, Reg50, Reg52, and Reg54.

## 8. Mixer Registers List

Accessing odd numbered registers, or reading unimplemented registers, will return a 0.

### 8.1. Reg-00h: Reset

Default: 59B4h

**Table 10. Reg-00h: Reset**

| Name           | Bits  | Read/Write | Reset State | Description                                                              |
|----------------|-------|------------|-------------|--------------------------------------------------------------------------|
| Reserved       | 15    | R          | 0'h         | Reserved. Read as 0                                                      |
| REG-00_b14_b10 | 14:10 | R          | 16'h        | SE[4:0]=10110b                                                           |
| REG-00_b9      | 9     | R          | 0'h         | No Support for 20-Bit ADC                                                |
| REG-00_b8      | 8     | R          | 1'h         | Supports 16-Bit ADC                                                      |
| REG-00_b7      | 7     | R          | 1'h         | Supports 16-Bit DAC                                                      |
| REG-00_b6      | 6     | R          | 0'h         | No Support for 18-Bit DAC                                                |
| REG-00_b5      | 5     | R          | 1'h         | Support for Loudness                                                     |
| REG-00_b4      | 4     | R          | 1'h         | Headphone Output Support                                                 |
| Reserved       | 3     | R          | 0'h         | Reserved                                                                 |
| REG-00_b2      | 2     | R          | 1'h         | Supports EQ Control                                                      |
| Reserved       | 1     | R          | 0'h         | Reserved. Read as 0                                                      |
| REG-00_b0      | 0     | R          | 0'h         | Dedicated MIC PCM input is not supported. Can be for touch panel ADC use |

*Note: Writes to this register will reset all registers to their default values except PLL related Register. The written data will be ignored.*

### 8.2. Reg-02h: Speaker Output Volume

Default: 8080h

**Table 11. Reg-02h: Speaker Output Volume**

| Name        | Bits | Read/Write | Reset State | Description                                                                   |
|-------------|------|------------|-------------|-------------------------------------------------------------------------------|
| sp_l_mute   | 15   | RW         | 1'h         | Mute Left Control<br>0: On                      1: Mute Left Channel (-∞dB)   |
| sp_l_dezero | 14   | RW         | 0'h         | Left Zero-Cross Detector Control<br>0: Disable              1: Enable         |
| Reserved    | 13   | R          | 0'h         | Reserved. Read as 0                                                           |
| sp_l_vol    | 12:8 | RW         | 0'h         | Speaker Output Left Volume (SPKL[4:0]) in 1.5dB Steps                         |
| sp_r_mute   | 7    | RW         | 1'h         | Mute Right Control<br>0: On                      1: Mute Right Channel (-∞dB) |
| sp_r_dezero | 6    | RW         | 0'h         | Right Zero-Cross Detector Control<br>0: Disable              1: Enable        |
| Reserved    | 5    | R          | 0'h         | Reserved. Read as 0                                                           |
| sp_r_vol    | 4:0  | RW         | 0'h         | Speaker Output Right Volume (SPKR[4:0]) in 1.5dB Steps                        |

*Note: For SPKR/SPKL, 00h: 0dB attenuation*

*1Fh: 46.5dB attenuation*

### 8.3. Reg-04h: Headphone Output Volume

Default: 8080h

### Table 12. Reg-04h: Headphone Output Volume

| Name        | Bits | Read/Write | Reset State | Description                                                                            |
|-------------|------|------------|-------------|----------------------------------------------------------------------------------------|
| hp_l_mute   | 15   | RW         | 1'h         | Mute Left Control<br>0: On                      1: Mute Left Channel ( $-\infty$ dB)   |
| hp_l_dezero | 14   | RW         | 0'h         | Left Zero-Cross Detector Control<br>0: Disable                1: Enable                |
| Reserved    | 13   | R          | 0'h         | Reserved. Read as 0                                                                    |
| hp_l_vol    | 12:8 | RW         | 0'h         | Headphone Output Left Volume (HPL[4:0]) in 1.5dB Steps                                 |
| hp_r_mute   | 7    | RW         | 1'h         | Mute Right Control<br>0: On                      1: Mute Right Channel ( $-\infty$ dB) |
| hp_r_dezero | 6    | RW         | 0'h         | Right Zero-Cross Detector Control<br>0: Disable                1: Enable               |
| Reserved    | 5    | R          | 0'h         | Reserved. Read as 0                                                                    |
| hp_r_vol    | 4:0  | RW         | 0'h         | Headphone Output Right Volume (HPR[4:0]) in 1.5dB Steps                                |

*Note: For HPR/HPL, 00h: 0dB attenuation*

*1Fh: 46.5dB attenuation*

#### 8.4. *Reg-08h: Phone Input/MONO Output Volume*

Default: C880h

### Table 13. Reg-08h: Phone Input/MONO Output Volume

| Name            | Bits | Read/Write | Reset State | Description                                                                              |
|-----------------|------|------------|-------------|------------------------------------------------------------------------------------------|
| phone2hp_mute   | 15   | RW         | 1'h         | Mute Phone Input to Headphone Mixer Control<br>0: On                      1: Mute (-∞dB) |
| phone2spk_mute  | 14   | RW         | 1'h         | Mute Phone Input to Speaker Mixer Control<br>0: On                      1: Mute (-∞dB)   |
| phone_diff_ctrl | 13   | RW         | 0'h         | Phone Differential Input Control<br>0: Disable                1: Enable                  |
| phone_vol       | 12:8 | RW         | 8'h         | Phone Input Volume (PV[4:0]) in 1.5dB Steps (not to ADC)                                 |
| MONO_mute       | 7    | RW         | 1'h         | Mute MONO Output Control<br>0: On                      1: Mute (-∞dB)                    |
| MONO_dezero     | 6    | RW         | 0'h         | Zero-Cross Detector Control<br>0: Disable                1: Enable                       |
| MONO_diff_ctrl  | 5    | RW         | 0'h         | MONO Output Differential Control<br>0: Disable (SE)        1: Enable (BTL)               |
| MONO_vol        | 4:0  | RW         | 0'h         | MONO Output Master Volume (MOV[4:0]) in 1.5dB Steps                                      |

*Note: For MOV, 00h: 0dB attenuation*

*1Fh: 46.5dB attenuation*

For PV, 00h: +12dB gain

08h: 0dB attenuation

*1Fh: 34.5dB attenuation*

## 8.5. Reg-0Ah: LINE\_IN Volume

Default: E808h

**Table 14. Reg-0Ah: LINE\_IN Volume**

| Name         | Bits | Read/Write | Reset State | Description                                                    |
|--------------|------|------------|-------------|----------------------------------------------------------------|
| li2hp_mute   | 15   | RW         | 1'h         | Mute Volume Output to Headphone Mixer Control<br>0: On 1: Mute |
| li2spk_mute  | 14   | RW         | 1'h         | Mute Volume Output to Speaker Mixer Control<br>0: On 1: Mute   |
| li2MONO_mute | 13   | RW         | 1'h         | Mute Volume Output to MONO Mixer Control<br>0: On 1: Mute      |
| li_l_vol     | 12:8 | RW         | 08'h        | LINE_IN Left Volume (NLV[4:0]) in 1.5dB Steps                  |
| Reserved     | 7:5  | R          | 0'h         | Reserved                                                       |
| li_r_vol     | 4:0  | RW         | 8'h         | LINE_IN Right Volume (NRV[4:0]) in 1.5dB Steps                 |

Note: For NRV/NLV, 00h: +12dB gain

08h: 0dB attenuation

1Fh: 34.5dB attenuation

## 8.6. Reg-0Ch: STEREO DAC Volume

Default: E808h

**Table 15. Reg-0Ch: STEREO DAC Volume**

| Name          | Bits | Read/Write | Reset State | Description                                                           |
|---------------|------|------------|-------------|-----------------------------------------------------------------------|
| dac2hp_mute   | 15   | RW         | 1'h         | Mute Volume Output to Headphone Mixer Control<br>0: On 1: Mute (-∞dB) |
| dac2spk_mute  | 14   | RW         | 1'h         | Mute Volume Output to Speaker Mixer Control<br>0: On 1: Mute (-∞dB)   |
| dac2mono_mute | 13   | RW         | 1'h         | Mute Volume Output to MONO Mixer Control<br>0: On 1: Mute (-∞dB)      |
| dac_l_vol     | 12:8 | RW         | 08'h        | Left DAC Volume (PLV[4:0]) in 1.5dB Steps                             |
| Reserved      | 7:5  | R          | 0'h         | Reserved                                                              |
| dac_r_vol     | 4:0  | RW         | 8'h         | Right DAC Volume (PRV[4:0]) in 1.5dB Steps                            |

Note: For PRV/PLV, 00h: +12dB gain

08h: 0dB attenuation

1Fh: 34.5dB attenuation

## 8.7. Reg-0Eh: MIC Volume

Default: 0808h

**Table 16. Reg-0Eh: MIC Volume**

| Name     | Bits  | Read/Write | Reset State | Description                           |
|----------|-------|------------|-------------|---------------------------------------|
| Reserved | 15:13 | R          | 0'h         | Reserved                              |
| mic1_vol | 12:8  | RW         | 08'h        | MIC1 Volume (M1V[4:0]) in 1.5dB Steps |
| Reserved | 7:5   | R          | 0'h         | Reserved                              |
| mic2_vol | 4:0   | RW         | 8'h         | MIC2 Volume (M2V[4:0]) in 1.5dB Steps |

Note: For M2V/M1V, 00h: +12dB gain

08h: 0dB attenuation

1Fh: 34.5dB attenuation

## 8.8. Reg-10h: MIC Routing Control

Default: E0E0h

**Table 17. Reg-10h: MIC Routing Control**

| Name           | Bits | Read/Write | Reset State | Description                                                                      |
|----------------|------|------------|-------------|----------------------------------------------------------------------------------|
| mic12hp_mute   | 15   | RW         | 1'h         | Mute MIC1 Volume Output to Headphone Mixer<br>0: On                      1: Mute |
| mic12spk_mute  | 14   | RW         | 1'h         | Mute MIC1 Volume Output to Speaker Mixer<br>0: On                      1: Mute   |
| mic12MONO_mute | 13   | RW         | 1'h         | Mute MIC1 Volume Output to MONO Mixer<br>0: On                      1: Mute      |
| mic1_diff_ctrl | 12   | RW         | 0'h         | MIC1 Differential Input Control<br>0: Disable              1: Enable             |
| Reserved       | 11:8 | R          | 0'h         | Reserved                                                                         |
| mic22hp_mute   | 7    | RW         | 1'h         | Mute MIC2 Volume Output to Headphone Mixer<br>0: On                      1: Mute |
| mic22spk_mute  | 6    | RW         | 1'h         | Mute MIC2 Volume Output to Speaker Mixer<br>0: On                      1: Mute   |
| mic22MONO_mute | 5    | RW         | 1'h         | Mute MIC2 Volume Output to MONO Mixer<br>0: On                      1: Mute      |
| mic2_diff_ctrl | 4    | RW         | 0'h         | MIC2 Differential Input Control<br>0: Disable              1: Enable             |
| Reserved       | 3:0  | R          | 0'h         | Reserved                                                                         |

## 8.9. Reg-12h: ADC Record Gain

Default: F58Bh

**Table 18. Reg-12h: ADC Record Gain**

| Name            | Bits | Read/Write | Reset State | Description                                                                                                                      |
|-----------------|------|------------|-------------|----------------------------------------------------------------------------------------------------------------------------------|
| adc2hp_l_mute   | 15   | RW         | 1'h         | Mute Left Gain Output to Headphone Mixer Control<br>0: On                      1: Mute ( $-\infty$ dB)                           |
| adc2hp_r_mute   | 14   | RW         | 1'h         | Mute Right Gain Output to Headphone Mixer Control<br>0: On                      1: Mute ( $-\infty$ dB)                          |
| adc2MONO_l_mute | 13   | RW         | 1'h         | Mute Left Gain Output to MONO Mixer Control<br>0: On                      1: Mute ( $-\infty$ dB)                                |
| adc2MONO_r_mute | 12   | RW         | 1'h         | Mute Right Gain Output to MONO Mixer Control<br>0: On                      1: Mute ( $-\infty$ dB)                               |
| adc_l_vol       | 11:7 | RW         | 0B'h        | ADC Record Gain Left Channel (LRG[4:0]) in 1.5dB Steps<br>00h: -16.5dB attenuation<br>0Bh: 0dB gain              1Fh: 30dB gain  |
| adc_l_dezero    | 6    | RW         | 0'h         | ADC_L Zero-Cross Detector Control<br>0: Disable              1: Enable                                                           |
| adc_r_dezero    | 5    | RW         | 0'h         | ADC_R Zero-Cross Detector Control<br>0: Disable              1: Enable                                                           |
| adc_r_vol       | 4:0  | RW         | 0B'h        | ADC Record Gain Right Channel (RRG[4:0]) in 1.5dB Steps<br>00h: -16.5dB attenuation<br>0Bh: 0dB gain              1Fh: 30dB gain |

## 8.10. Reg-14h: ADC Record Mixer Control

Default: 7F7Fh

**Table 19. Reg-14h: ADC Record Mixer Control**

| Name          | Bits | Read/Write | Reset State | Description                                                                                                                                                                                                   |
|---------------|------|------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved      | 15   | R          | 0'h         | Reserved                                                                                                                                                                                                      |
| adcrec_l_mute | 14:8 | RW         | 7F'h        | Left Mixer Mute Control<br>0: On<br>1: Mute (-∞dB)<br>Bit 14: MIC1<br>Bit 13: MIC2<br>Bit 12: LINE_IN_L<br>Bit 11: PHONE<br>Bit 10: Headphone Mixer Left Channel<br>Bit 9: Speaker Mixer<br>Bit 8: MONO Mixer |
| Reserved      | 7    | R          | 0'h         | Reserved                                                                                                                                                                                                      |
| adcrec_r_mute | 6:0  | RW         | 7F'h        | Right Mixer Mute Control<br>0: On<br>1: Mute (-∞dB)<br>Bit 6: MIC1<br>Bit 5: MIC2<br>Bit 4: LINE_IN_R<br>Bit 3: PHONE<br>Bit 2: Headphone Mixer Right Channel<br>Bit 1: Speaker Mixer<br>Bit 0: MONO Mixer    |

## 8.11. Reg-1Ch: Output Mixer Control

Default: 0000h

**Table 20. Reg-1Ch: Output Mixer Control**

| Name             | Bits  | Read/Write | Reset State | Description                                                                                                |
|------------------|-------|------------|-------------|------------------------------------------------------------------------------------------------------------|
| spk_l_vol_in_sel | 15:14 | RW         | 0'h         | SPKL Volume Input Select<br>00: VMID (No input)      01: HP Left Mixer<br>10: Speaker mixer      11: MONO  |
| spk_l_out_sel    | 13    | RW         | 0'h         | SPKL and SPKR Output Select<br>0: Class-AB      1: Class-D                                                 |
| spk_r_vol_in_sel | 12:11 | RW         | 0'h         | SPKR Volume Input Select<br>00: VMID (No input)      01: HP Right Mixer<br>10: Speaker Mixer      11: MONO |
| Reserved         | 10    | R          | 0'h         | Reserved                                                                                                   |

| Name                | Bits | Read/Write | Reset State | Description                                                                                                                                                             |
|---------------------|------|------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| hp_l_in_sel         | 9    | RW         | 0'h         | HPL Volume Input Select<br>0: VMID (No input)      1: HP Left Mixer                                                                                                     |
| hp_r_in_sel         | 8    | RW         | 0'h         | HPR Volume Input Select<br>0: VMID (No input)      1: HP Right Mixer                                                                                                    |
| MONO_in_sel         | 7:6  | RW         | 0'h         | MONO Volume Input Select<br>00: VMID (No input)      01: HP Left + Right Mixer<br>10: Speaker Mixer      11: MONO Mixer                                                 |
| Reserved            | 5    | R          | 0'h         | Reserved                                                                                                                                                                |
| clab_amp_source_sel | 4    | RW         | 0'h         | In Class-AB Mode<br>SPK_OUT_R Output Amplifier Source Select<br>0: SPKR Volume Output<br>1: SPKL Volume Output<br><i>Note: SPK_OUT_RN: SPKR Volume Negative Output.</i> |
| Reserved            | 3:0  | R          | 0'h         | Reserved                                                                                                                                                                |

## 8.12. Reg-22h: Microphone Control

Default: 0000h

**Table 21. Reg-22h: Microphone Control**

| Name                   | Bits  | Read/Write | Reset State | Description                                                                            |
|------------------------|-------|------------|-------------|----------------------------------------------------------------------------------------|
| Reserved               | 15:12 | R          | 0'h         | Reserved                                                                               |
| mic1_boost_ctrl        | 11:10 | RW         | 0'h         | MIC1 Boost Control<br>00: Bypass      01: +20dB<br>10: +30dB      11: +40dB            |
| mic2_boost_ctrl        | 9:8   | RW         | 0'h         | MIC2 Boost Control<br>00: Bypass      01: +20dB<br>10: +30dB      11: +40dB            |
| Reserved               | 7:6   | R          | 0'h         | Reserved. Read as 0                                                                    |
| mic1_bias_voltage_ctrl | 5     | RW         | 0'h         | MICBIAS1 Output Voltage Control<br>0: 0.9*AVDD      1: 0.75*AVDD                       |
| mic2_bias_voltage_ctrl | 4     | RW         | 0'h         | MICBIAS2 Output Voltage Control<br>0: 0.9*AVDD      1: 0.75*AVDD                       |
| Reserved               | 2:3   | R          | 0'h         | Reserved. Read as 0                                                                    |
| mic_bias_threshold     | 1:0   | RW         | 0'h         | MICBIAS1/2 Short Current Detector Threshold<br>00: 600μA      01: 1200μA<br>1x: 1800μA |

### 8.13. Reg-26h: Power Down Control/Status

Default: EF00h

**Table 22. Reg-26h: Power Down Control/Status**

| Name                | Bits | Read/Write | Reset State | Description                                                                                                                |
|---------------------|------|------------|-------------|----------------------------------------------------------------------------------------------------------------------------|
| ac_pr7              | 15   | RW         | 1'h         | PR7<br>0: Normal<br>1: Power down Speaker Amplifier                                                                        |
| ac_pr6              | 14   | RW         | 1'h         | PR6<br>0: Normal<br>1: Power down Headphone Out and MONO Out                                                               |
| ac_pr5              | 13   | RW         | 1'h         | PR5<br>0: Normal<br>1: Disable internal clock of AC'97 (Without PLL)                                                       |
| ac_pr4              | 12   | RW         | 0'h         | PR4<br>0: Normal<br>1: Power down AC-Link<br><i>Note: Though this bit is read as 1, write 1 to power down the AC-Link.</i> |
| ac_pr3              | 11   | RW         | 1'h         | PR3<br>0: Normal<br>1: Power down Mixer (Vref/Vrefout off)                                                                 |
| ac_pr2              | 10   | RW         | 1'h         | PR2<br>0: Normal<br>1: Power down Mixer (Vref/Vrefout are still on)                                                        |
| ac_pr1              | 9    | RW         | 1'h         | PR1<br>0: Normal<br>1: Power down STEREO DAC                                                                               |
| ac_pr0              | 8    | RW         | 1'h         | PR0<br>0: Normal<br>1: Power down STEREO ADC, and input MUX                                                                |
| Reserved            | 7:4  | R          | 0'h         | Reserved. Read as 0                                                                                                        |
| vref_status         | 3    | R          | 0'h         | Vref Status<br>1: Vref is up to normal level<br>0: Not yet up to normal level                                              |
| analog_mixer_status | 2    | R          | 0'h         | Analog Mixer Status<br>1: Ready<br>0: Not yet ready                                                                        |
| dac_status          | 1    | R          | 0'h         | DAC Status<br>1: Ready<br>0: Not yet ready (Inverse of PR1)                                                                |
| adc_status          | 0    | R          | 0'h         | ADC Status<br>1: Ready<br>0: Not yet ready (Inverse of PR0)                                                                |

**Table 23. Truth Table for Power Down Mode (PD=Power Down)**

|       | ADC | DAC | Mixer | Vref | ACLINK | Int CLK | HP-OUT | MONO-OUT | SPK-OUT |
|-------|-----|-----|-------|------|--------|---------|--------|----------|---------|
| PR0=1 | PD  | -   | -     | -    | -      | -       | -      | -        | -       |
| PR1=1 | -   | PD  | -     | -    | -      | -       | -      | -        | -       |
| PR2=1 | -   | -   | PD    | -    | -      | -       | PD     | -        | -       |
| PR3=1 | PD  | PD  | PD    | PD   | -      | -       | PD     | -        | -       |
| PR4=1 | PD  | PD  | -     | -    | PD     | -       | -      | -        | -       |
| PR5=1 | PD  | PD  | -     | -    | PD     | PD      | -      | -        | -       |
| PR6=1 | -   | -   | -     | -    | -      | -       | PD     | PD       | -       |
| PR7=1 | -   | -   | -     | -    | -      | -       | -      | -        | PD      |

## 8.14. Reg-2Ah: Tone Control

Default: 0000h

**Table 24. Reg-2Ah: Tone Control**

| Name      | Bits | Read/Write | Reset State | Description                                                             |
|-----------|------|------------|-------------|-------------------------------------------------------------------------|
| Reserved  | 15:1 | R          | 0'h         | Reserved                                                                |
| ac_src_en | 0    | RW         | 0'h         | Enable Variable Rate Audio Control<br>0: Off                      1: On |

## 8.15. Reg-2Ch: AC'97 Stereo DAC Rate/DPE Rate

Default: BB80h

**Table 25. Reg-2Ch: AC'97 Stereo DAC Rate/DPE Rate**

| Name            | Bits | Read/Write | Reset State | Description                     |
|-----------------|------|------------|-------------|---------------------------------|
| dac_sample_rate | 15:0 | RW         | BB80'h      | FOSR[15:0] Output Sampling Rate |

The ALC5611 supports the following PC99/PC2001 design guide sampling rates.

**Table 26. PC99/PC2001 Design Guide Sampling Rates**

| Sampling Rate | FOSR[15:0] |
|---------------|------------|
| 8000          | 1F40h      |
| 11025         | 2B11h      |
| 12000         | 2EE0       |
| 16000         | 3E80h      |
| 22050         | 5622h      |
| 24000         | 5DC0       |
| 32000         | 7D00h      |
| 44100         | AC44h      |
| 48000         | BB80h      |

When ac\_src\_en=0 (VRA is disabled), any non-zero value in this register will be forced to BB80h.

## 8.16. Reg-32h: AC'97 Stereo ADC Rate

Default: BB80h

**Table 27. Reg-32h: AC'97 Stereo ADC Rate**

| Name            | Bits | Read/Write | Reset State | Description                      |
|-----------------|------|------------|-------------|----------------------------------|
| adc_sample_rate | 15:0 | RW         | BB80'h      | IISR[15:0] Output Sampling Rate. |

The ALC5611 supports the following PC99/PC2001 design guide sampling rates.

**Table 28. PC99/PC2001 Design Guide Sampling Rates**

| Sampling Rate | IISR[15:0] |
|---------------|------------|
| 8000          | 1F40h      |
| 11025         | 2B11h      |
| 12000         | 2EE0       |
| 16000         | 3E80h      |
| 22050         | 5622h      |
| 24000         | 5DC0       |
| 32000         | 7D00h      |
| 44100         | AC44h      |
| 48000         | BB80h      |

## 8.17. Reg-3Ah: Power Management Addition 1

Default: 0000h

**Table 29. Reg-3Ah: Power Management Addition 1**

| Name                   | Bits | Read/Write | Reset State | Description                                                                   |
|------------------------|------|------------|-------------|-------------------------------------------------------------------------------|
| depop_MONOoutb         | 15   | RW         | 0'h         | Depop of MONO Out<br>0: Enable (De-pop Enable)<br>1: Disable (De-pop Disable) |
| depop_hp_outb          | 14   | RW         | 0'h         | Depop of HP Out<br>0: Enable (De-pop Enable)<br>1: Disable (De-pop Disable)   |
| pow_zcd                | 13   | RW         | 0'h         | All Zero-Cross Detect Power down<br>0: Disable<br>1: Enable                   |
| ip_en                  | 12   | RW         | 0'h         | Pressure Measurement Source Current Enable<br>0: Disable<br>1: Enable         |
| Pow_zcd_timo_out_en    | 11   | RW         | 0'h         | Zero Cross Time Out Enable<br>0: Disable<br>1: Enable                         |
| Reserved               | 10:6 | RW         | 0'h         | Reserved                                                                      |
| pow_mic1_bias_det_ctrl | 5    | RW         | 0'h         | MICBIAS1 Short Current Detector Control<br>0: Disable<br>1: Enable            |
| pow_mic2_bias_det_ctrl | 4    | RW         | 0'h         | MICBIAS2 Short Current Detector Control<br>0: Disable<br>1: Enable            |
| pow_mic1_bias          | 3    | RW         | 0'h         | 0: Disable<br>1: Enable microphone1 bias                                      |
| pow_mic2_bias          | 2    | RW         | 0'h         | 0: Disable<br>1: Enable microphone2 bias                                      |
| pow_main_bias          | 1    | RW         | 0'h         | 0: Disable<br>1: Enable Main bias of the ALC5611                              |
| pow_dac_ref            | 0    | RW         | 0'h         | 0: Disable<br>1: Enable ALL DAC reference of the ALC5611                      |

## 8.18. Reg-3Ch: Power Management Addition 2

Default: 0000h

**Table 30. Reg-3Ch: Power Management Addition 2**

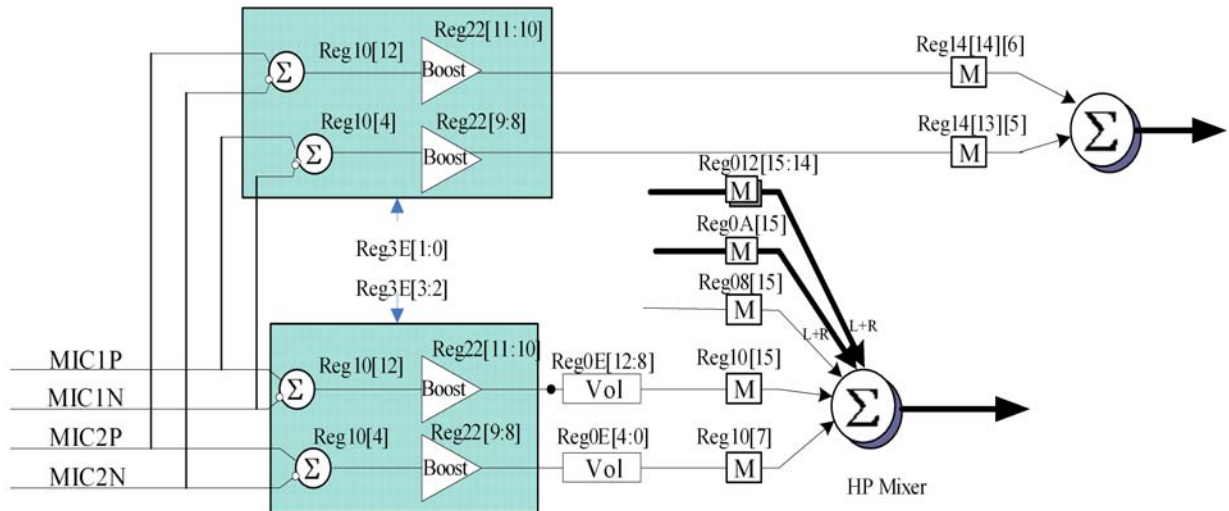
| Name                | Bits | Read/Write | Reset State | Description                                                                               |
|---------------------|------|------------|-------------|-------------------------------------------------------------------------------------------|
| pow_thermal         | 15   | RW         | 0'h         | Thermal Detect (Temp Sensor)<br>0: Disable                      1: Enable                 |
| pow_clsab           | 14   | RW         | 0'h         | Class_AB Power (All)<br>0: Disable                      1: Enable                         |
| pow_vref            | 13   | RW         | 0'h         | VREF of All Analog Circuits<br>0: Disable                      1: Enable                  |
| pow_pll             | 12   | RW         | 0'h         | PLL<br>0: Disable                      1: Enable PLL                                      |
| pow_tp_adc          | 11   | RW         | 0'h         | Touch Panel and AUX_ADC<br>0: Disable                      1: Enable                      |
| Reserved            | 10   | RW         | 0'h         | Reserved                                                                                  |
| pow_dac_l           | 9    | RW         | 0'h         | Left Stereo DAC Filter Clock<br>0: Disable                      1: Enable                 |
| pow_dac_r           | 8    | RW         | 0'h         | Right Stereo DAC Filter Clock<br>0: Disable                      1: Enable                |
| pow_adc_l           | 7    | RW         | 0'h         | Left Stereo ADC Filter Clock and Input Gain<br>0: Disable                      1: Enable  |
| pow_adc_r           | 6    | RW         | 0'h         | Right Stereo ADC Filter Clock and Input Gain<br>0: Disable                      1: Enable |
| pow_hp_l            | 5    | RW         | 0'h         | Left Headphone Mixer<br>0: Disable                      1: Enable                         |
| pow_hp_r            | 4    | RW         | 0'h         | Right Headphone Mixer<br>0: Disable                      1: Enable                        |
| pow_spk_mixer       | 3    | RW         | 0'h         | Speaker Mixer<br>0: Disable                      1: Enable                                |
| pow_MONO_mixer      | 2    | RW         | 0'h         | MONO Mixer<br>0: Disable                      1: Enable                                   |
| pow_adc_rec_l_mixer | 1    | RW         | 0'h         | Left ADC Record Mixer<br>0: Disable                      1: Enable                        |
| pow_adc_rec_r_mixer | 0    | RW         | 0'h         | Right ADC Record Mixer<br>0: Disable                      1: Enable                       |

## 8.19. Reg-3Eh: Power Management Addition 3

Default: 0000h

**Table 31. Reg-3Eh: Power Management Addition 3**

| Name              | Bits | Read/Write | Reset State | Description                                                               |
|-------------------|------|------------|-------------|---------------------------------------------------------------------------|
| Reserved          | 15   | R          | 0'h         | Reserved                                                                  |
| pow_MONO_out_vol  | 14   | RW         | 0'h         | MONO_OUT Volume Control (Amp)<br>0: Disable      1: Enable                |
| pow_spk_outln     | 13   | RW         | 0'h         | SPK_OUTLN Output (Enable Class-AB & Class-D)<br>0: Disable      1: Enable |
| pow_spk_outrn     | 12   | RW         | 0'h         | SPK_OUTRN Output (Enable Class-AB & Class-D)<br>0: Disable      1: Enable |
| pow_hp_l_vol      | 11   | RW         | 0'h         | HP_OUT_L Volume Control (Amp)<br>0: Disable      1: Enable                |
| pow_hp_r_vol      | 10   | RW         | 0'h         | HP_OUT_R Volume Control (Amp)<br>0: Disable      1: Enable                |
| pow_spk_l         | 9    | RW         | 0'h         | SPK_OUT_L Output (Enable Class-AB & Class-D)<br>0: Disable      1: Enable |
| pow_spk_r         | 8    | RW         | 0'h         | SPK_OUT_R Output (Enable Class-AB & Class-D)<br>0: Disable      1: Enable |
| pow_li_l_vol      | 7    | RW         | 0'h         | LINE_IN Left Volume Control<br>0: Disable      1: Enable                  |
| pow_li_r_vol      | 6    | RW         | 0'h         | LINE_IN Right Volume Control<br>0: Disable      1: Enable                 |
| pow_phone_vol     | 5    | RW         | 0'h         | PHONE Volume Control<br>0: Disable      1: Enable                         |
| pow_phone_admixer | 4    | RW         | 0'h         | PHONE AD Mixer<br>0: Disable      1: Enable                               |
| pow_mic1_vol      | 3    | RW         | 0'h         | MIC1 Volume Control<br>0: Disable      1: Enable                          |
| pow_mic2_vol      | 2    | RW         | 0'h         | MIC2 Volume Control<br>0: Disable      1: Enable                          |
| pow_mic1_admixer  | 1    | RW         | 0'h         | MIC1 AD Mixer and Boost<br>0: Disable      1: Enable                      |
| pow_mic2_admixer  | 0    | RW         | 0'h         | MIC2 AD Mixer and Boost<br>0: Disable      1: Enable                      |



**Figure 11. Power Control to MIC Input**

## 8.20. Reg-40h: General Purpose Control Register 1

Default: 0428h

**Table 32. Reg-40h: General Purpose Control Register 1**

| Name           | Bits  | Read/Write | Reset State | Description                                                                                                                                                                                                                                             |
|----------------|-------|------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| sel_sysclk     | 15    | RW         | 0'h         | Clock Source MUX Control<br>0: MCLK                      1: PLL Output                                                                                                                                                                                  |
| Reserved       | 14:10 | RW         | 1'h         | Reserved                                                                                                                                                                                                                                                |
| hp_amp_ctrl    | 9:8   | RW         | 0'h         | Headphone Amplifier $V_{MID}$ Ratio Control (Output Gain Control)<br>00: 1                              01: 1.25<br>1x: 1.5                                                                                                                             |
| spk_ampD_ctrl  | 7:6   | RW         | 0'h         | Speaker Class-D Amplifier $V_{MID}$ Ratio Control (Output Gain Control)<br>00: 1.75 Vdd                      01: 1.5 Vdd<br>10: 1.25 Vdd                      11: 1.0 Vdd                                                                               |
| spk_ampAB_ctrl | 5:3   | RW         | 5'h         | Speaker Class-AB Amplifier $V_{MID}$ Ratio Control (Output Gain Control)<br>000: 2.25 Vdd                      001: 2.00 Vdd<br>010: 1.75 Vdd                      011: 1.5 Vdd<br>100: 1.25 Vdd                      101: 1 Vdd<br>Others: Not allowed |
| Reserved       | 2:0   | RW         | 0'h         | Reserved                                                                                                                                                                                                                                                |

## 8.21. Reg-42h: General Purpose Control Register 2

Default: 0000h

**Table 33. Reg-42h: General Purpose Control Register 2**

| Name         | Bits  | Read/Write | Reset State | Description                                                                                  |
|--------------|-------|------------|-------------|----------------------------------------------------------------------------------------------|
| Reserved     | 15:14 | RW         | 0'h         | Reserved                                                                                     |
| se_btl_clsab | 13    | RW         | 0'b         | Single-Ended & BTL of SPK_Class-AB Selection<br>0: Differential Mode<br>1: Single-ended Mode |
| Reserved     | 12:1  | RW         | 0'h         | Reserved                                                                                     |
| pll_pre_div  | 0     | RW         | 0'b         | PLL Pre-Divider<br>0b: ÷1<br>1b: ÷2                                                          |

## 8.22. Reg-44h: PLL Control

Default: 0000h

**Table 34. Reg-44h: PLL Control**

| Name         | Bits | Read/Write | Reset State | Description                                                                                    |
|--------------|------|------------|-------------|------------------------------------------------------------------------------------------------|
| pll_n_code   | 15:8 | RW         | 00'h        | N[7:0] Code for Analog PLL<br>00000000: Div 2<br>00000001: Div 3<br>.....<br>11111111: Div 257 |
| pll_m_bypass | 7    | RW         | 0'h         | Bypass PLL M<br>0b: No bypass<br>1b: Bypass                                                    |
| pll_k_code   | 6:4  | RW         | 0'h         | K[2:0] Code for Analog PLL<br>000: Div 2<br>001: Div 3<br>.....<br>111: Div 9                  |
| pll_m_code   | 3:0  | RW         | 0'h         | M[3:0] Code for Analog PLL<br>0000: Div 2<br>0001: Div 3<br>.....<br>1111: Div 17              |

Note: The PLL transmit formula is  $F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2))$  {Typical K=2}.

### 8.22.1. AC-Link PLL Clock Setting Table (Unit: MHz)

**Table 35. AC-Link PLL Clock Setting Table (Unit: MHz)**

| MCLK   | N  | M | F <sub>VCO</sub> | K | F <sub>OUT</sub> |
|--------|----|---|------------------|---|------------------|
| 13     | 66 | 7 | 98.222           | 2 | 24.555           |
| 3.6864 | 78 | 1 | 98.304           | 2 | 24.576           |
| 2.048  | 94 | 0 | 98.304           | 2 | 24.576           |
| 4.096  | 70 | 1 | 98.304           | 2 | 24.576           |

*Note: PLL will only be enabled after a warm reset of the AC-Link.*

### 8.23. Reg-4Ch: GPIO Pin Configuration

Default: 2E3Eh

**Table 36. Reg-4Ch: GPIO Pin Configuration**

| Name                | Bits  | Read/Write | Reset State | Description                                                                                    |
|---------------------|-------|------------|-------------|------------------------------------------------------------------------------------------------|
| Reserved            | 15:14 | R          | 00'b        | Reserved                                                                                       |
| pendown_conf        | 13    | RW         | 1'h         | Pen-down Detect Status Source Configuration<br>0: Bypass                      1: Normal        |
| Reserved            | 12    | R          | 0'b         | Reserved                                                                                       |
| over_temp_conf      | 11    | RW         | 1'h         | Over-Temperature Status Source Configuration<br>0: Bypass                      1: Normal       |
| mic1_short_det_conf | 10    | RW         | 1'h         | MICBIAS1 Short Current Status Source Configuration<br>0: Bypass                      1: Normal |
| mic2_short_det_conf | 9     | RW         | 1'h         | MICBIAS2 Short Current Status Source Configuration<br>0: Bypass                      1: Normal |
| Reserved            | 8:6   | R          | 0'h         | Reserved                                                                                       |
| gpio5_conf          | 5     | RW         | 1'h         | GPIO5 Pin Configuration<br>0: Output                      1: Input                             |
| gpio4_conf          | 4     | RW         | 1'h         | GPIO4 Pin Configuration<br>0: Output                      1: Input                             |
| gpio3_conf          | 3     | RW         | 1'h         | GPIO3 Pin Configuration<br>0: Output                      1: Input                             |
| gpio2_conf          | 2     | RW         | 1'h         | GPIO2 Pin Configuration<br>0: Output                      1: Input                             |
| gpio1_conf          | 1     | RW         | 1'h         | GPIO1 Pin Configuration<br>0: Output                      1: Input                             |
| Reserved            | 0     | R          | 0'h         | Reserved. Read as 0                                                                            |

## 8.24. Reg-4Eh: GPIO Pin Polarity

Default: 2E3Eh

**Table 37. Reg-4Eh: GPIO Pin Polarity**

| Name                    | Bits  | Read/Write | Reset State | Description                                                                                 |
|-------------------------|-------|------------|-------------|---------------------------------------------------------------------------------------------|
| Reserved                | 15:14 | R          | 00'b        | Reserved                                                                                    |
| pendown_polarity        | 13    | RW         | 1'h         | Pen-Down Detect Polarity<br>0: Low Active                      1: High Active               |
| Reserved                | 12    | R          | 0'b         | Reserved                                                                                    |
| over_temp_polarity      | 11    | RW         | 1'h         | Over-Temperature Polarity<br>0: Low Active                      1: High Active              |
| mic1_short_det_polarity | 10    | RW         | 1'h         | MICBIAS1 Short Current Detect Polarity<br>0: Low Active                      1: High Active |
| mic2_short_det_polarity | 9     | RW         | 1'h         | MICBIAS2 Short Current Detect Polarity<br>0: Low Active                      1: High Active |
| Reserved                | 8:6   | R          | 0'h         | Reserved. Read as 0                                                                         |
| gpio5_polarity          | 5     | RW         | 1'h         | GPIO Pin Polarity<br>0: Low Active                      1: High Active                      |
| gpio4_polarity          | 4     | RW         | 1'h         | GPIO Pin Polarity<br>0: Low Active                      1: High Active                      |
| gpio3_polarity          | 3     | RW         | 1'h         | GPIO Pin Polarity<br>0: Low Active                      1: High Active                      |
| gpio2_polarity          | 2     | RW         | 1'h         | GPIO Pin Polarity<br>0: Low Active                      1: High Active                      |
| gpio1_polarity          | 1     | RW         | 1'h         | GPIO Pin Polarity<br>0: Low Active                      1: High Active                      |
| Reserved                | 0     | R          | 0'h         | Reserved. Read as 0                                                                         |

## 8.25. Reg-50h: GPIO Pin Sticky

Default: 0000h

**Table 38. Reg-50h: GPIO Pin Sticky**

| Name                     | Bits  | Read/Write | Reset State | Description                                                                                 |
|--------------------------|-------|------------|-------------|---------------------------------------------------------------------------------------------|
| Reserved                 | 15:14 | R          | 00'b        | Reserved                                                                                    |
| pendown_sticky_En        | 13    | RW         | 0'h         | Pen-Down Detect Sticky Enable<br>0: Not sticky                      1: Sticky               |
| Reserved                 | 12    | R          | 0'b         | Reserved                                                                                    |
| over_temp_sticky_En      | 11    | RW         | 0'h         | Over-Temperature Sticky Enable<br>0: Not sticky                      1: Sticky              |
| mic1_short_det_sticky_En | 10    | RW         | 0'h         | MICBIAS1 Short Current Detect Sticky Enable<br>0: Not sticky                      1: Sticky |
| mic2_short_det_sticky_En | 9     | RW         | 0'h         | MICBIAS2 Short Current Detect Sticky Enable<br>0: Not sticky                      1: Sticky |

| Name            | Bits | Read/Write | Reset State | Description                                                             |
|-----------------|------|------------|-------------|-------------------------------------------------------------------------|
| Reserved        | 8:6  | R          | 0'h         | Reserved. Read as 0                                                     |
| gpio5_sticky_En | 5    | RW         | 0'h         | GPIO5 Pin Sticky Enable<br>0: Not sticky                      1: Sticky |
| gpio4_sticky_En | 4    | RW         | 0'h         | GPIO4 Pin Sticky Enable<br>0: Not sticky                      1: Sticky |
| gpio3_sticky_En | 3    | RW         | 0'h         | GPIO3 Pin Sticky Enable<br>0: Not sticky                      1: Sticky |
| gpio2_sticky_En | 2    | RW         | 0'h         | GPIO2 Pin Sticky Enable<br>0: Not sticky                      1: Sticky |
| gpio1_sticky_En | 1    | RW         | 0'h         | GPIO1 Pin Sticky Enable<br>0: Not sticky                      1: Sticky |
| Reserved        | 0    | R          | 0'h         | Reserved. Read as 0                                                     |

## 8.26. Reg-52h: GPIO Pin Wake-Up

Default: 0000h

**Table 39. Reg-52h: GPIO Pin Wake-Up**

| Name                     | Bits  | Read/Write | Reset State | Description                                                                                   |
|--------------------------|-------|------------|-------------|-----------------------------------------------------------------------------------------------|
| Reserved                 | 15:14 | R          | 00'b        | Reserved                                                                                      |
| pendown_wakeup_en        | 13    | RW         | 0'h         | Pen-Down Detect Wake-Up Enable<br>0: No wake-up                      1: Wake Up               |
| Reserved                 | 12    | R          | 0'b         | Reserved                                                                                      |
| over_temp_wakeup_en      | 11    | RW         | 0'h         | Over-Temperature Wake-Up Enable<br>0: No wake-up                      1: Wake Up              |
| mic1_short_det_wakeup_en | 10    | RW         | 0'h         | MICBIAS1 Short Current Detect Wake-Up Enable<br>0: No wake-up                      1: Wake Up |
| mic2_short_det_wakeup_en | 9     | RW         | 0'h         | MICBIAS2 Short Current Detect Wake-Up Enable<br>0: No wake-up                      1: Wake Up |
| Reserved                 | 8:6   | R          | 0'h         | Reserved. Read as 0                                                                           |
| gpio5_wakeup_en          | 5     | RW         | 0'h         | GPIO5 Pin Wake-Up Enable<br>0: No wake-up                      1: Wake Up                     |
| gpio4_wakeup_en          | 4     | RW         | 0'h         | GPIO4 Pin Wake-Up Enable<br>0: No wake-up                      1: Wake Up                     |
| gpio3_wakeup_en          | 3     | RW         | 0'h         | GPIO3 Pin Wake-Up Enable<br>0: No wake-up                      1: Wake Up                     |
| gpio2_wakeup_en          | 2     | RW         | 0'h         | GPIO2 Pin Wake-Up Enable<br>0: No wake-up                      1: Wake Up                     |
| gpio1_wakeup_en          | 1     | RW         | 0'h         | GPIO1 Pin Wake-Up Enable<br>0: No wake-up                      1: Wake Up                     |
| Reserved                 | 0     | R          | 0'h         | Reserved. Read as 0                                                                           |

## 8.27. Reg-54h: GPIO Pin Status

Default: 003Ah

**Table 40. Reg-54h: GPIO Pin Status**

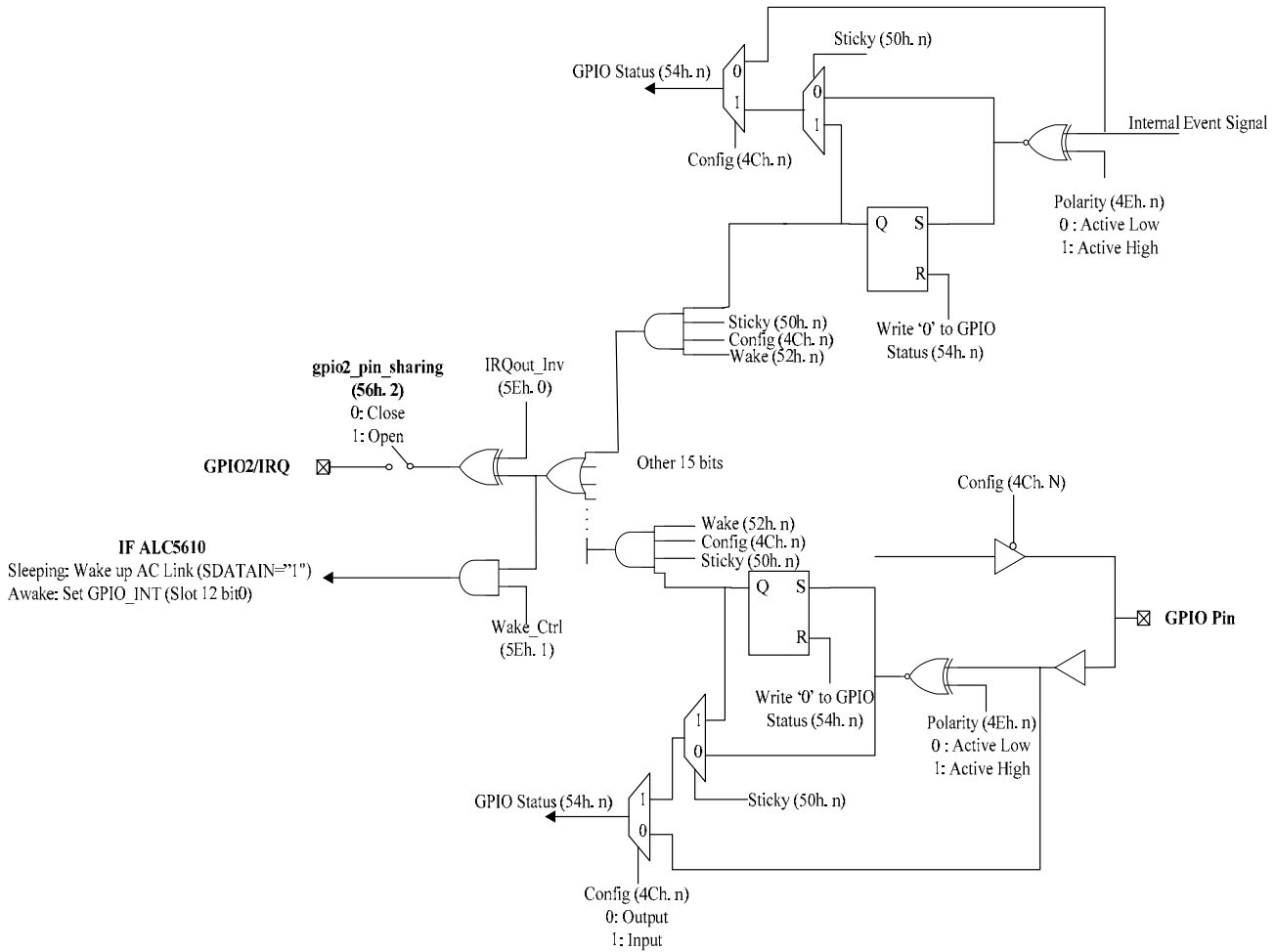
| Name                  | Bits  | Read/Write | Reset State | Description                                                                                             |
|-----------------------|-------|------------|-------------|---------------------------------------------------------------------------------------------------------|
| Reserved              | 15:14 | R          | 00'b        | Reserved                                                                                                |
| pendown_status        | 13    | R          | 0'h         | Pen-Down Detect Status<br>Read: Return status<br>Write: Writing '0' clears the sticky bit               |
| Reserved              | 12    | R          | 0'b         | Reserved                                                                                                |
| over_temp_status      | 11    | R          | 0'h         | Over-Temperature Status<br>Read: Return status<br>Write: Writing '0' clears the sticky bit              |
| mic1_short_det_status | 10    | R          | 0'h         | MICBIAS1 Short Current Detect Status<br>Read: Return status<br>Write: Writing '0' clears the sticky bit |
| mic2_short_det_status | 9     | R          | 0'h         | MICBIAS2 Short Current Detect Status<br>Read: Return status<br>Write: Writing '0' clears the sticky bit |
| Reserved              | 8:6   | R          | 0'h         | Reserved. Read as 0                                                                                     |
| gpio5_status          | 5     | R          | 1'h         | GPIO5 Pin Status<br>Read: Return status of each GPIO pin<br>Write: Writing '0' clears the sticky bit    |
| gpio4_status          | 4     | R          | 1'h         | GPIO4 Pin Status<br>Read: Return status of each GPIO pin<br>Write: Writing '0' clears the sticky bit    |
| gpio3_status          | 3     | R          | 1'h         | GPIO3 Pin Status<br>Read: Return status of each GPIO pin<br>Write: Writing '0' clears the sticky bit    |
| gpio2_status          | 2     | R          | 1'h         | GPIO2 Pin Status<br>Read: Return status of each GPIO pin<br>Write: Writing '0' clears the sticky bit    |
| gpio1_status          | 1     | R          | 1'h         | GPIO1 Pin Status<br>Read: Return status of each GPIO pin<br>Write: Writing '0' clears the sticky bit    |
| Reserved              | 0     | R          | 0'h         | Reserved. Read as 0                                                                                     |

## 8.28. Reg-56h: Pin Sharing

Default: 0000h

**Table 41. Reg-56h: Pin Sharing**

| Name              | Bits | Read/Write | Reset State | Description                                                         |
|-------------------|------|------------|-------------|---------------------------------------------------------------------|
| Reserved          | 15:3 | R          | 0'h         | Reserved                                                            |
| gpio2_pin_sharing | 2    | RW         | 0'h         | GPIO2 Pin Sharing<br>0: IRQ_Out                      1: GPIO enable |
| Reserved          | 1:0  | R          | 0'h         | Reserved                                                            |


**Figure 12. GPIO and IRQ Logic**
**Table 42. GPIO and IRQ Logic**

| GPIO Bit Reg54[15:1] | SLOT 12 Bit | Source   | Description                   |
|----------------------|-------------|----------|-------------------------------|
| 1                    | 5           | GPIO Pin | GPIO1 Input Status            |
| 2                    | 6           | GPIO Pin | GPIO2 Input Status            |
| 3                    | 7           | GPIO Pin | GPIO3                         |
| 4                    | 8           | GPIO Pin | GPIO4                         |
| 5                    | 9           | GPIO Pin | GPIO5                         |
| 6                    | 10          | -        | Unused                        |
| 7                    | 11          | -        | Unused                        |
| 8                    | 12          | -        | Unused                        |
| 9                    | 13          | VGPI0    | MICBIAS2 Short Current Detect |
| 10                   | 14          | VGPI0    | MICBIAS1 Short Current Detect |
| 11                   | 15          | VGPI0    | Over-Temperature              |
| 12                   | 16          | -        | Unused                        |
| 13                   | 17          | VGPI0    | Pen-Down Detect               |
| 14                   | 18          | -        | Unused                        |
| 15                   | 19          | -        | Unused                        |

## 8.29. Reg-58h: Over-Temp/Current Status

Default: 0CFFh

**Table 43. Reg-58h: Over-Temp/Current Status**

| Name                | Bits  | Read/Write | Reset State | Description                                                           |
|---------------------|-------|------------|-------------|-----------------------------------------------------------------------|
| Reserved            | 15:12 | R          | 0000'h      | Reserved                                                              |
| ovt_hp_status       | 11    | R          | 1'h         | Headphone Amp Over-Temperature<br>0: Normal 1: Over-temperature       |
| ovt_MONO_status     | 10    | R          | 1'h         | MONO Amp Over-Temperature<br>0: Normal 1: Over-temperature            |
| ovc_micbias1_status | 9     | R          | 0'h         | MICBIAS1 Over-Current<br>0: Normal 1: Over-current                    |
| ovc_micbias2_status | 8     | R          | 0'h         | MICBIAS2 Over-Current<br>0: Normal 1: Over-current                    |
| rp_depopped_status  | 7     | R          | 1'h         | RP Channel Depop Status<br>0: Depop ready 1: Depop finished           |
| rn_depopped_status  | 6     | R          | 1'h         | RN Channel Depop Status<br>0: Depop ready 1: Depop finished           |
| lp_depopped_status  | 5     | R          | 1'h         | LP Channel Depop Status<br>0: Depop ready 1: Depop finished           |
| ln_depopped_status  | 4     | R          | 1'h         | LN Channel Depop Status<br>0: Depop ready 1: Depop finished           |
| ovt_rp_status       | 3     | R          | 1'h         | RP Channel Temperature Sensor Status<br>0: Normal 1: Over-temperature |
| ovt_rn_status       | 2     | R          | 1'h         | RN Channel Temperature Sensor Status<br>0: Normal 1: Over-temperature |
| ovt_lp_status       | 1     | R          | 1'h         | LP Channel Temperature Sensor Status<br>0: Normal 1: Over-temperature |
| ovt_ln_status       | 0     | R          | 1'h         | LN Channel Temperature Sensor Status<br>0: Normal 1: Over-temperature |

## 8.30. Reg-5Ch: GPIO\_Output Pin Control

Default: 0000h

**Table 44. Reg-5Ch: GPIO\_Output Pin Control**

| Name             | Bits | Read/Write | Reset State | Description                                              |
|------------------|------|------------|-------------|----------------------------------------------------------|
| Reserved         | 15:6 | R          | 0000'h      | Reserved                                                 |
| gpio5_out_status | 5    | RW         | 0'h         | GPIO5 Output Pin Control<br>0b: Drive Low 1b: Drive High |
| gpio4_out_status | 4    | RW         | 0'h         | GPIO4 Output Pin Control<br>0b: Drive Low 1b: Drive High |
| gpio3_out_status | 3    | RW         | 0'h         | GPIO3 Output Pin Control<br>0b: Drive Low 1b: Drive High |
| gpio2_out_status | 2    | RW         | 0'h         | GPIO2 Output Pin Control<br>0b: Drive Low 1b: Drive High |
| gpio1_out_status | 1    | RW         | 0'h         | GPIO1 Output Pin Control<br>0b: Drive Low 1b: Drive High |
| Reserved         | 0    | R          | 0'h         | Reserved. Read as 0                                      |

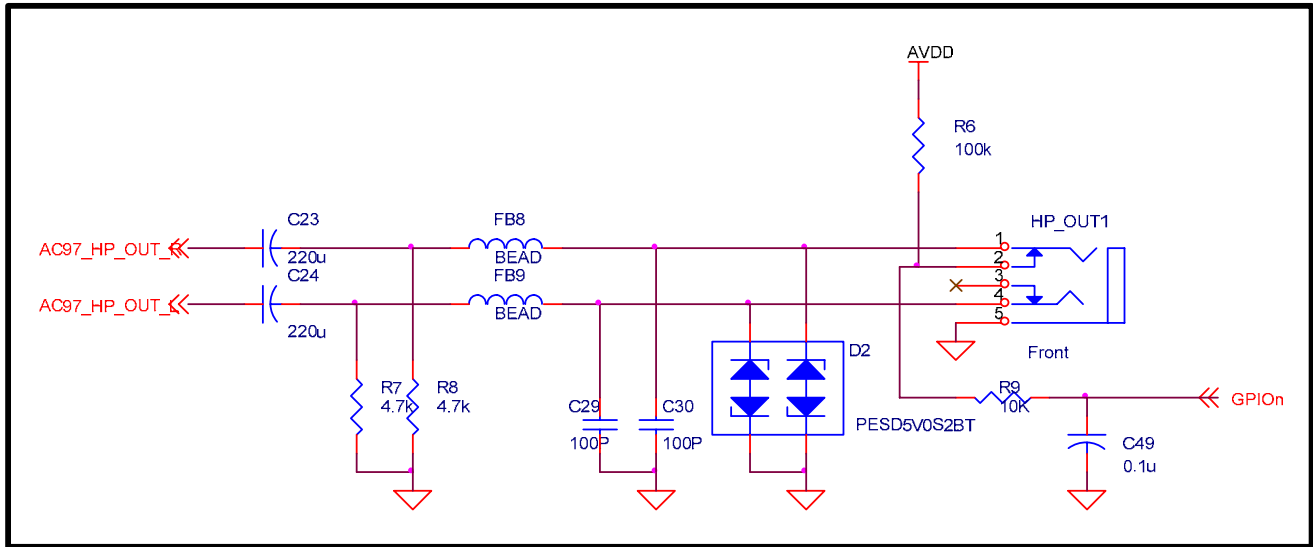
### 8.31. Reg-5Eh: MISC Control

Default: 0000h

**Table 45. Reg-5Eh: MISC Control**

| Name                | Bits  | Read/Write | Reset State | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------------------|-------|------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| en_vref_fast        | 15    | RW         | 0'b         | Enable Fast Vref<br>0: Enable fast Vref<br>1: Disable fast Vref<br><i>Note: To improve PSRR, en_vref_fast should be disabled before playback/record.</i>                                                                                                                                                                                                                                                                                                                                                                                                           |
| clsab_amp_sel       | 14    | RW         | 0'b         | Class-AB Output Amplifier Select<br>0: Strong Amp<br>1: Weak Amp<br><i>Note: Strong Amp, SPKVDD: 3.0V~5V and Set index44[8:6]=100'b.<br/>Weak Amp, SPKVDD: 2.3V~5V and set index44[8:6]=000'b.</i>                                                                                                                                                                                                                                                                                                                                                                 |
| AVC_target_sel      | 13:12 | RW         | 0'b         | AVC Target Select<br>00: Reserved (No AVC)      01: R Channel<br>10: L Channel                11: Both channel                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| thermal_shutdown_en | 11    | RW         | 0'b         | Thermal Shutdown Enable<br>0: Disable                      1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| reset_pendown_sel   | 10    | RW         | 0'b         | Reset/Pen-Down Selection<br>0: Reset Input<br>1: Pen-down Output<br><i>Note: Output Reg78[15] status as pen-down signal when Reset_Pendown_sel=1.<br/>Sequence:<br/>1. Set the GPIO of the controller as output and set the ALC5611 as Reset_Input.<br/>2. After Reset, Set the GPIO of the controller as Input and set the ALC5611 as Pendown_Output.<br/>3. Enable the GPIO of the controller to receive INT.<br/>4. After the controller Received INT, the controller disables INT and starts to check AUXADC.<br/>5. Pen-up will be reported by Reg78[15].</i> |
| Reserved            | 9:7   | RW         | 0'h         | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| main_dac_l_mute     | 6     | RW         | 0'h         | Mute Main DAC Left Input<br>0: On                              1: Mute (-∞dB)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| main_dac_r_mute     | 5     | RW         | 0'h         | Mute Main DAC Right Input<br>0: On                              1: Mute (-∞dB)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Reserved            | 4:2   | RW         | 0'h         | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| gpio_wakeup_ctrl    | 1     | RW         | 0'h         | GPIO wakeup Control<br>0: Disable                      1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| irqout_inv_ctrl     | 0     | RW         | 0'h         | IRQOUT Inverter Control<br>0: Normal                      1: Invert                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

The Jack-insert-detect pull up resistor is implemented via an external circuit (see Figure 13, below).



**Figure 13. Jack-Insert-Detect Pull Up Resistor Implemented via an External Circuit**

## 8.32. Reg-68h: Pseudo Stereo and Spatial Effect Block Control

Default: 0053h

**Table 46. Reg-68h: Pseudo Stereo and Spatial Effect Block Control**

| Name                | Bits | Read/Write | Reset State | Description                                                                                                                                                |
|---------------------|------|------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| spatial_ctrl_enable | 15   | RW         | 0'b         | Spatial Enable<br>0b: Disable (Clear internal state)<br>1b: Enable                                                                                         |
| apf_en              | 14   | RW         | 0'h         | Enable All Pass Filter APF(z) (EN-APF)<br>0: Disable (Bypass) and reset.<br>1: Enable all pass filters. The coefficient a1 is loaded from apf_parm_a1[7:0] |
| pseudo_stereo_en    | 13   | RW         | 0'h         | Enable Pseudo Stereo Block (EN-PSB)<br>0: Disabled<br>1: Enabled                                                                                           |
| en_3d               | 12   | RW         | 0'h         | Enable Stereo Expansion Block (EN-SEB)<br>0: Disable<br>1: Enabled. Load 3D Ratio from ratio_parm_3d and 3D Gain from gain_parm_3d                         |
| Reserved            | 11:8 | -          | 0'h         | Reserved                                                                                                                                                   |
| gain_parm_3d        | 7:6  | RW         | 1'h         | 3D Gain Parameter (SEGn)<br>00: Gain=1.0                      01: Gain=1.5<br>10: Gain=2.0                      11: Reserved                               |

| Name          | Bits | Read/Write | Reset State | Description                                                                                                                                                     |
|---------------|------|------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ratio_parm_3d | 5:4  | RW         | 1'h         | 3D Ratio Parameter (DPn)<br>00: Ratio=0.0                      01: Ratio=0.66<br>10: Ratio=1.0                      11: Reserved                                |
| Reserved      | 3:2  | -          | 0'h         | Reserved                                                                                                                                                        |
| apf_parm_a1   | 1:0  | RW         | 3'h         | All Pass Filter Parameter<br>00: Disable<br>01: Enable for 32kHz sample rate or lower<br>10: Enable for 44.1kHz sample rate<br>11: Enable for 48kHz sample rate |

*Note: Writes to SEGn and DPn will be ignored when the Spatial effect control bit is enabled. This means individual Spatial coefficients cannot be modified when Spatial is enabled.*

### 8.33. Reg-6Ah: Index Address

Default: 0000h

**Table 47. Reg-6Ah: Index Address**

| Name       | Bits | Read/Write | Reset State | Description   |
|------------|------|------------|-------------|---------------|
| Reserved   | 15:7 | R          | 0'h         | Reserved      |
| index_addr | 6:0  | RW         | 0'h         | Index Address |

### 8.34. Reg-6Ch: Index Data

Default: 0000h

**Table 48. Reg-6Ch: Index Data**

| Name       | Bits | Read/Write | Reset State | Description |
|------------|------|------------|-------------|-------------|
| index_data | 15:0 | RW         | 0'h         | Index Data  |



### 8.38. Index-02h: EQ Band-1 Coefficient (BP1: a1)

Default: 0000h

**Table 52. Index-02h: EQ Band-1 Coefficient (BP1: a1)**

| Bit  | Type | Function                                                                                 |
|------|------|------------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a1 should be in -2 ~ 1.99) |

### 8.39. Index-03h: EQ Band-1 Coefficient (BP1: a2)

Default: 0000h

**Table 53. Index-03h: EQ Band-1 Coefficient (BP1: a2)**

| Bit  | Type | Function                                                                                 |
|------|------|------------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a1 should be in -2 ~ 1.99) |

### 8.40. Index-04h: EQ Band-1 Gain (BP1: Ho)

Default: 0000h

**Table 54. Index-04h: EQ Band-1 Gain (BP1: Ho)**

| Bit  | Type | Function                                                                                 |
|------|------|------------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the Ho should be in -4 ~ 3.99) |

### 8.41. Index-05h: EQ Band-2 Coefficient (BP2: a1)

Default: 0000h

**Table 55. Index-05h: EQ Band-2 Coefficient (BP2: a1)**

| Bit  | Type | Function                                                                                 |
|------|------|------------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a1 should be in -2 ~ 1.99) |

### 8.42. Index-06h: EQ Band-2 Coefficient (BP2: a2)

Default: 0000h

**Table 56. Index-06h: EQ Band-2 Coefficient (BP2: a2)**

| Bit  | Type | Function                                                                                 |
|------|------|------------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a2 should be in -2 ~ 1.99) |

### 8.43. Index-07h: EQ Band-2 Gain (BP2: Ho)

Default: 0000h

**Table 57. Index-07h: EQ Band-2 Gain (BP2: Ho)**

| Bit  | Type | Function                                                                                 |
|------|------|------------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the Ho should be in -4 ~ 3.99) |

### 8.44. Index-08h: EQ Band-3 Coefficient (BP3: a1)

Default: 0000h

**Table 58. Index-08h: EQ Band-3 Coefficient (BP3: a1)**

| Bit  | Type | Function                                                                                 |
|------|------|------------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a1 should be in -2 ~ 1.99) |

### 8.45. Index-09h: EQ Band-3 Coefficient (BP3: a2)

Default: 0000h

**Table 59. Index-09h: EQ Band-3 Coefficient (BP3: a2)**

| Bit  | Type | Function                                                                                 |
|------|------|------------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a2 should be in -2 ~ 1.99) |

### 8.46. Index-0Ah: EQ Band-3 Gain (BP3: Ho)

Default: 0000h

**Table 60. Index-0Ah: EQ Band-3 Gain (BP3: Ho)**

| Bit  | Type | Function                                                                                 |
|------|------|------------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the Ho should be in -4 ~ 3.99) |

### 8.47. Index-0Bh: EQ Band-4 Coefficient (HPF: a1)

Default: 0000h

**Table 61. Index-0Bh: EQ Band-4 Coefficient (HPF: a1)**

| Bit  | Type | Function                                                                                 |
|------|------|------------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a1 should be in -2 ~ 1.99) |



## 8.51. Index-12h: EQ Output Volume Control

Default: 0001h

**Table 65. Index-12h: EQ Output Volume Control**

| Bit  | Type | Function                                                                                                                                             |
|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:3 | -    | Reserved                                                                                                                                             |
| 2:0  | RW   | 7-Bit Volume Unsigned Ratio EQOut-VOL-LR<br>000b: -3dB<br>010b: 3dB<br>100b: 9dB<br>110b: 15dB<br>001b: 0dB<br>011b: 6dB<br>101b: 12dB<br>111b: 18dB |

## 8.52. Index-20h: Auto Volume Control Register 0

Default: 0050h

**Table 66. Index-20h: Auto Volume Control Register 0**

| Bit  | Type | Function                                                                                                                                                                                                                                                                                                                                 |
|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RW   | Select the Controlled Gain Block for AVC (Default: 00b)<br>0: Disable AVC<br>1: Enable AVC to control ADC gain                                                                                                                                                                                                                           |
| 14:8 | -    | Reserved                                                                                                                                                                                                                                                                                                                                 |
| 7:3  | RW   | Monitor Window Control (Unit: $2^{(n+1)}$ samples) (Default: 01010b)<br>00000b: $2^{(1)}$ sample<br>00001b: $2^{(2)}$ samples<br>00010b: $2^{(3)}$ samples<br>...<br>10000b: $2^{(17)}$ samples<br>...<br>Others: Reserved.<br>Maximum n=16<br><i>Note: The Monitor Window can only be changed after soft-reset when AVC is enabled.</i> |
| 2:1  | -    | Reserved                                                                                                                                                                                                                                                                                                                                 |
| 0    | RW   | AVC Reference Channel Selection (Default: 0b)<br>0: Left Channel<br>1: Right Channel                                                                                                                                                                                                                                                     |

### 8.53. Index-21h: Auto Volume Control Register 1

Default: 2710h

**Table 67. Index-21h: Auto Volume Control Register 1**

| Bit  | Type | Function                                                                                |
|------|------|-----------------------------------------------------------------------------------------|
| 15   | -    | Reserved                                                                                |
| 14:0 | RW   | The Maximum internal PCM data absolute level after AVC, Thmax (=0 ~ 2 <sup>15</sup> -1) |

### 8.54. Index-22h: Auto Volume Control Register 2

Default: 0BB8h

**Table 68. Index-22h: Auto Volume Control Register 2**

| Bit  | Type | Function                                                                                |
|------|------|-----------------------------------------------------------------------------------------|
| 15   | -    | Reserved                                                                                |
| 14:0 | RW   | The Minimum internal PCM data absolute level after AVC, Thmin (=0 ~ 2 <sup>15</sup> -1) |

### 8.55. Index-23h: Auto Volume Control Register 3

Default: 01F4h

**Table 69. Index-23h: Auto Volume Control Register 3**

| Bit  | Type | Function                                                                                                           |
|------|------|--------------------------------------------------------------------------------------------------------------------|
| 15   | -    | Reserved                                                                                                           |
| 14:0 | RW   | The Non-active internal PCM data absolute level AVC will keep analog unit gain, Thnonact (=0 ~ 2 <sup>15</sup> -1) |

*Note: Initial Index23=0001'h.*

### 8.56. Index-24h: Auto Volume Control Register 4

Default: 0190h

**Table 70. Index-24h: Auto Volume Control Register 4**

| Bit  | Type | Function                                                                                                                                            |
|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RW   | The CNTMAXTH1 to control the sensitivity to increase Gain (Unit:2 <sup>1</sup> )<br>This value should be less than CNTMAXTH2 (Max:2 <sup>17</sup> ) |

## 8.57. Index-25h: Auto Volume Control Register 5

Default: 0200h

**Table 71. Index-25h: Auto Volume Control Register 5**

| Bit  | Type | Function                                                                                                                                                                                    |
|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RW   | The CNTMAXTH2 to control the sensitivity to decrease Gain (Unit:2 <sup>1</sup> )<br>This value should be less than Monitor Window (Optimized: 1/2 Monitor Window)<br>(Max:2 <sup>17</sup> ) |

Note: CNTMAXTH1 < CNTMAXTH2.

## 8.58. Index-39h: Digital Internal Register

Default: 9000h

**Table 72. Index-39h: Digital Internal Register**

| Bit  | Type | Function                                                   |
|------|------|------------------------------------------------------------|
| 15   | RW   | Pad Drive Capability<br>0b: Weak drive<br>1b: Strong drive |
| 14:0 | RW   | Reserved                                                   |

## 8.59. Index-4Ah: Class-D Temperature Sensor

Default: 4444h

**Table 73. Index-4Ah: Class-D Temperature Sensor**

| Bit   | Type | Function                                                                                             |
|-------|------|------------------------------------------------------------------------------------------------------|
| 15    | RW   | Reserved                                                                                             |
| 14:12 | RW   | RP Channel Temp. Sensor Threshold Setting<br>001: 35°C      011: 65°C      101: 95°C      111: 125°C |
| 11    | RW   | Reserved                                                                                             |
| 10:8  | RW   | RN Channel Temp. Sensor Threshold Setting<br>001: 35°C      011: 65°C      101: 95°C      111: 125°C |
| 7     | RW   | Reserved                                                                                             |
| 6:4   | RW   | LP Channel Temp. Sensor Threshold Setting<br>001: 35°C      011: 65°C      101: 95°C      111: 125°C |
| 3     | RW   | Reserved                                                                                             |
| 2:0   | RW   | LN Channel Temp. Sensor Threshold Setting<br>001: 35°C      011: 65°C      101: 95°C      111: 125°C |

Note: Tolerance: ± 15 °C.



| Name                | Bits | Read/Write | Reset State | Description                                                                                                                                                |
|---------------------|------|------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| tp_slot_sel         | 5    | RW         | 0'h         | AC'97 Slot Select<br>0: Slot 5                      1: Slot 6                                                                                              |
| tp_clk_div          | 4:2  | RW         | 3'h         | AUX ADC Clock Divider<br>000~010: Reserved<br>011: ÷64 (Default)          100: ÷80<br>101: ÷96                      110: ÷112<br>111: ÷128                 |
| conversion_rate_sel | 1:0  | RW         | 0'h         | Conversion Rate Select for No Delay Setting<br>00: 93.75Hz (512 frames)<br>01: 124.67Hz (384 frames)<br>10: 187.5Hz (256 frames)<br>11: 374Hz (128 frames) |

### 8.62. Reg-76h: Touch Panel Control Byte 2

Default: 3F00h

**Table 76. Reg-76h: Touch Panel Control Byte 2**

| Name                   | Bits | Read/Write | Reset State | Description                                                                                                                                    |
|------------------------|------|------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| polling_trig           | 15   | RW         | 0'h         | Writing 1 initiates a measurement in polling mode. This bit will self-clear when measured data is received                                     |
| tp_adc_mode_sel        | 14   | RW         | 0'h         | Touch Panel ADC Data Mode Select During Position Measurement<br>0: Polling mode<br>1: Continuous mode                                          |
| pd_pullup_resistor_sel | 13:8 | RW         | 3F'h        | Programmable Internal Pull-Up Resistor For Pen-down Detection<br>000000: 1K Ohm<br>000001: 2K Ohm<br>000010: 3K Ohm<br>.....<br>111111: 64KOhm |
| AUX_measure_en         | 7    | RW         | 0'h         | AUX Measurement<br>0: Disable                      1: Enable                                                                                   |
| Reserved               | 6:4  | R          | 0'h         | Reserved                                                                                                                                       |
| pressure_measure_en    | 3    | RW         | 0'h         | Pressure Measurement<br>0: Disable                      1: Enable                                                                              |
| y_measure_en           | 2    | RW         | 0'h         | Y Co-Ordinate Measurement<br>0: Disable                      1: Enable                                                                         |
| x_measure_en           | 1    | RW         | 0'h         | X Co-Ordinate Measurement<br>0: Disable                      1: Enable                                                                         |
| AUX_measure_sel        | 0    | RW         | 0'h         | AUX3/AUX4 Measure Selection<br>0: AUX4                        1: AUX3                                                                          |

### 8.63. Reg-78h: Touch Panel Indication

Default: 0000h

**Table 77. Reg-78h: Touch Panel Indication**

| Name            | Bits  | Read/Write | Reset State | Description                                                                                                                                                                                                   |
|-----------------|-------|------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| pen_status      | 15    | R          | 0'h         | Indicates Pen Status after AUX_ADC Measured<br>0: Pen-up<br>1: Pen-down                                                                                                                                       |
| pipe_adc_source | 14:12 | R          | 0'h         | AUX ADC Source<br>000: No Data (AUX_ADC Busy)<br>001: X co-ordinate measurement<br>010: Y co-ordinate measurement<br>011: Pressure measurement<br>100: Reserved<br>101: Reserved<br>110: Reserved<br>111: AUX |
| pipe_adc_rpt    | 11:0  | R          | 0'h         | AUX ADC Data Report                                                                                                                                                                                           |

### 8.64. Reg-7Ch: VENDOR ID 1

Default: 10ECh

**Table 78. Reg-7Ch: VENDOR ID 1**

| Name       | Bits | Read/Write | Reset State | Description    |
|------------|------|------------|-------------|----------------|
| vender_id1 | 15:0 | R          | 10EC'h      | Vendor ID=10EC |

### 8.65. Reg-7Eh: VENDOR ID 2

Default: 1003h

**Table 79. Reg-7Eh: VENDOR ID 2**

| Name       | Bits | Read/Write | Reset State | Description   |
|------------|------|------------|-------------|---------------|
| vender_id  | 15:8 | R          | 10'h        | Device ID=10  |
| device_id2 | 7:0  | R          | 03'h        | Version ID=03 |

## 9. Electrical Characteristics

### 9.1. DC Characteristics

#### 9.1.1. Absolute Maximum Ratings

**Table 80. Absolute Maximum Ratings**

| Parameter                     | Symbol | Min  | Typ | Max            | Units |
|-------------------------------|--------|------|-----|----------------|-------|
| Power Supplies                |        |      |     |                |       |
| Digital IO Buffer             | DVDD1  | -0.3 | -   | 3.63           | V     |
| Digital Core                  | DVDD2  | -0.3 | -   | 3.63           | V     |
| Analog                        | AVDD   | -0.3 | -   | 3.63           | V     |
| Touch Panel                   | TPVDD  | -0.3 | -   | 3.63           | V     |
| Headphone                     | HPVDD  | -0.3 | -   | 3.63           | V     |
| Speaker                       | SPKVDD | -0.3 | -   | 7 <sup>1</sup> | V     |
| Operating Ambient Temperature | Ta     | -25  | -   | +85            | °C    |
| Storage Temperature           | Ts     | -55  | -   | +125           | °C    |

Note 1: SPKVDD=5V with 3.5% duty cycle Power bouncing up to SPKVDD=8V is acceptable.

#### 9.1.2. Recommended Operating Conditions

**Table 81. Recommended Operating Conditions**

| Parameter         | Symbol              | Min | Typ | Max | Units |
|-------------------|---------------------|-----|-----|-----|-------|
| Digital IO Buffer | DVDD1               | 1.8 | 3.3 | 3.6 | V     |
| Digital Core      | DVDD2               | 1.8 | 3.3 | 3.6 | V     |
| Analog            | AVDD                | 2.3 | 3.3 | 3.6 | V     |
| Touch Panel       | TPVDD               | 2.3 | 3.3 | 3.6 | V     |
| Headphone         | HPVDD               | 2.3 | 3.3 | 3.6 | V     |
| Speaker           | SPKVDD <sup>1</sup> | 2.3 | 3.3 | 5   | V     |

Note 1: A 10μF Capacitor must be connected from SPKVDD to SPKGND, and should be placed as close as possible to the SPKVDD pin of the ALC5611.

#### 9.1.3. Static Characteristics

**Table 82. Static Characteristics**

| Parameter                                       | Symbol          | Min      | Typ | Max       | Units |
|-------------------------------------------------|-----------------|----------|-----|-----------|-------|
| Input Voltage Range                             | V <sub>IN</sub> | -0.30    | -   | DVDD+0.30 | V     |
| Low Level Input Voltage                         | V <sub>IL</sub> | -        | -   | 0.35DVDD  | V     |
| High Level Input Voltage                        | V <sub>IH</sub> | 0.65DVDD | -   | -         | V     |
| High Level Output Voltage                       | V <sub>OH</sub> | 0.9DVDD  | -   | -         | V     |
| Low Level Output Voltage                        | V <sub>OL</sub> | -        | -   | 0.1DVDD   | V     |
| Input Leakage Current                           | -               | -1       | -   | 1         | μA    |
| Output Leakage Current (Hi-Z)                   | -               | -1       | -   | 1         | μA    |
| Output Buffer High Drive Current                | -               | -        | 22  | -         | mA    |
| Output Buffer Low Drive Current                 | -               | -        | 10  | -         | mA    |
| V <sub>MID</sub> Internal Serial Resistor       | -               | 25       | 50  | 75        | KΩ    |
| V <sub>MID</sub> Internal Serial Resistor Ratio | -               | 95       | 100 | 105       | %     |

Note: DVDD=3.3V, T<sub>ambient</sub>=25 °C, with 50pF external load.

## 9.2. Analog Performance Characteristics

**Table 83. Analog Performance Characteristics**

| Parameter                                                                         | Min  | Typ | Max  | Units      |
|-----------------------------------------------------------------------------------|------|-----|------|------------|
| Full Scale Input Voltage                                                          |      |     |      |            |
| Line Inputs                                                                       | -    | 1.0 | -    | Vrms       |
| MIC Inputs (Non-Boost)                                                            | -    | 1.0 | -    | Vrms       |
| MIC Inputs (Boost 20dB)                                                           | -    | 0.1 | -    | Vrms       |
| ADC                                                                               | -    | 0.7 | -    | Vrms       |
| Full Scale Output Voltage                                                         |      |     |      |            |
| MONO Outputs                                                                      | -    | 1.0 | -    | Vrms       |
| Headphone Amplifiers Outputs                                                      | -    | 1.0 | -    | Vrms       |
| Speaker Amplifiers Outputs                                                        | -    | 1.3 | -    | Vrms       |
| S/N Ratio<br>(A-weighted, HPL/R or MONO with 10K $\Omega$ /50pF Load)             |      |     |      |            |
| STEREO DAC                                                                        | -    | 90  | -    | dB         |
| STEREO ADC                                                                        | -    | 85  | -    | dB         |
| Total Harmonic Distortion + Noise<br>(HPL/R or MONO with 10K $\Omega$ /50pF Load) |      |     |      |            |
| STEREO DAC                                                                        | -    | -85 | -    | dB         |
| STEREO ADC                                                                        | -    | -80 | -    | dB         |
| MIC Boost Amplifier                                                               |      |     |      |            |
| Gain=20dB                                                                         | 18   | 20  | 22   | dB         |
| Gain=30dB                                                                         | -    | 30  | -    | dB         |
| Gain=40dB                                                                         | -    | 40  | -    | dB         |
| Input Impedance (Gain=0dB, ADC Mixer=On/Off)                                      |      |     |      |            |
| PHONEN (Differential Mode)                                                        | -    | 16  | -    | K $\Omega$ |
| MIC1N, MIC2N (Differential Mode)                                                  | -    | 16  | -    | K $\Omega$ |
| MIC1P, MIC2P                                                                      | -    | 16  | -    | K $\Omega$ |
| PHONEP                                                                            | -    | 16  | -    | K $\Omega$ |
| Input Impedance (Gain=0dB, ADC Mixer=On)                                          |      |     |      |            |
| LINE_IN                                                                           | 12.8 | 16  | 19.2 | K $\Omega$ |
| Input Impedance (Gain=0dB, ADC Mixer=Off)                                         |      |     |      |            |
| LINE_IN                                                                           | 25.6 | 32  | 38.4 | K $\Omega$ |
| Output Impedance                                                                  |      |     |      |            |
| MONO_OUT                                                                          | -    | 2   | -    | $\Omega$   |
| HP_OUT                                                                            | -    | 2   | -    | $\Omega$   |
| SPK_OUT (Class-AB)                                                                | -    | 1   | -    | $\Omega$   |
| SPK_OUT (Class-D)                                                                 | -    | 0.3 | 0.4  | $\Omega$   |
| MONO_OUT Amplifier Output Power (32 $\Omega$ Load)                                |      |     |      |            |
| Single-Ended Mode                                                                 | 25   | -   | -    | mW         |
| BTL Mode                                                                          | 75   | -   | -    | mW         |
| MONO_OUT Amplifier Quiescent Current (32 $\Omega$ load)/CH                        | -    | 700 | -    | $\mu$ A    |
| MONO_OUT Amplifier Efficiency ( $f_N$ =1kHz, 32 $\Omega$ Load)                    |      |     |      |            |
| Single-Ended Mode (Output Power=25mW)                                             | 50   | -   | -    | %          |
| BTL Mode (Output Power=75mW)                                                      | 50   | -   | -    | %          |

| Parameter                                                                                  | Min | Typ  | Max   | Units   |
|--------------------------------------------------------------------------------------------|-----|------|-------|---------|
| MONO_OUT Amplifier THD+N<br>Single-Ended Mode (10K $\Omega$ Load)<br>Output Power=0.1mW    | -   | 0.01 | -     | %       |
| BTL Mode (10K $\Omega$ Load)<br>Output Power=0.1mW                                         | -   | 0.01 | -     | %       |
| MONO_OUT Amplifier PSRR                                                                    | -   | 60   | -     | dB      |
| Headphone Amplifier Output Power (32 $\Omega$ Load)                                        | -   | -    | 31.25 | mW      |
| Headphone Amplifier Quiescent Current (32 $\Omega$ Load)                                   | -   | 700  | -     | $\mu$ A |
| Headphone Amplifier Efficiency<br>( $f_{IN}$ =1kHz, 32 $\Omega$ Load, Output Power=25mW)   | 50  | -    | -     | %       |
| Headphone Amplifier THD+N (32 $\Omega$ Load)<br>Output Power=20mW                          | -   | -70  | -     | dB      |
| Output Power=25mW                                                                          | -   | -70  | -     | dB      |
| Headphone Amplifier PSRR                                                                   | -   | 68   | -     | dB      |
| Class-D BTL Speaker Amplifier Output Power<br>(SPKVDD=5V with 8 $\Omega$ Load, 1% THD+N)   | -   | 1    | -     | W       |
| (SPKVDD=5V with 8 $\Omega$ Load, 10% THD+N)                                                | -   | 1.2  | -     | W       |
| (SPKVDD=5V with 4 $\Omega$ Load, 1% THD+N)                                                 | -   | 1.4  | -     | W       |
| (SPKVDD=5V with 4 $\Omega$ Load, 10% THD+N)                                                | -   | 1.7  | -     | W       |
| Class-D BTL Speaker Amplifier Output Power<br>(SPKVDD=4.2V with 8 $\Omega$ Load, 1% THD+N) | -   | 0.7  | -     | W       |
| (SPKVDD=4.2V with 8 $\Omega$ Load, 10% THD+N)                                              | -   | 0.9  | -     | W       |
| (SPKVDD=4.2V with 4 $\Omega$ Load, 1% THD+N)                                               | -   | 1    | -     | W       |
| (SPKVDD=4.2V with 4 $\Omega$ Load, 10% THD+N)                                              | -   | 1.2  | -     | W       |
| BTL Speaker Amplifier Quiescent Current<br>(8 $\Omega$ Load, SPKVDD=3.7V)                  |     |      |       |         |
| Class-AB_Strong                                                                            | -   | 7    | -     | mA      |
| Class-D                                                                                    | -   | 4    | -     | mA      |
| BTL Speaker Amplifier Efficiency<br>( $f_{IN}$ =1kHz, 8 $\Omega$ Load, Output Power=700mW) |     |      |       |         |
| Class-AB                                                                                   | 50  | -    | -     | %       |
| Class-D                                                                                    | -   | 82   | -     | %       |
| BTL Speaker Amplifier THD+N (8 $\Omega$ Load, SPKVDD=5V)                                   |     |      |       |         |
| Class-AB_Strong                                                                            |     |      |       |         |
| Output Power=350mW                                                                         | -   | -70  | -     | dB      |
| Output Power=600mW                                                                         | -   | -70  | -     | dB      |
| Class-D                                                                                    |     |      |       |         |
| Output Power=350mW                                                                         | -   | -70  | -     | dB      |
| Output Power=600mW                                                                         | -   | -60  | -     | dB      |
| BTL Speaker Amplifier THD+N<br>Class-AB_Weak (10K $\Omega$ /50pF Load)                     | -   | -85  | -     | dB      |
| BTL Speaker Amplifier SNR (A-Weighted)<br>Class-AB_Weak (10K $\Omega$ /50pF Load)          | -   | 90   | -     | dB      |
| BTL Speaker Amplifier PSRR                                                                 | -   | 65   | -     | dB      |

| Parameter                                                | Min | Typ   | Max | Units |
|----------------------------------------------------------|-----|-------|-----|-------|
| Quiescent Playback Current (DAC to HP_OUT with 16Ω Load) | -   | 7.4   | -   | mA    |
| Quiescent Record Current (LINE_IN to ADC)                | -   | 11.3  | -   | mA    |
| Power Down Current                                       |     |       |     |       |
| I <sub>DDA</sub> (Analog Block)                          | -   | -     | 10  | μA    |
| I <sub>DDD</sub> (Digital Block)                         | -   | -     | 1   | μA    |
| MICBIAS1 Output Voltage                                  |     |       |     |       |
| 0.75*AVDD Setting                                        | -   | 2.475 | -   | V     |
| 0.9*AVDD Setting                                         | -   | 2.97  | -   | V     |
| MICBIAS1 and MICBIAS2 Drive Current                      | -   | 16    | -   | mA    |
| MICBIAS2 Output Voltage                                  |     |       |     |       |
| 0.75*AVDD Setting                                        | -   | 2.475 | -   | V     |
| 0.9*AVDD Setting                                         | -   | 2.97  | -   | V     |
| Verf Pull Up Resistor                                    | -   | 50    | -   | KΩ    |

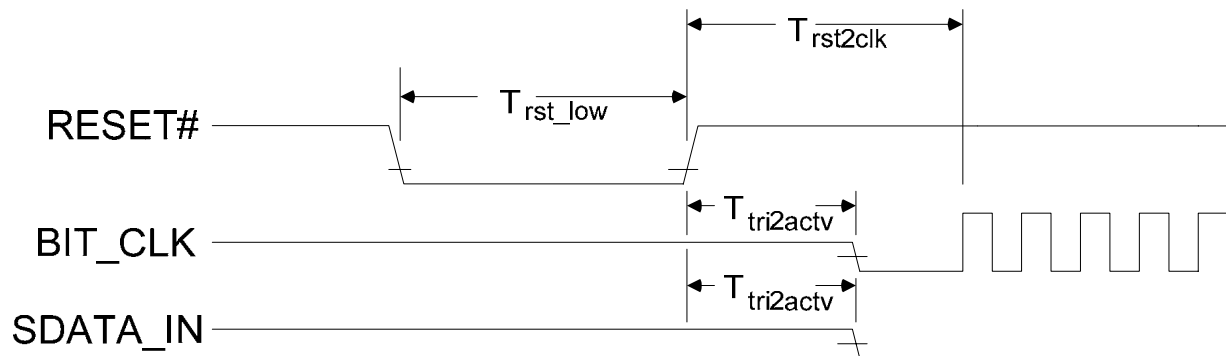
*Note: Standard test conditions:*

*T<sub>ambient</sub> = 25 °C, DVDD = AVDD = HPVDD = 3.3V, SPKVDD = 4.2V.*

*1kHz input sine wave; internal PCM data Sampling frequency = 48kHz; 0dB = 1V<sub>rms</sub>, Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation; EQ and 3D disabled.*

## 9.3. Signal Timing

### 9.3.1. Cold Reset

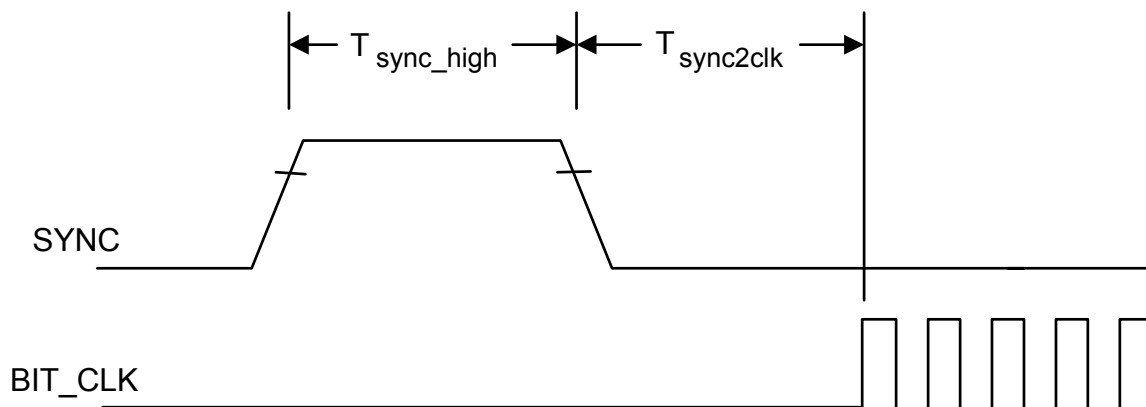


**Figure 14. Cold Reset Timing**

**Table 84. Cold Reset Timing Parameters**

| Parameter                                          | Symbol         | Min   | Typ | Max | Units   |
|----------------------------------------------------|----------------|-------|-----|-----|---------|
| RESET# Active Low Pulse Width                      | $T_{rst\_low}$ | 1.0   | -   | -   | $\mu s$ |
| RESET# Inactive to SDATA-IN or BITCLK Active Delay | $T_{tri2actv}$ | -     | -   | 25  | ns      |
| RESET# Inactive to BIT_CLK Startup Delay           | $T_{rst2clk}$  | 162.8 | -   | -   | ns      |

### 9.3.2. Warm Reset



**Figure 15. Warm Reset Timing**

**Table 85. Warm Reset Timing Parameters**

| Parameter                              | Symbol           | Min    | Typ (Design)  | Max | Units   |
|----------------------------------------|------------------|--------|---------------|-----|---------|
| SYNC Active High Pulse Width           | $T_{sync\_high}$ | 1.0    | 1.3 (16 BCLK) | -   | $\mu s$ |
| SYNC Inactive to BIT_CLK Startup Delay | $T_{sync2clk}$   | 0.1628 | -             | 400 | $\mu s$ |

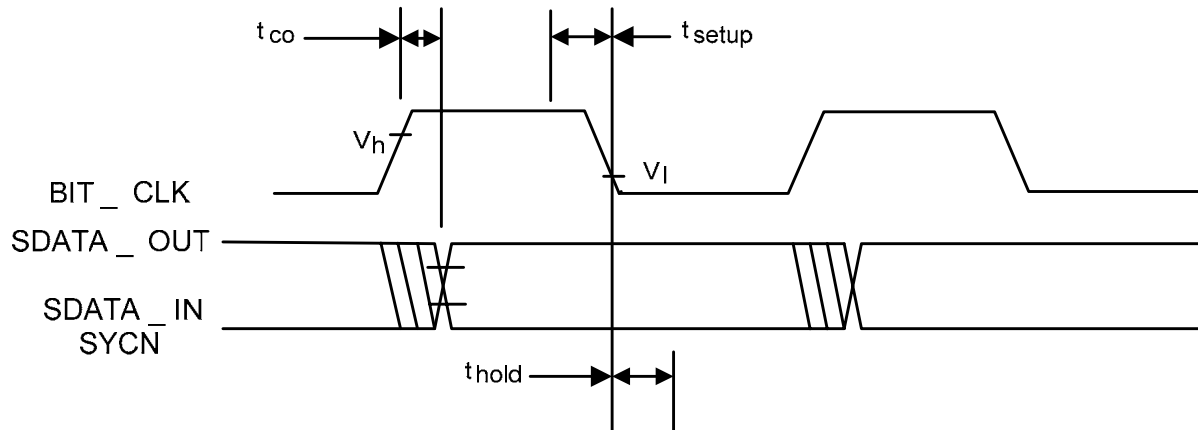
### 9.3.3. AC-Link Clocks

**Table 86. AC-Link Clock Parameters**

| Parameter                 | Symbol             | Min | Typ    | Max | Units   |
|---------------------------|--------------------|-----|--------|-----|---------|
| BIT_CLK Frequency         | -                  | -   | 12.288 | -   | MHz     |
| BIT_CLK Period            | $T_{clk\_period}$  | -   | 81.4   | -   | ns      |
| BIT_CLK Output Jitter     | -                  | -   | -      | 750 | ps      |
| BIT_CLK High Pulse Width* | $T_{clk\_high}$    | 36  | 40.7   | 45  | ns      |
| BIT_CLK Low Pulse Width*  | $T_{clk\_low}$     | 36  | 40.7   | 45  | ns      |
| SYNC Frequency            | -                  | -   | 48.0   | -   | kHz     |
| SYNC Period               | $T_{sync\_period}$ | -   | 20.8   | -   | $\mu$ s |
| SYNC High Pulse Width     | $T_{sync\_high}$   | -   | 1.3    | -   | $\mu$ s |
| SYNC Low Pulse Width      | $T_{sync\_low}$    | -   | 19.5   | -   | $\mu$ s |

Note: Worse case duty cycle restricted to 45/55.

### 9.3.4. AC-Link Data Output and Input Timing


**Figure 16. Data Output and Input Timing**
**Table 87. AC-Link Data Timing Parameters**

| Parameter                                      | Symbol   | Min | Typ | Max | Units |
|------------------------------------------------|----------|-----|-----|-----|-------|
| Output Valid Delay from Rising Edge of BIT_CLK | $t_{co}$ | -   | -   | 15  | ns    |

Note 1: Timing is for SDATA and SYNC outputs with respect to BIT\_CLK at the device driving the output.

Note 2: 50pF external load.

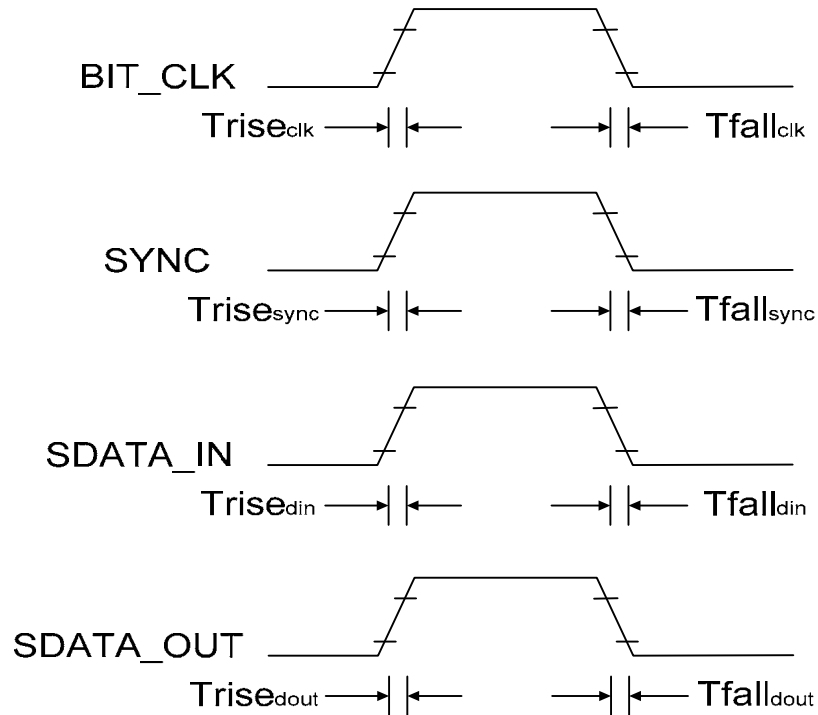
| Parameter                               | Symbol      | Min | Typ | Max | Units |
|-----------------------------------------|-------------|-----|-----|-----|-------|
| Input Setup to Falling Edge of BIT_CLK  | $t_{setup}$ | 10  | -   | -   | ns    |
| Input Hold from Falling Edge of BIT_CLK | $t_{hold}$  | 10  | -   | -   | ns    |

Note: Timing is for SDATA and SYNC outputs with respect to BIT\_CLK at the device driving the output.

| Parameter                                      | Symbol | Min | Typ | Max | Units |
|------------------------------------------------|--------|-----|-----|-----|-------|
| BIT_CLK Combined Rise or Fall Plus Flight Time | -      | -   | -   | 7   | ns    |
| SDATA Combined Rise or Fall Plus Flight Time   | -      | -   | -   | 7   | ns    |

Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes.

### 9.3.5. AC-Link Signal Rise and Fall Timing



**Figure 17. Signal Rise and Fall Timing**

**Table 88. AC-Link Signal Rise and Fall Timing Parameters**

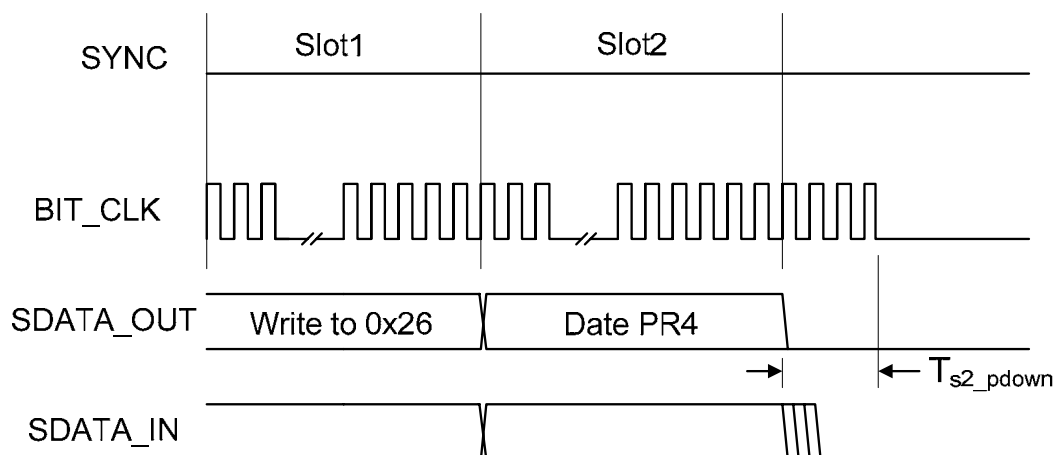
| Parameter           | Symbol           | Min | Typ | Max | Units |
|---------------------|------------------|-----|-----|-----|-------|
| BIT_CLK Rise Time   | $T_{rise\_clk}$  | -   | -   | 6   | ns    |
| BIT_CLK Fall Time   | $T_{fall\_clk}$  | -   | -   | 6   | ns    |
| SYNC Rise Time      | $T_{rise\_sync}$ | -   | -   | 6   | ns    |
| SYNC Fall Time      | $T_{fall\_sync}$ | -   | -   | 6   | ns    |
| SDATA_IN Rise Time  | $T_{rise\_din}$  | -   | -   | 6   | ns    |
| SDATA_IN Fall Time  | $T_{fall\_din}$  | -   | -   | 6   | ns    |
| SDATA_OUT Rise Time | $T_{rise\_dout}$ | -   | -   | 6   | ns    |
| SDATA_OUT Fall Time | $T_{fall\_dout}$ | -   | -   | 6   | ns    |

Note 1: 55pF external load (50pF in AC'97 rev2.1), only for PC system verify case.

Note 2: Rise is from 10% to 90% of  $V_{dd}$  ( $V_{ol}$  to  $V_{oh}$ ).

Note 3: Fall is from 90% to 10% of  $V_{dd}$  ( $V_{oh}$  to  $V_{ol}$ ).

### 9.3.6. AC-Link Low Power Mode Timing



**Figure 18. AC-Link Low Power Mode Timing**

**Table 89. AC-Link Low Power Mode Timing Parameters**

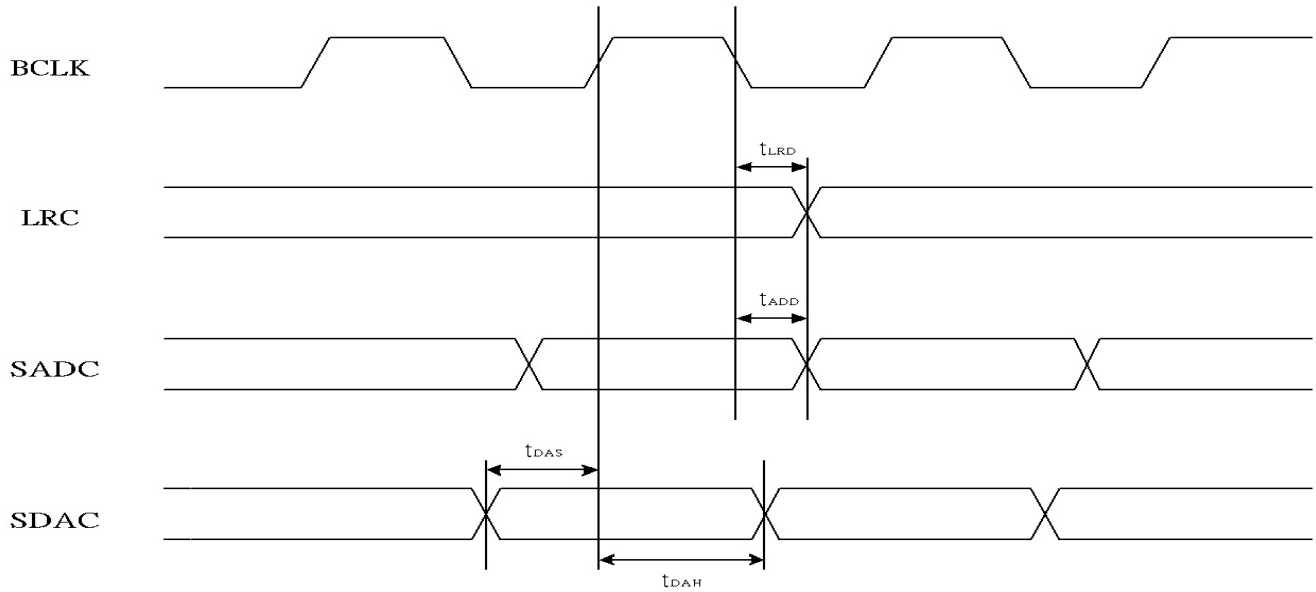
| Parameter                              | Symbol          | Min | Typ | Max | Units   |
|----------------------------------------|-----------------|-----|-----|-----|---------|
| End of Slot 2 to BIT_CLK, SDATA_IN Low | $T_{s2\_pdown}$ | -   | -   | 1.0 | $\mu s$ |

### 9.3.7. AC-Link IO Pin Capacitance and Loading

**Table 90. AC-Link IO Pin Capacitance Parameters**

| Output Pin               | For PC | For PDA | Units |
|--------------------------|--------|---------|-------|
| RESET#, SYNC & SDATA_OUT | 47.5   | 25      | pF    |
| BIT_CLK                  | 47.5   | 25      | pF    |
| SDATA_IN                 | 47.5   | 25      | pF    |

### 9.3.8. I<sup>2</sup>S/PCM Interface Master Mode

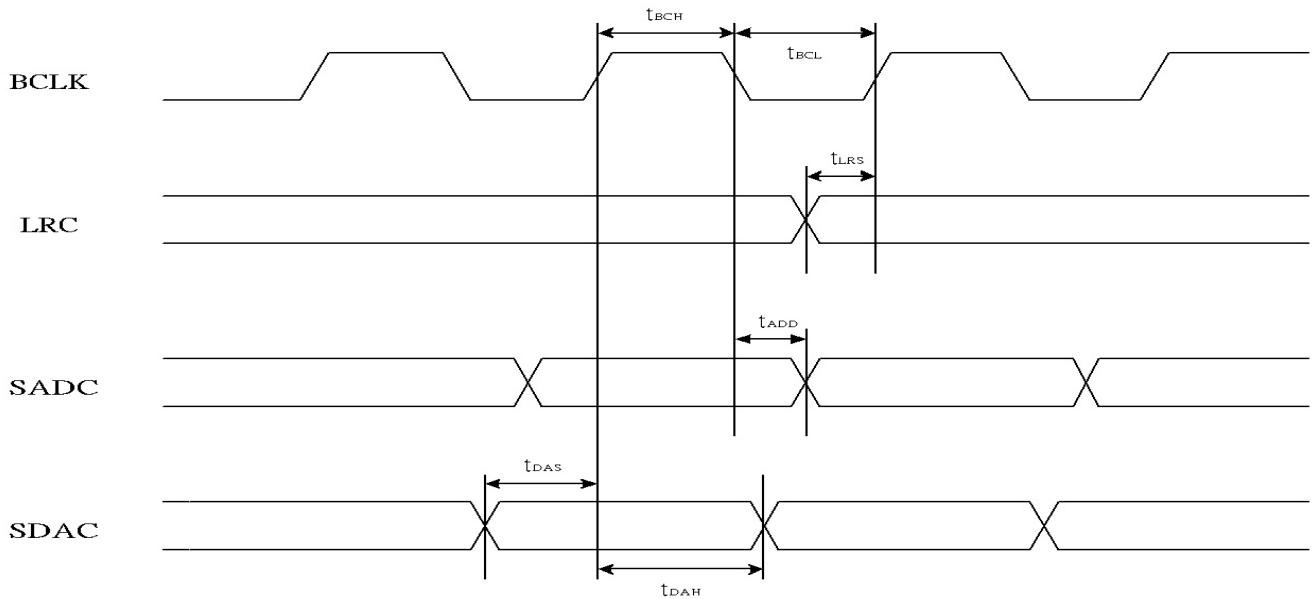


**Figure 19. Timing of I<sup>2</sup>S/PCM Master Mode**

**Table 91. Timing of I<sup>2</sup>S/PCM Master Mode**

| Parameter                 | Symbol    | Min | Typ | Max | Units |
|---------------------------|-----------|-----|-----|-----|-------|
| LRCK Output to BCLK Delay | $t_{LRD}$ | -   | -   | 30  | ns    |
| Data Output to BCLK Delay | $t_{ADD}$ | -   | -   | 30  | ns    |
| Data Input Setup Time     | $t_{DAS}$ | 10  | -   | -   | ns    |
| Data Input Hold Time      | $t_{DAH}$ | 10  | -   | -   | ns    |

### 9.3.9. I<sup>2</sup>S/PCM Interface Slave Mode

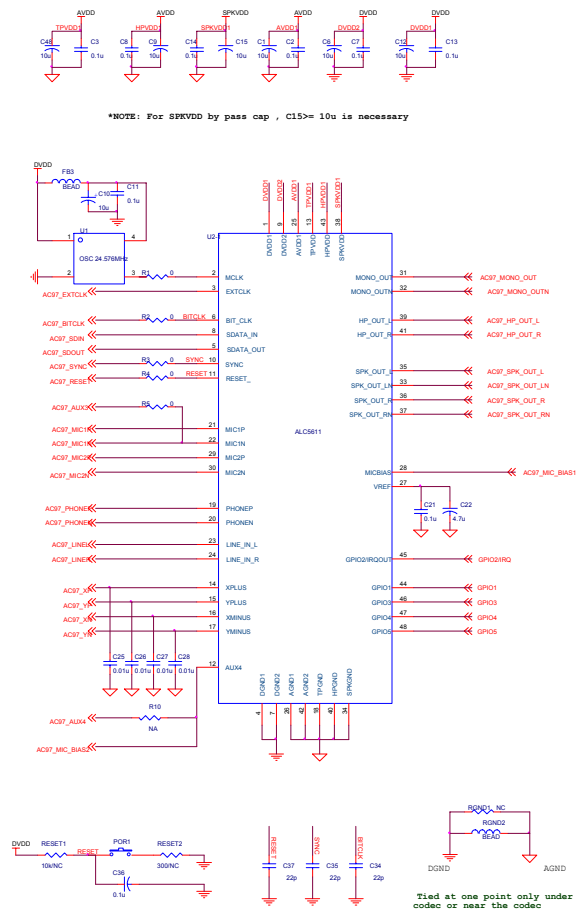


**Figure 20. I<sup>2</sup>S/PCM Slave Mode Timing**

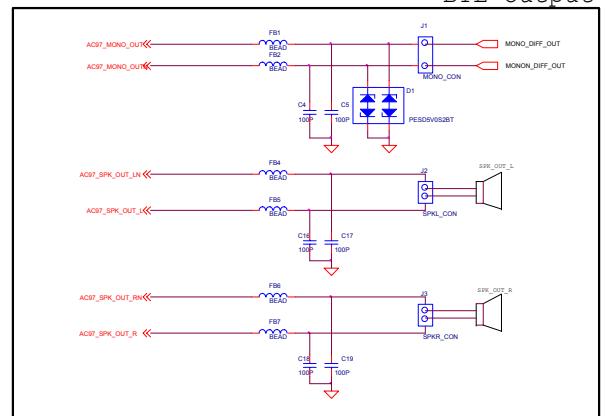
**Table 92. I<sup>2</sup>S/PCM Slave Mode Timing**

| Parameter                 | Symbol    | Min | Typ | Max | Units |
|---------------------------|-----------|-----|-----|-----|-------|
| BCLK High Pulse Width     | $t_{BCH}$ | 20  | -   | -   | ns    |
| BCLK Low Pulse Width      | $t_{BCL}$ | 20  | -   | -   | ns    |
| LRCK Input Setup Time     | $t_{LRS}$ | 30  | -   | -   | ns    |
| Data Output to BCLK Delay | $t_{ADD}$ | -   | -   | 30  | ns    |
| Data Input Setup Time     | $t_{DAS}$ | 10  | -   | -   | ns    |
| Data Input Hold Time      | $t_{DAH}$ | 10  | -   | -   | ns    |

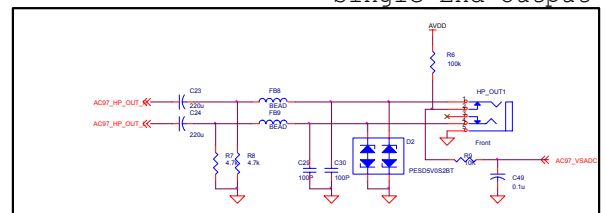
## 10. Application Circuits



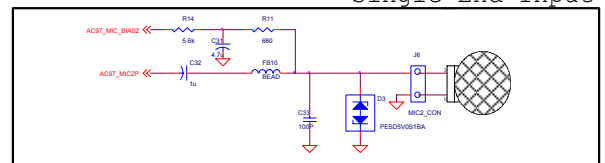
### BTL Output



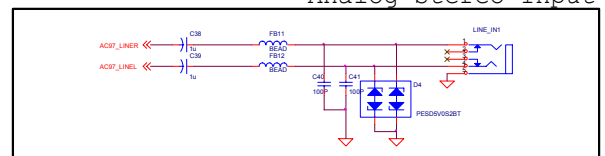
### Single End Output



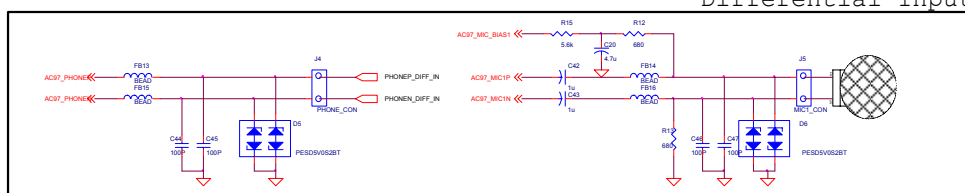
### Single End Input



### Analog Stereo Input

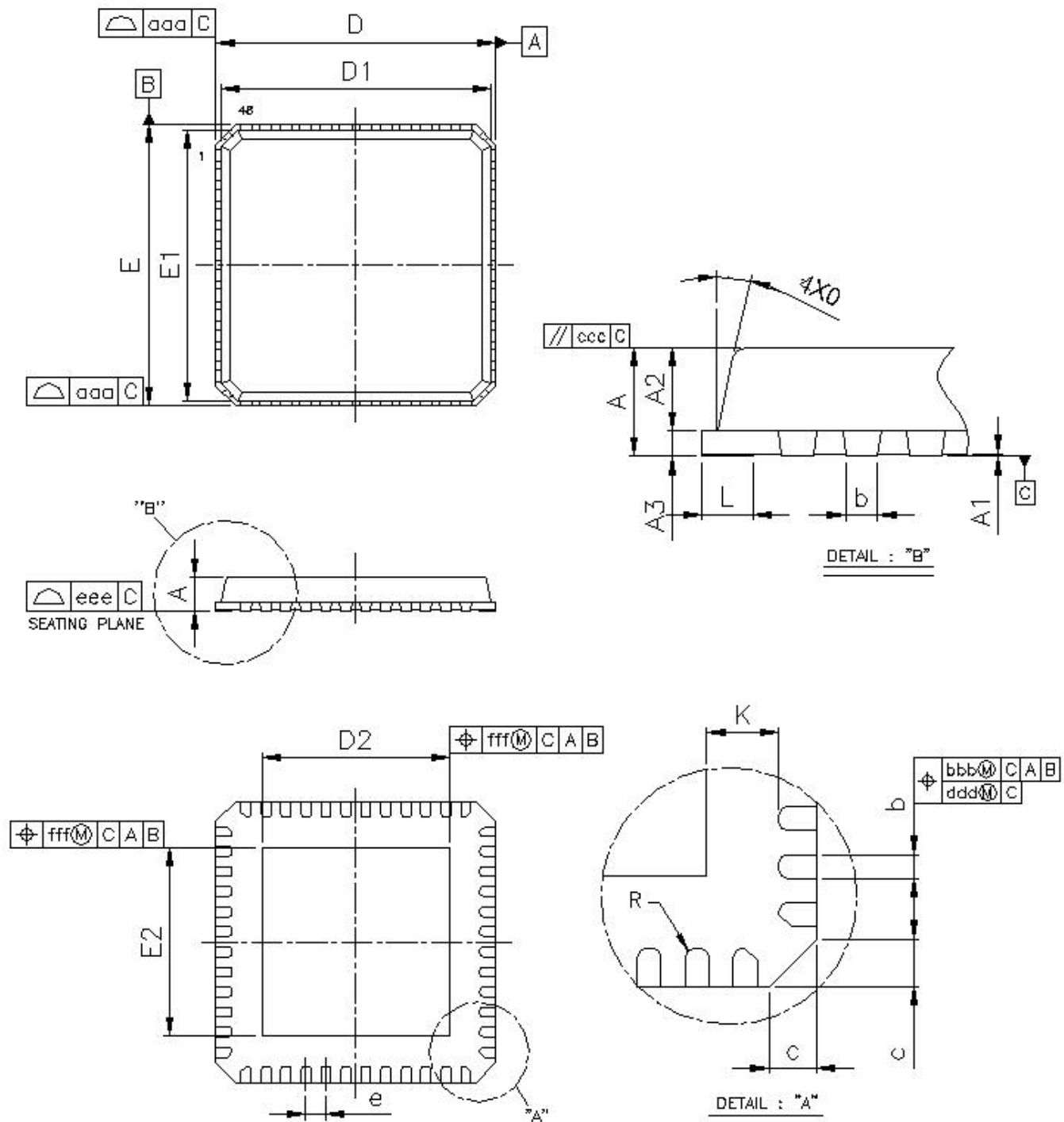


Differential Input



## 11. Mechanical Dimensions

### Plastic Quad Flat No-Lead Package 48 Leads 7x7mm Outline



| Symbol                         | Dimension in mm |      |      | Dimension in inch |       |       |
|--------------------------------|-----------------|------|------|-------------------|-------|-------|
|                                | Min             | Nom  | Max  | Min               | Nom   | Max   |
| A                              | 0.75            | 0.85 | 1.00 | 0.030             | 0.034 | 0.039 |
| A <sub>1</sub>                 | 0.00            | 0.02 | 0.05 | 0.000             | 0.001 | 0.002 |
| A <sub>2</sub>                 | 0.55            | 0.65 | 0.80 | 0.022             | 0.026 | 0.032 |
| A <sub>3</sub>                 | 0.20REF         |      |      | 0.008REF          |       |       |
| b                              | 0.18            | 0.25 | 0.30 | 0.007             | 0.010 | 0.012 |
| c                              | -               | -    | 0.6  | -                 | -     | 0.024 |
| D/E                            | 7.00BSC         |      |      | 0.276BSC          |       |       |
| D <sub>1</sub> /E <sub>1</sub> | 6.75BSC         |      |      | 0.266BSC          |       |       |
| D <sub>2</sub> /E <sub>2</sub> | 4.80            | 5.05 | 5.30 | 0.189             | 0.199 | 0.209 |
| e                              | 0.50BSC         |      |      | 0.020BSC          |       |       |
| L                              | 0.30            | 0.40 | 0.50 | 0.012             | 0.016 | 0.020 |
| K                              | 0.2             | -    | -    | 0.008             | -     | -     |
| θ                              | 0°              | -    | 14°  | 0°                | -     | 14°   |
| aaa                            | -               | -    | 0.15 | -                 | -     | 0.006 |
| bbb                            | -               | -    | 0.10 | -                 | -     | 0.004 |
| ccc                            | -               | -    | 0.10 | -                 | -     | 0.004 |
| ddd                            | -               | -    | 0.05 | -                 | -     | 0.002 |
| eee                            | -               | -    | 0.08 | -                 | -     | 0.003 |
| fff                            | -               | -    | 0.10 | -                 | -     | 0.004 |

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).

Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

## 12. Ordering Information

**Table 93. Ordering Information**

| Part Number | Package                                 | Status |
|-------------|-----------------------------------------|--------|
| ALC5611-GR  | QFN-48 in 'Green' Package (Tray)        | MP     |
| ALC5611-GRT | QFN-48 in 'Green' Package (Tape & Reel) | MP     |

*Note 1: See page 6 for Green package and version identification.*

*Note 2: Above parts are tested under AVDD=3.3V.*

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