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# AL240 Video Decoder Data Sheets

Version 1.0

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## Amendments

- 11.01.04 Preliminary version 0.1
- 11.10.04 Change input video port selection: Y0/C0 = AI1/AI2; Y1/C1 = AI0/AI3
- 11.17.04 Fix crystal input/output (XIN/XOUT) frequency range at 20MHz.
- 11.18.04 Delete register 01h<bit7> definition; change to “Reserse”
- 12.27.04 Update to Version 0.3
- Change to Lead Free (PBF) package
  - Revised “Function Description” contents. Add “Software Reset”/“Phase Lock Loop” descriptions.
  - Add Sec10.3 “reference setting value” in register description.
  - Add “Electrical Characteristics”
  - Revised registers description of register# BDh~BFh/D0h
- 1.13.05 Update to Version 0.4
- Change input video port selection: Y0/C0 = AI0/AI2; Y1/C1 = AI1/AI3
  - Add Reg#03h<bit 2:0> “adaptive\_mode” to software programming table of input video selection.
  - Add registers to section 10.1 “Register Set”
  - Remove “color bar” function.
  - Revised “AGC control” content.
  - Revised “Input Format” content. Add channel switch programming suggestions.
  - Change register BAh name to “ PLLCTRL2”
  - Add “ Feh = FF” in section 10.3 “Reference setting value” for all modes; change register 02h value to “4Eh” for all modes.
- 2.10.05
- Remove 22-bit RGB output support
  - Add 22-bit YCbCr output support
  - Rearrange VBI registers number
  - Change Reg#65<5:4> to reserve
  - Add output timing diagrams
  - Add AC characteristics for output interface
- 2.14.05
- Revise output data format from YUV to YCbCr
  - Revise contents of *Analog Front End* section
- 2.15.05
- Update to Version 1.0
- 2.19.05
- Change Marking to “AL240-B-QF44-PBF”
  - Replace the Analog front-end application schematic with AL240.

THE INFORMATION CONTAINED HEREIN IS SUBJECT TO CHANGE WIHOUT NOTICE.

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## 1 General Description

The AL240 is silicon efficient, cost effective high video quality NTSC/PAL SECAM video decoder with high quality Y/C separation process. The AL240 decode NTSC/PAL SECAM composite video or S-video and convert it into YCbCr 4:2:2, 8-bit digital video output. Employing adaptive filter technology, the AL240 is able to provide a clear Y/C separated signals while maintaining excellent frequency response. The result is sharp, high detail video that eliminates unwanted dot crawl and false color effects. Fully programmable video characteristic control, such as hue, contrast, brightness, saturation, are supported. The AL240 decoder incorporates an advanced vertical blanking interval (VBI) data processor to do data slicing, parsing and decoding teletext, closed caption, and other formats. Two wires of hardware channel switching input allow decoder to do an instant alternation of analog CVBS input from one to the other. Up to 4 serial bus addresses can be selected via 2 configuration pins that allows multiple AL240 chips on the design without extra logic.

The AL240 supports power saving mode and operates under the low power voltages (3.3V and 1.8V) with 44-pin Lead Free (PBF) QFP package.

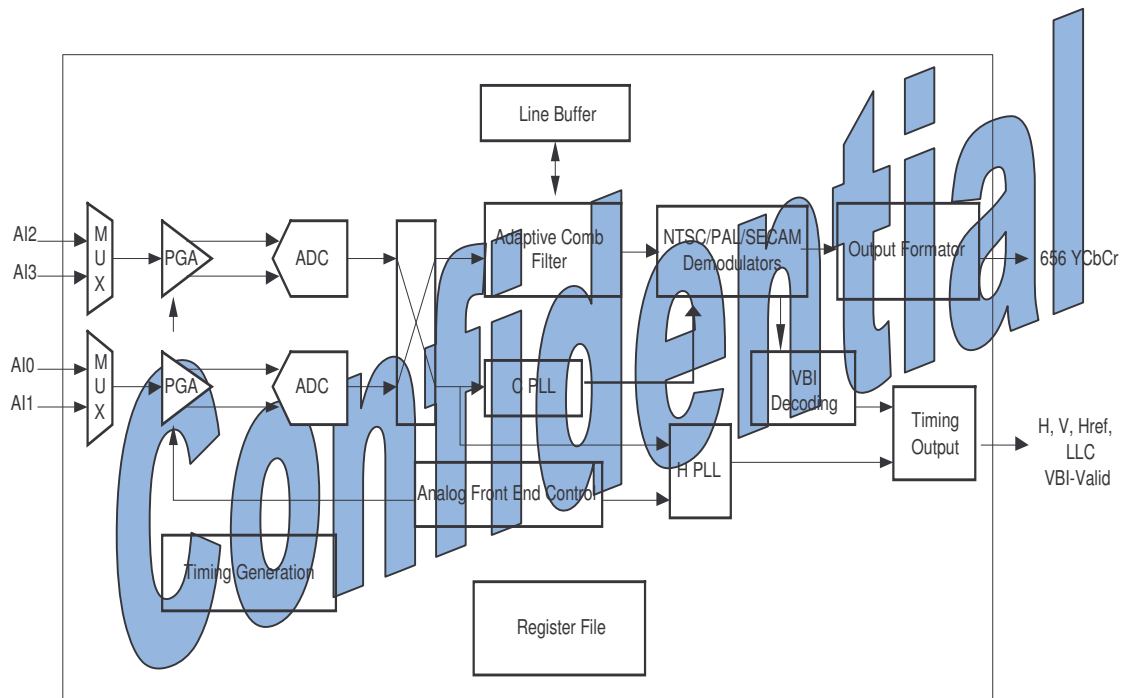
## 2 Features

- Decodes NTSC, PAL and SECAM composite video or S-video
- Supports all variations of the NTSC standard – (M, 4.43)
- Supports all variation of the PAL standard – (I, B, G, H, D, N, M, combination N)
- 2x 10-bit A/D converter
- Supports digital automatic gain control (AGC)
- 4 analog input with internal switches among four input for e.g. 4xCVBS, 2xS-Video or (2xCVBS & 1xS-Video)
- Standard 8-bit ITU-R.BT656 along with separate sync signals, YCbCr 4:2:2 format output
- Line-Locked system clock frequencies
- Excellent quality Y/C separation – minimizes cross luma and cross color effects
- Adaptive Comb Filter for NTSC&PAL Y/C separation
- Software support format detection of video standard (NTSC, PAL or SECAM)
- BCS (Brightness/Contrast/Saturation and Hue) control
- Auto detects and locks VCR trick modes
- Support VBI decoding
- Decodes weak and noisy off-air signals
- Hardware channel switching
- Two-wire serial bus programming with up to 4 serial bus sub-addresses selectable
- Software power down mode
- 3.3V and 1.8V mix low power supply
- 44-pin QFP Lead Free package

### 3 Applications

- Video surveillance applications.
- Mobile System
- Handheld Applications
- Video Capture devices
- Video Phone
- Networking Video

### 4 Block Diagram

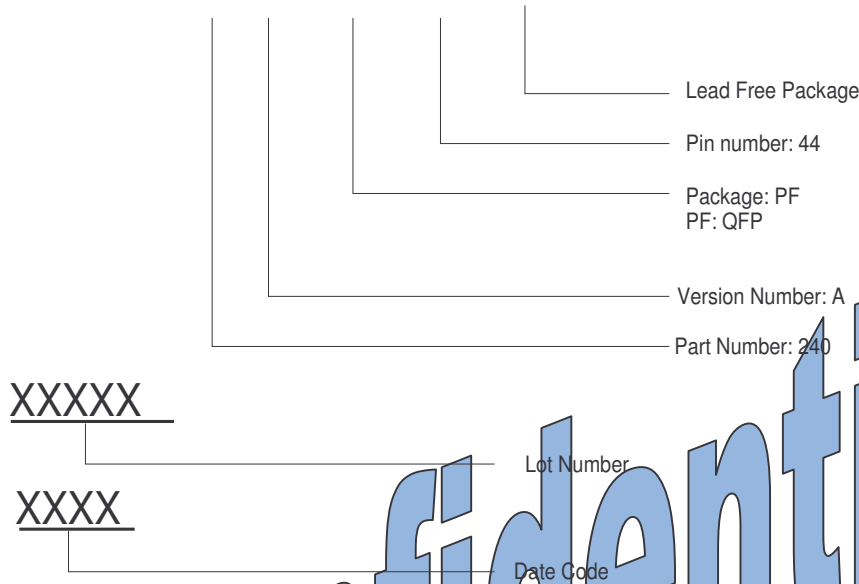


AL240 Adaptive Comb Filter Video Decoder Block Diagram

## 5 Chip Information

### 5.1 Marking Information

AL240-Y-ZZZddd-PBF



### 5.2 Ordering Information

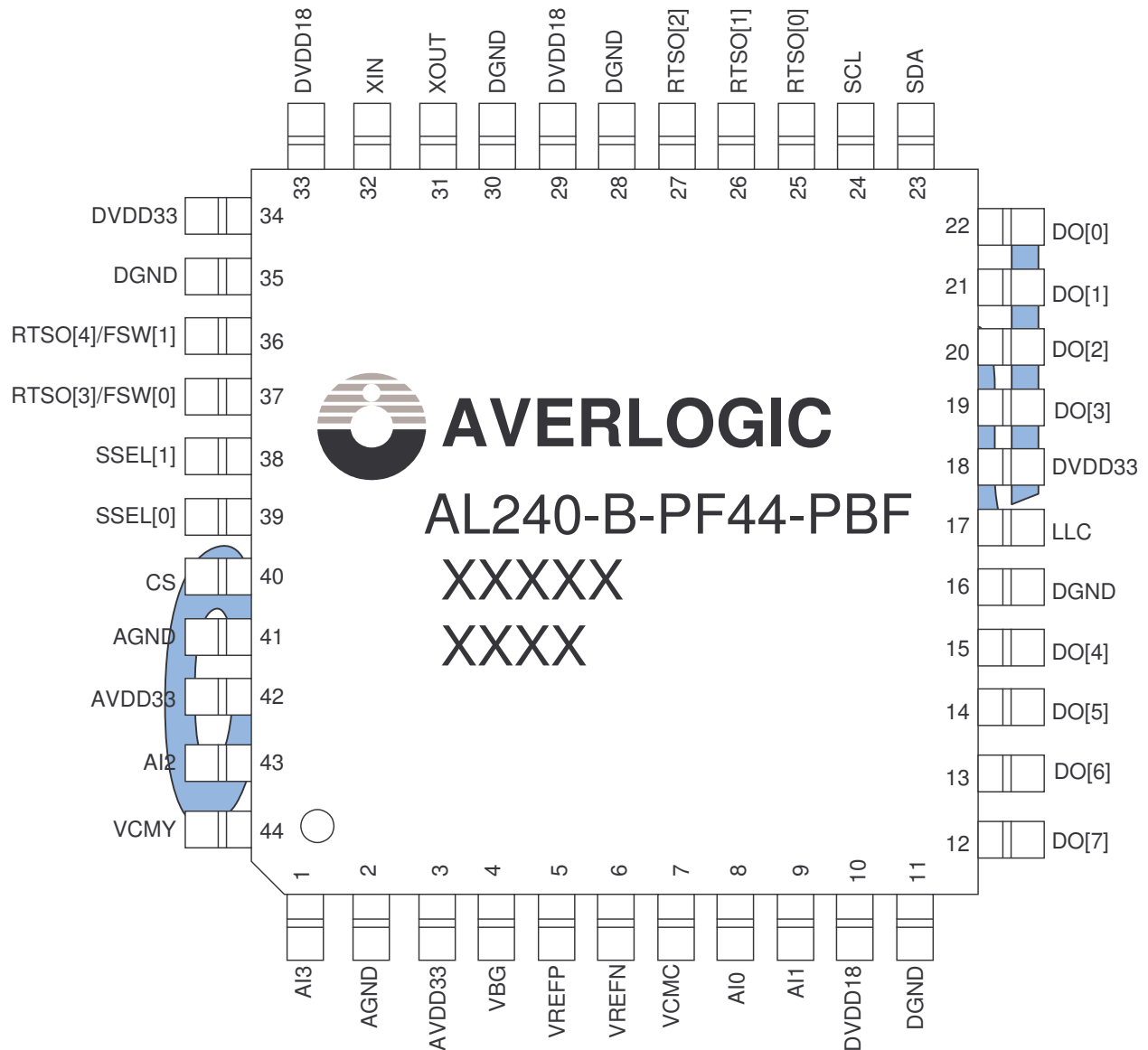
AL240 is available in 44-pin QFP package.

| Part number      | Package                            | Power Supply | Status   |
|------------------|------------------------------------|--------------|----------|
| AL240-B-PF44-PBF | PF44: 44-pin plastic QFP (10x10mm) | +1.8/3.3V    | Q1, 2005 |

Note: AverLogic Technologies PB-free products employ special PB-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish do not use materials containing PBB, PBDE or red phosphorus for green-product chips. AverLogic's PB-free products are MSL classified at PB-free peak reflow temperatures that meet or exceed the PB-free requirements of IPC/JEDEC J Std-020B."

## 6 Pin Diagram

The AL240 pin-out diagrams are following:



AL240 QFP - 44 PACKAGE TOP VIEW

## 7 Pin Definition and Description

The pin-out definition and function are described as following:

| Pin name       | QFP-44<br>Pin number | I/O<br>type | Description                                                                                                                                                                                                          |
|----------------|----------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AI3            | 1                    | I           | Analog input 3 (see input signal mapping table for details)                                                                                                                                                          |
| VBG            | 4                    | I           | Decoupling or bypass of Bandgap voltage                                                                                                                                                                              |
| VREFP          | 5                    | I           | Decoupling or bypass of positive internal reference voltage                                                                                                                                                          |
| VREFN          | 6                    | I           | Decoupling or bypass of negative internal reference voltage                                                                                                                                                          |
| VCMC           | 7                    | I           | Chroma channel PGA negative reference input                                                                                                                                                                          |
| AI0            | 8                    | I           | Analog input 0 (see input signal mapping table for details)                                                                                                                                                          |
| AI1            | 9                    | I           | Analog input 1 (see input signal mapping table for details)                                                                                                                                                          |
| DO[7:0]        | 12~15,<br>19~22      | O           | Digital 8-bit Video Data output signal;<br>• YCbCr output data bus for 8-bit ITU-R.BT656                                                                                                                             |
| LLC            | 17                   | O           | 27 MHz LLC (line-locked clock) output                                                                                                                                                                                |
| SDA            | 23                   | I/O         | Serial data input/output (Two-wire serial bus)                                                                                                                                                                       |
| SCL            | 24                   | I           | Serial clock input (Two-wire serial bus)                                                                                                                                                                             |
| RTSO[0]        | 25                   | O           | Real Time Synchronization signals output 0                                                                                                                                                                           |
| RTSO[1]        | 26                   | O           | Real Time Synchronization signals output 1                                                                                                                                                                           |
| RTSO[2]        | 27                   | O           | Real Time Synchronization signals output 2                                                                                                                                                                           |
| RTSO[3]/FSW[0] | 37                   | O           | Real Time Synchronization signals output 3 when B7h[3] = 0 or hardware channel switching control, input channel select FSW[0] when register B7h[3] = 1                                                               |
| RTSO[4]/FSW[1] | 36                   | O           | Real Time Synchronization signals output 4 when B7h[4] = 0 or hardware channel switching control, input channel select FSW[1] when register B7h[4] = 1                                                               |
| XOUT           | 31                   | O           | Crystal output: 20 MHz                                                                                                                                                                                               |
| XIN            | 32                   | I           | Crystal input: 20 MHz                                                                                                                                                                                                |
| SSEL[1:0]      | 38, 39               | I           | Serial bus slave address select:<br>00: write address: 20H, read address: 21H<br>01: write address: 22H, read address: 23H<br>10: write address: 24H, read address: 25H<br>11: write address: 26H, read address: 27H |
| CS             | 40                   | I           | Global Reset Input and chip select. Pull high to enable chip operation and pull low to do chip reset                                                                                                                 |
| AI2            | 43                   | I           | Analog input 2 (see input signal mapping table for details)                                                                                                                                                          |
| VCMY           | 44                   | I           | Luma channel PGA negative reference input                                                                                                                                                                            |

| POWER, GROUND |                   |     |                                |
|---------------|-------------------|-----|--------------------------------|
| AGND          | 2, 41             | PWR | Analog ground                  |
| AVDD33        | 3, 42             | PWR | Analog power, 3.3V             |
| AVDD18        | 10                | PWR | Analog power, 1.8V             |
| AGND          | 11                | PWR | Analog ground                  |
| DGND          | 16, 28, 30,<br>35 | PWR | Digital pad ground             |
| DVDD33        | 18, 34            | PWR | Digital I/O pad power, 3.3V    |
| DVDD18        | 29, 33            | PWR | Digital core logic power, 1.8V |

Note: I/O signal level: 3.3V and 5V tolerant.

## 8 Function Description

### 8.1 Analog Front End

The Analog Front End circuit of decoder incorporates two 10-bit Analog-to-Digital Converters (ADC) performs the following functions

- DC restore
- Variable gain
- Analog to Digital conversion

The video signal is inherently a DC signal. It requires DC restoration as normally been AC coupled. Sustaining the same voltage level of certain reference part of the signal is crucial for proper decoding. The programmable gain amplifier (PGA) and the AGC circuit compensate the input signal amplitude to ensure the proper input range for the ADC.

Input base-band video signal amplitudes may vary significantly from the nominal level. It may be doubly terminated with 2 loads or un-terminated to allow pass through to other video equipment. This will result in a gain range from 4 to 1/2.

- The signal will have a gain of one if it is properly terminated
- The signal will have a gain of ½ if it is doubly terminated
- The signal will have a gain of 2 if it is un-terminated

Thus the automatic gain control (AGC) can be set to a range of ½ to 2. Normally the AGC has a maximum gain larger than 2 (possibly as high as 4) in order to ensure that processing signals are maintained at constant levels by boosting weak signals for instance output from a distant broadcast. However, the AGC does not need a wide bandwidth for gain larger than 2 because a larger gain usually introduces “noise” on the signal.

### 8.1.1 Analog Input Process

AL240 offers four analog inputs with internal switches to select among them e.g. 4 CVBS or 2 Y/C or 1 Y/C and 2 CVBS. It allows seamless switching between video sources through software programming. In addition, the hardware channel switching is also supported for composite video inputs. During the hardware channel switching, the FSW[1:0] pins are configured as control signals to select among 4 CVBS inputs. The selections of inputs are illustrated in input format section. The analog input processor contains clamp circuit, analog amplifier, anti-alias filter and two video 10-bit CMOS ADCs. This high performance analog process converts an analog signal to a quality digital data for further decoding process.

### 8.1.2 AGC control

The gain control circuit will refer the gain levels defined at registers for the two analog amplifiers or control these amplifiers automatically via a built – in Automatic Gain Control (AGC) circuit. The automatic chroma gain control compensates for reduced chroma and color-burst amplitude. The automatic luma/composite gain control is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range. This means AGC will attempt to maintain all signals at a constant level, the video signals, and general noise when input video is interrupted which should not be amplified. In practical, the AL240 displays “Blue screen” (no video) once proper video signal is not presented, yet the AGC seeks to boost any signals despite its nature, AL240 would fail to exhibit “Blue screen” under noisy environment while attempting to display the “noise”. Manual gain control is preferred in professional application. The Luma and chroma AGC target values can be specified in register “HAGC” (04h)/ “CHROMAAGC” (0Ch) respectively.

### 8.1.3 Sync and Clocks

AL240 produces a 27 MHz (LLC) output clock to synchronize 8-bit data output in YCbCr 4:2:2 formats. The sync signals are output from RTSO[0] ~ RTSO[4] and control by registers B2h[4:0] ~ B6h[4:0] respectively. The pins are individually programmable to yield following signals:

| Register value of bit <4:0> | Output            |
|-----------------------------|-------------------|
| 00h                         | 0                 |
| 01h                         | 1                 |
| 02h                         | Hsync             |
| 03h                         | Vsync             |
| 04h                         | Field             |
| 05h                         | Hactive           |
| 06h                         | Vactive           |
| 07h                         | Hactive & vactive |
| 08h                         | VBI-valid         |
| 09h                         | No signal         |
| 0Ah                         | Sync_locked       |
| 0Bh                         | Composite sync    |
| Others                      | Reserved          |

## 8.2 Power-Up and Chip Select (CS)

During power-up, the CS pin must be low for few ms to initial the reset sequence to bring AL240 registers to its default values. After the rising edge of CS, the chip will be in active stage after some ms period; then the chip can be programmed for the desired configuration.

## 8.3 Software Reset

After power-up or a hardware reset, the decoder will remain in a reset state until register 3Fh bit 0 is set to “0” (default value is “1”). The chip will perform a software reset if 3Fh bit 0 is set to “1”. The software reset will affect all modules except for the registers and only a hardware reset will restore the registers back to default values.

## 8.4 Power-down and Power saving

A low stage of CS pin will reset the chip to default condition and keep at this stage as long as the CS is in low position. The internal operating clock will be in quiet period and no register can be access until a high stage of CS. During the operation mode (CS in high), the AL240 supports power saving mode where the PLL clock can be turned off by programming B8h<1>=1 via two-wire serial bus. To wake up the chip, just program B8h<1>=0 back to normal operation while register values are maintained.

## 8.5 Phase Lock Loop (PLL)

The input clock frequency for the decoder is 20MHz. The clock frequency tolerance should be within  $\pm 50$ ppm. Both the chroma and the horizontal acquisition DTO registers must be programmed appropriately for a specific input (and output) clock frequency.

### Chroma DTO:

Registers 18h through 1Bh are used to control the chroma DTO increment value. Following formula applies to determine the setting values,

$$cdto\_inc = (4f_{sc} / f_{input}) \times 2^{30}, \text{ where } f_{sc} \text{ is the chroma sub-carrier frequency}$$

Where,

$f_{input}$  is 20MHz input clock;

$4f_{sc}$  is sub-carrier frequency.

And their corresponding frequencies in different standard are:

| Standard        | $4f_{sc}$ (MHz) |
|-----------------|-----------------|
| NTSC 3.58       | 14.31818182     |
| NTSC 4.43       | 17.734475       |
| PAL B,D,G,H,I,N | 17.734475       |
| PAL M           | 14.30244596     |
| PAL CN          | 14.328225       |

|       |        |
|-------|--------|
| SECAM | 17.144 |
|-------|--------|

## 8.6 Input Format

The AL240 is capable to multiplex 4 CVBS or 2 S-video of 4 analog ports without external multiplexer. The video input selector is illustrated in the proceeding figures.

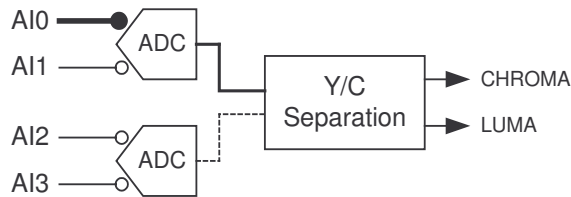


Fig. CVBS0

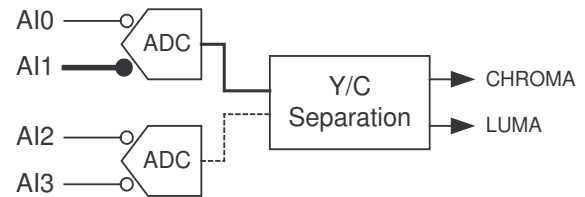


Fig. CVBS1

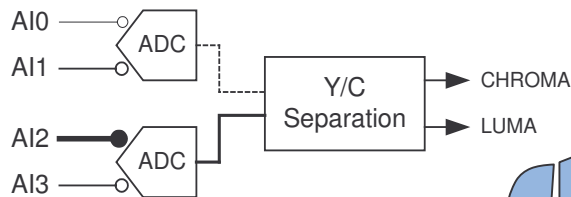


Fig. CVBS2

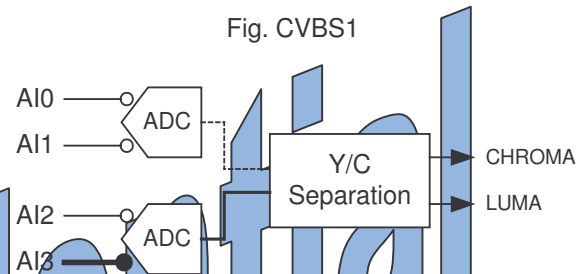


Fig. CVBS3

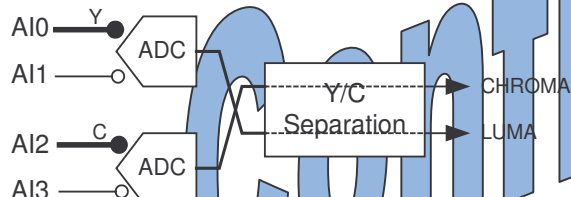


Fig. S-Video: Y0/C0

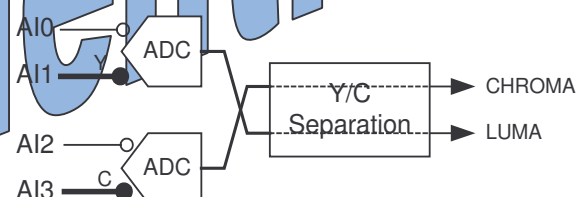


Fig. S-Video: Y1/C1

**Figure 1: Input Format Selector**

The input video signals can be selected either through software programming setup (registers) via two-wire serial bus or by hardware control-pins RTSO[3]/FSW[0] and RTSO[4]/FSW[1]. The hardware control is only available for CVBS inputs. The control methods of input selection are defined in “fast\_sw” (bit 3 of register B7h). When this bit is set to 0, the input signals are selected via registers setup; logic 1 will select hardware control for input composite signals.

When the input video signals are selected by software settings, the corresponding register values and input video signals are described in the following table.

Where

adaptive\_mode: 03h<bit 2:0>  
 fast\_sw : register B7h<bit 3>,  
 yc\_src: register 00h<bit 0>,  
 afe\_in\_sel: register B7h<bit 1:0>.

| 03h<2:0><br>adaptive_mode | B7h<3><br>Fast_sw | 00h<0><br>yc_src | B7h<1:0><br>afe_in_sel | Input pin     | Signal          |
|---------------------------|-------------------|------------------|------------------------|---------------|-----------------|
| XXX                       | 0                 | 0                | 00                     | AI0           | CVBS0           |
| XXX                       | 0                 | 0                | 01                     | AI1           | CVBS1           |
| XXX                       | 0                 | 0                | 10                     | AI2           | CVBS2           |
| XXX                       | 0                 | 0                | 11                     | AI3           | CVBS3           |
| 011                       | 0                 | 1                | 00                     | AI0/AI2 (Y/C) | S video (Y0/C0) |
| 011                       | 0                 | 1                | 01                     | AI1/AI3 (Y/C) | S video (Y1/C1) |

For composite video inputs (4 CVBS), AL240 provides hardware channel switching by using hardware control pins RTSO[3]/FSW[0] and RTSO[4]/FSW[1] (in this case RTSO[3]/FSW[0] and RTSO[4]/FSW[1] are input pins). The input CVBS signals can be configured via hardware pins according to the table below.

Where

fast\_sw : register B7h<bit 3>,

yc\_src: register 00h<bit 0>,

FSW[1:0]: pin RSTO[4]/FSW[1] and RSTO[3]/FSW[0].

| B7h<3><br>Fast_sw | 00h<0><br>yc_src | FSW[1:0]<br>Signals | Input pin | Signal                   |
|-------------------|------------------|---------------------|-----------|--------------------------|
| 1                 | 0                | LL                  | AI0       | Hardware switching CVBS0 |
| 1                 | 0                | LH                  | AI1       | Hardware switching CVBS1 |
| 1                 | 0                | HL                  | AI2       | Hardware switching CVBS2 |
| 1                 | 0                | HH                  | AI3       | Hardware switching CVBS3 |

Note: Note: L – Input logic low; H – Input logic high.

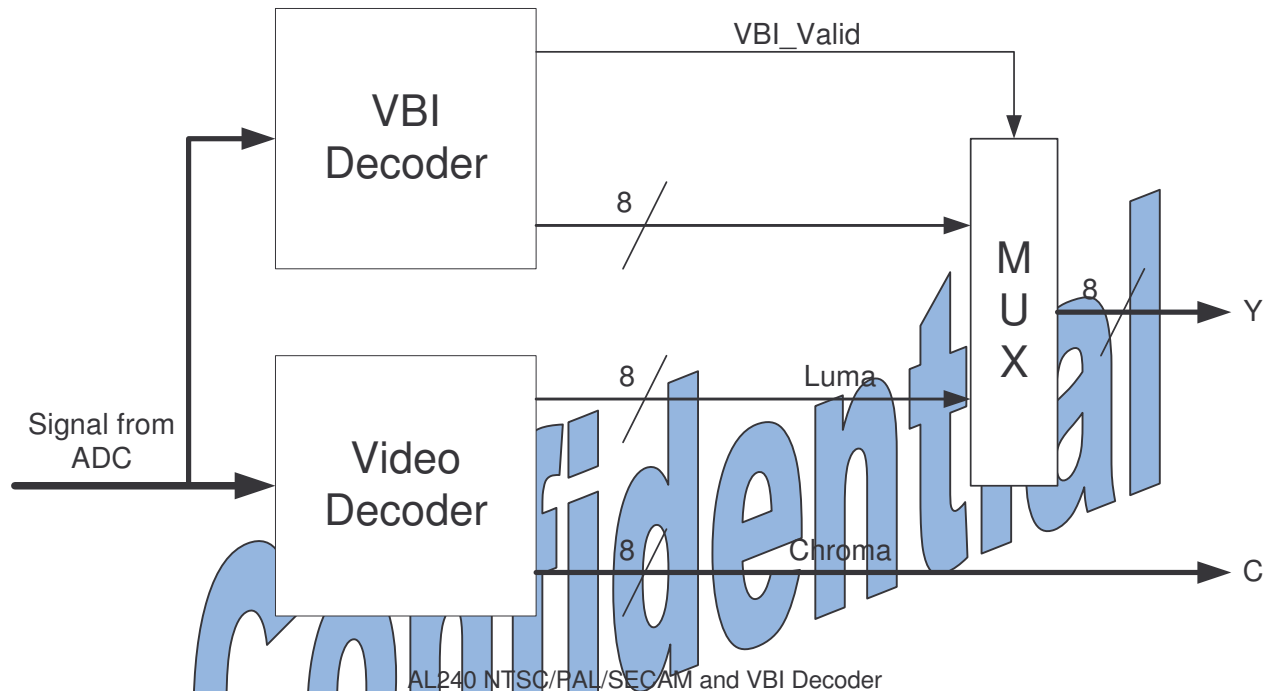
For smooth channel switching, it is essential to ensure that AL240 detects the proper phase of the video signal. Selecting appropriate vertical sync control mode ensure that following the channel switch operation the AL240 is locked to the Luminance as well as chrominance for the color video signal.

## 8.7 Adaptive Comb Filter

A comb filter can provide the better Y/C separation result from standard broadcasts, laserdisc, and other composite sources without introducing some artifact in digital output. It also reduces discolorations in fine picture details and provides purer color overall. A 3/5-line digital comb filter is incorporated in the chip for NTSC/PAL composite video input to do Y and C signals separation. The separation parse will look up 3/5 consecutive horizontal scan lines simultaneously so that it can identify true chromance data out of lumance data for better data separation. The AL240's adaptive comb filter can dynamically change filter algorithm in the luma or chroma path to have a better luma and chroma separation without introducing artifacts such as dots crawling at color boundaries or false colors in high frequency luminance images (e.g. multi-burst pattern). Various Y/C separation modes can also be manually selected by "adaptive\_mode" (bit<2:0> of register 03h)

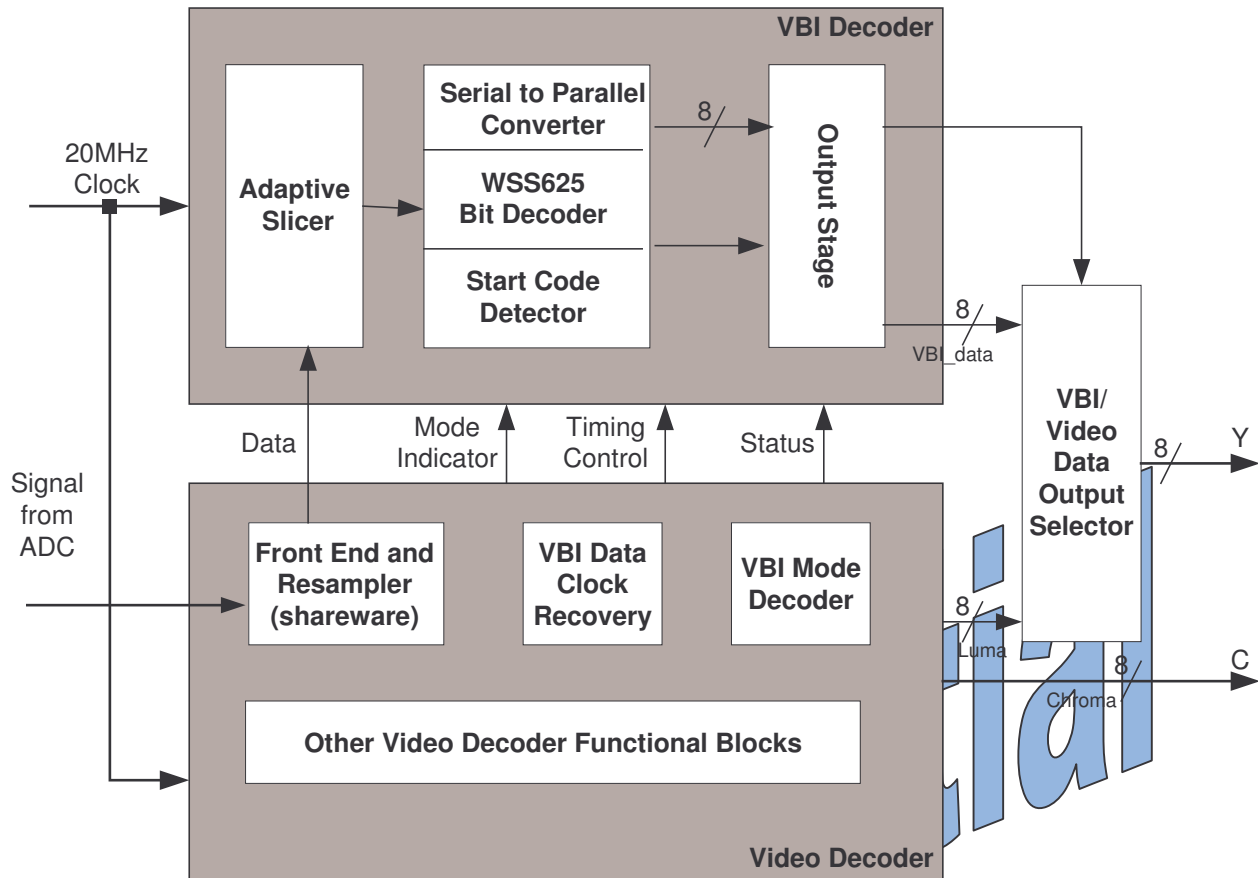
## 8.8 VBI

AL240's VBI decoder services various data type, teletext, close caption (CC) and wide screen (WSS) signals, etc. The basic function of VBI decoder is to capture the VBI data embedded in the analog video signal and convert it to its digital counterpart. The VBI output data is a stream of 8-bit (byte) data, which can be stored in the registers for further decoding according to different VBI data type. Figure below shows the data path in the decoder for the video and VBI data decoding.



**Figure 2: VBI Decoder**

Following figure is a simplified block diagram of a VBI decoder. The start code detector compares the 8-bit data from the ADC to the predefined code-word during the valid start code detection period. If start code detected, the bit-counter, byte-counter in the serial to parallel convert and the output stage block will be reset to zero. In addition, the next bit from the slicer is the least significance of the first valid VBI data.



A simplified block diagram for the partition of VBI decoder and Video decoder

**Figure 3. VBI Decoder Functional Blocks**

VBI data will be captured and stored in the internal buffer and accessible through corresponding registers. The data in the buffer will be output in the next horizontal blanking interval of the data capture. The VBI data will be multiplexed together with the luma data so that they are sharing the same y-out port at the AL240. The VBI data can be retrieved from the multiplexed data based on the v-count signal from AL240. For example, the US Close Caption will be at Line21. Hence by enabling the VBI US Close Caption Register for Line21, the VBI data will be captured when  $(v\text{-count} + 5) = 21$  and the result will be available at the y-out port when  $(v\text{-count} + 5) = 22$ . Each of the VBI will have 5-byte header followed by the VBI data. The following table summarized the various VBI data type support by AL240.

**VBI Data Type Supported by the AL240 VBI Decoder**

| VBI Data Type         | Data Amplitude (IRE) | Starting Time (μsec) | Sample Rate (MHz) | Data Rate (Mb/sec) | Run-In Clock                                | Start Code               | Valid VBI Data Line                                                 | Data Length (Excluding Start Code or Frame Code) |
|-----------------------|----------------------|----------------------|-------------------|--------------------|---------------------------------------------|--------------------------|---------------------------------------------------------------------|--------------------------------------------------|
| US Closed Caption     | 50 ± 2<br>0 ± 2      | 10.50±0.500          | 0.5035            | 0.5035             | 7 – Cycle Sinewave                          | 001b                     | Line 21, 284 for NTSC                                               | 2-byte                                           |
| EURO Closed Caption   | 50 ± 2<br>0 ± 2      | 10.50±0.500          | 0.5000            | 0.5000             | 7 – Cycle Sinewave                          | 001b                     | Line 18, 281 for PAL M<br>line 22, 335 for PAL B, D, G, H, I, N, CN | 2-byte                                           |
| Teletext 625A         | -                    | 10.50±0.32           | 6.203125          | 6.203125           | 1010 1010 1010<br>1010b                     | Programmable (11100111b) | Programmable                                                        | 37-byte                                          |
| Teletext 625B/ WST625 | 66 ± 2<br>0 ± 2      | 13.874               | 6.9375            | 6.9375             | -                                           | Programmable (11100100b) | Programmable                                                        | 42-byte                                          |
| Teletext 625C         | 70, 100<br>0         | 10.48±0.34           | 5.734375          | 5.734375           | 1010 1010 1010<br>1010b                     | Programmable (11100111b) | Programmable                                                        | 33-byte                                          |
| Teletext 625D         | 70 ± 2.5<br>0 ± 2.5  | 10.5-10.97           | 5.6427875         | 5.6427875          | 1010 1010 1010<br>1010b                     | Programmable (11100101b) | Programmable                                                        | 34-byte                                          |
| Teletext 525B/ WST525 | 70 ± 2<br>0 ± 2      | 11.70±0.175          | 5.7272            | 5.7272             | -                                           | Programmable (11100100b) | Programmable                                                        | 34-byte                                          |
| Teletext 525C/ NABTS  | 70, 100<br>0         | 10.48±0.340          | 5.7272            | 5.7272             | 1010 1010 1010<br>1010b                     | Programmable (11100111b) | Programmable                                                        | 33-byte                                          |
| Teletxt 525D          | 70 ± 2.5<br>0 ± 2.5  | 9.78±0.350           | 5.7272            | 5.7272             | 1010 1010 1010<br>1010b                     | Programmable (11100101b) | Programmable                                                        | 34-byte                                          |
| WSS625                | 500mV±5%<br>0mV±5%   | 11.00±0.250          | 5                 | 0.8333 (fs/6)      | 1 1111 0001<br>1100 0111 0001<br>1100 0111b | IE3C1Fh                  | Line 17, 280 for PAL M<br>Line 23, 336 for PAL B, D, G, H, I, N, CN | 14-bit (~2-byte)                                 |
| WSSJ                  | -                    | 11.20±0.3            | 0.447             | 0.447              | -                                           | 10b                      | Line 20, 283 for NTSC                                               | 20-bit (~3-byte)                                 |

## 8.9 Serial Bus Interface

The AL240 registers can be accessed via a two-wire (serial data SDA and serial clock SCL) serial bus, which is industrial I<sup>2</sup>C standard compliant. Each device connected to this serial bus is recognized by a unique address and can operate as a transmitter or receiver. The device on the bus that initiates and terminates a transfer called master, and the device on the bus that is addressed by the master called slave. The AL240 chip acts as a slave device and responses command from master device, such as micro-controller, to do the register update and feedback correspondingly.

The AL240 chip has two pins, SEL0 and SEL1, to select up to 4 different access addresses. By setting up different configuration on these two pins, that allows AL240 chip to select the write/read access addresses among 24h/25h, 26h/27h, 28h/29h or 2Ah/2Bh. This can be very useful for the design requires multiple AL240 chips. Table below summarizes the selections of write/read addresses.

| SEL1:SEL0 | Write Address | Read Address |
|-----------|---------------|--------------|
| 00:       | 24H           | 25H          |
| 01:       | 26H           | 27H          |
| 10:       | 28H           | 29H          |
| 11:       | 2AH           | 2BH          |

The serial interface, SCL (serial clock) and SDA (serial data) signals must be pull high to a positive supply voltage via a resistor. Data transfer rate on the bus can be up to 400 Kbits/s. The read/write command format is as follows:

**Write:** <S> <Write SA> <A> <Register Index> <A> <Data> <A> <P>

**Read:** <S> <Write SA> <A> <Register Index> <A> <S> <Read SA> <A> <Data>  
<NA> <P>

Following are the details:

<S>: Start signal

| SCL  | SDA         |
|------|-------------|
| High | High to Low |

The Start signal appears at High to Low transition on the SDA line when SCL is High.

<Write SA>: Write Slave Address

The Write Slave Address is 20h, 22h, 24h or 26h,

<Read SA>: Read Slave Address

The Read Slave Address is 21h, 22h, 25h or 27h.

<Register Index>: Value of the AL240 register index.

<A>: Acknowledge stage

The host (master) generates acknowledge-related clock pulse. During the acknowledge clock pulse, the host must release the SDA line (to High) in order that AL240 (slave) can pull down the SDA.

<NA>: Non-Acknowledged stage

The host (master) generates acknowledge-related clock pulse. The host also releases the SDA line (to High) during the acknowledge clock pulse, but the AL240 does not pull it down during this stage.

<Data>: Data byte written to or read from the register index

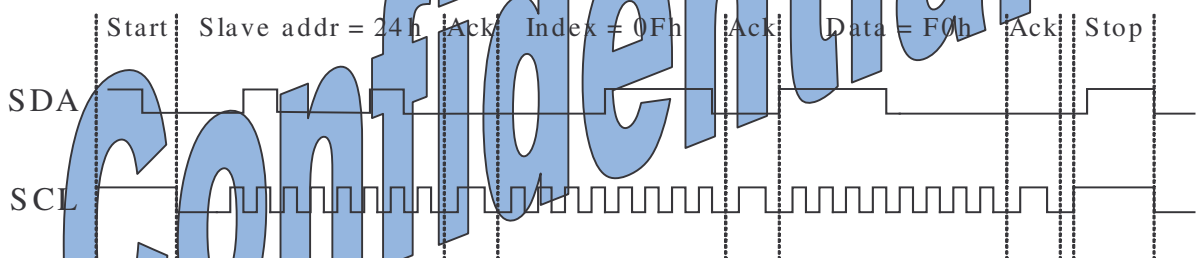
In read operation, the host must release the SDA line (to High) before the first clock pulse is transmitted to the AL240.

<P>: Stop signal

| SCL  | SDA         |
|------|-------------|
| High | Low to High |

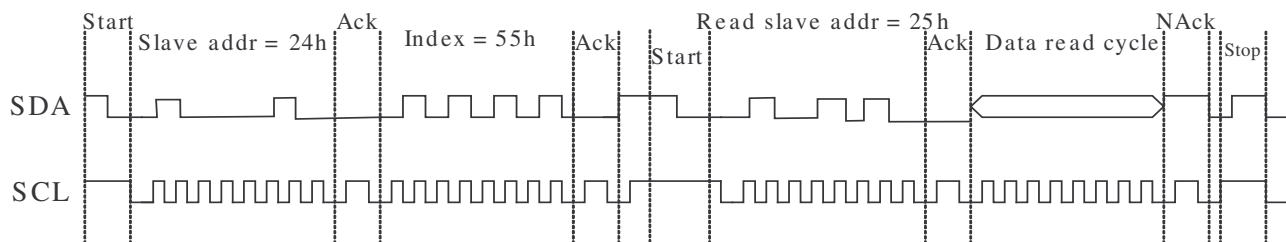
The Stop signal appears at Low to High transition on the SDA line when SCL is High.

Suppose data F0h is to be written to register 0Fh using write slave address 24h, the timing is as follows:



**Figure 4: Two-wire Serial Bus Write Timing**

Suppose data is to be read from register 55h using read slave address 25h, the timing is as follows:



**Figure 5: Two-wire Serial Bus Read Timing**

## 8.10 Output Format

The AL240 supports 8-bit YCbCr 4:2:2 digital formats along with LLC (27Mhz) line-lock clocks for output. The ITU-R BT.656 standard is embedded in output data.

The internal output format control register needs to be set for proper output. The register value vs. output format and corresponding output bus interface are described in the following tables.

| Register Value<br>B1h<3:0> | Output                                                                  |
|----------------------------|-------------------------------------------------------------------------|
| 000x                       | ITU-R BT. 656 (8-bit. hsync & vsync can be output from RTSO[4:0] pins). |

And corresponding data output mapping is indicated as following.

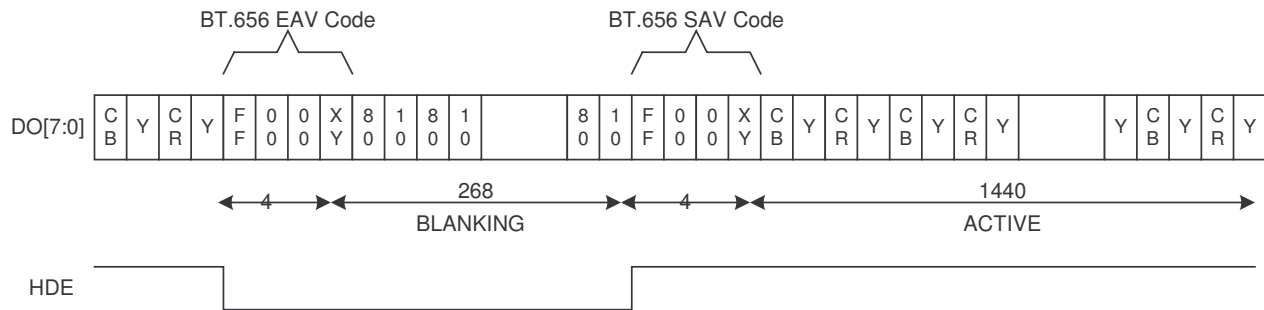
**DO[7:0] Input/Output Pin Mappings**

| Pin # | 656 output |
|-------|------------|
| 12    | YCbCr7     |
| 13    | YCbCr 6    |
| 14    | YCbCr 5    |
| 15    | YCbCr 4    |
| 19    | YCbCr 3    |
| 20    | YCbCr 2    |
| 21    | YCbCr 1    |
| 22    | YCbCr 0    |
| 36    | RTSO[4]    |
| 37    | RTSO[3]    |
| 27    | RTSO[2]    |
| 26    | RTSO[1]    |
| 25    | RTSO[0]    |

Table below is the output video standard and their specification.

| STANDARDS       | LINE RATE (KHz) | PIXEL TOTAL PER LINE | ACTIVE PIXEL PER LINE | PIXEL CLOCK RATE |
|-----------------|-----------------|----------------------|-----------------------|------------------|
| NTSC (M, 4.43)  | 15.73426        | 858                  | 720                   | 27               |
| PAL (B,D,G,H,I) | 15.625          | 864                  | 720                   | 27               |
| PAL (M)         | 15.73426        | 858                  | 720                   | 27               |
| PAL (N)         | 15.625          | 864                  | 720                   | 27               |
| SECAM           | 15.625          | 864                  | 720                   | 27               |

The 8-bit ITU-R BT.656 output format is indicated by the following figure,



**Figure 6: ITU-R.BT656 Timing reference codes**

Each timing reference code consists of a four word sequence in the following format: FF 00 00 XY (in hexadecimal notation). Codes “FF 00 00” are fixed preamble of timing code and fourth byte contains timing information as defined in following,

Where,

F (Field): 0 – filed 1; 1 – filed 2

V (Blanking): 0 – elsewhere; 1 – during filed blanking

H (SAV/EAV): 0 – in SAV; 1 – in EAV

P0, P1, P2, P3: Protection bits

| XY bit number | 7     | 6 | 5 | 4 | 3  | 2  | 1  | 0  |
|---------------|-------|---|---|---|----|----|----|----|
| Function      | Fixed | F | V | H | P3 | P2 | P1 | P0 |
| 0             | 1     | 0 | 0 | 0 | 0  | 0  | 0  | 0  |
| 1             | 1     | 0 | 0 | 1 | 1  | 1  | 0  | 1  |
| 2             | 1     | 0 | 1 | 0 | 1  | 0  | 1  | 1  |
| 3             | 1     | 0 | 1 | 1 | 0  | 1  | 1  | 0  |
| 4             | 1     | 1 | 0 | 0 | 0  | 1  | 1  | 1  |
| 5             | 1     | 1 | 0 | 1 | 1  | 0  | 1  | 0  |
| 6             | 1     | 1 | 1 | 0 | 1  | 1  | 0  | 0  |
| 7             | 1     | 1 | 1 | 1 | 0  | 0  | 0  | 1  |

## 9 Register Definition

### 9.1 Register Set

| Register Name | Address   | R/W | Default | Description                        |
|---------------|-----------|-----|---------|------------------------------------|
| CTRL0         | 00h       | R/W | 00h     | System configuration 0             |
| CTRL1         | 01h       | R/W | 01h     | System configuration 1             |
| CTRL2         | 02h       | R/W | 4Eh     | AGC configuration                  |
| YCSEPCTRL     | 03h       | R/W | 00h     | YC separation control              |
| HAGC          | 04h       | R/W | DDh     | Luma AGC target value              |
| NOISETH       | 05h       | R/W | 32h     | Noise threshold                    |
| ADCSWAP       | 06h       | R/W | 00h     | ADC swap                           |
| OUTPUTCTRL    | 07h       | R/W | A0h     | Output control                     |
| LUMAC         | 08h       | R/W | 80h     | Luma contrast adjustment           |
| LUMAB         | 09h       | R/W | 20h     | Luma brightness adjustment         |
| CHROMAS       | 0Ah       | R/W | 80h     | Chroma saturation adjustment       |
| CHROMAHPHASE  | 0Bh       | R/W | 00h     | Chroma Hue adjustment              |
| CHROMAAGC     | 0Ch       | R/W | 8Ah     | Chroma AGC target value            |
| CHROMAKILL    | 0Dh       | R/W | 07h     | Chroma kill control                |
| CHROMAPOS     | 0Fh       | R/W | 2Ch     | Chroma auto position control       |
| AGCPEAKNOM    | 10h       | R/W | 0Ah     | For manufacture use only           |
| AGCPEAKCTRL   | 11h       | R/W | 09h     | For manufacture use only           |
| BLUESCRY      | 12h       | R/W | 10h     | Blue screen Y value                |
| BLUESCRCB     | 13h       | R/W | B4h     | Blue screen Cb value               |
| BLUESCRCR     | 14h       | R/W | 80h     | Blue screen Cr value               |
| HDETCLAMPLV   | 15h       | R/W | 20h     | For manufacture use only           |
| LOCKCOUNT     | 16h       | R/W | 04h     | For manufacture use only           |
| HLOOPMAX      | 17h       | R/W | 0Bh     | For manufacture use only           |
| CHROMADTOINC  | 18h~1Bh   | R/W | 00h     | Chroma DTO increment [29:0]        |
| HSYNCDTOINC   | 1Ch ~ 1Fh | R/W | 00h     | For manufacture use only           |
| HSYNCTIME     | 20h       | R/W | 3Eh     | For manufacture use only           |
| HSYNCOFFSET   | 21h       | R/W | 3Eh     | For manufacture use only           |
| HSYNCSTART    | 22h       | R/W | 00h     | For manufacture use only           |
| HSYNCEND      | 23h       | R/W | 80h     | For manufacture use only           |
| HSYNCRISSTART | 26h       | R/W | 2Dh     | For manufacture use only           |
| HSYNCRISEND   | 27h       | R/W | 50h     | For manufacture use only           |
| HSYNCFLTSTART | 2Ah       | R/W | D6h     | For manufacture use only           |
| HSYNCFLTEND   | 2Bh       | R/W | 4Eh     | For manufacture use only           |
| CHROMASTART   | 2Ch       | R/W | 32h     | For manufacture use only           |
| CHROMAEND     | 2Dh       | R/W | 46h     | For manufacture use only           |
| HACTIVESTART  | 2Eh       | R/W | 82h     | Active video horizontal start time |
| HACTIVEWIDTH  | 2Fh       | R/W | 50h     | Active video horizontal width      |
| VACTIVESTART  | 30h       | R/W | 22h     | Active video vertical start time   |
| VACTIVEHEIGHT | 31h       | R/W | 61h     | Active video vertical height       |

|              |         |     |     |                                                  |
|--------------|---------|-----|-----|--------------------------------------------------|
| VSYNCHMIN    | 32h     | R/W | F0h | For manufacture use only                         |
| VSYNCHMAX    | 33h     | R/W | 0Eh | For manufacture use only                         |
| VYSNCAGCMIN  | 34h     | R/W | EC  | For manufacture use only                         |
| VYSNCAGCMAX  | 35h     | R/W | 10h | For manufacture use only                         |
| VSYNVCBIMIN  | 36h     | R/W | F0h | For manufacture use only                         |
| VSYNVCBIMAX  | 37h     | R/W | 0Eh | For manufacture use only                         |
| VYSNCCTRL    | 38h     | R/W | 40h | For manufacture use only                         |
| VSYNTIMECNT  | 39h     | R/W | 0Ah | Vsync time constant                              |
| STATUS1      | 3Ah     | R   | 00h | Status register 1                                |
| STATUS2      | 3Bh     | R   | 00h | Status register 2                                |
| STATUS3      | 3Ch     | R   | 00h | Status register 3                                |
| MUXANALOG    | 3Dh     | R/W | 00h | For manufacture use only                         |
| MUXDIGITAL   | 3Eh     | R/W | 00h | For manufacture use only                         |
| SOFTTRST     | 3Fh     | W   | 01h | Soft reset                                       |
| VBICODECTRL  | 40h     | R/W | 04h | Teletext VBI frame code control                  |
| VBISTARTCODE | 41h     | R/W | 00h | Teletext VBI Frame code                          |
| VBIDATAHL    | 42h     | R/W | 00h | VBI data high level                              |
| VBILINE7     | 43h     | R/W | 00h | VBI data type configuration for line 7           |
| VBILINE8     | 44h     | R/W | 00h | VBI data type configuration for line 8           |
| VBILINE9     | 45h     | R/W | 00h | VBI data type configuration for line 9           |
| VBILINE10    | 46h     | R/W | 00h | VBI data type configuration for line 10          |
| VBILINE11    | 47h     | R/W | 00h | VBI data type configuration for line 11          |
| VBILINE12    | 48h     | R/W | 00h | VBI data type configuration for line 12          |
| VBILINE13    | 49h     | R/W | 00h | VBI data type configuration for line 13          |
| VBILINE14    | 4Ah     | R/W | 00h | VBI data type configuration for line 14          |
| VBILINE15    | 4Bh     | R/W | 00h | VBI data type configuration for line 15          |
| VBILINE16    | 4Ch     | R/W | 00h | VBI data type configuration for line 16          |
| VBILINE17    | 4Dh     | R/W | 00h | VBI data type configuration for line 17          |
| VBILINE18    | 4Eh     | R/W | 00h | VBI data type configuration for line 18          |
| VBILINE19    | 4Fh     | R/W | 00h | VBI data type configuration for line 19          |
| VBILINE20    | 50h     | R/W | 00h | VBI data type configuration for line 20          |
| VBILINE21    | 51h     | R/W | 00h | VBI data type configuration for line 21          |
| VBILINE22    | 52h     | R/W | 00h | VBI data type configuration for line 22          |
| VBILINE23    | 53h     | R/W | 00h | VBI data type configuration for line 23          |
| VBILINE24    | 54h     | R/W | 00h | VBI data type configuration for remaining lines  |
| VBILINE25    | 55h     | R/W | 00h | VBI data type configuration for remaining lines  |
| VBILINE26    | 56h     | R/W | 00h | VBI data type configuration for remaining lines  |
| VBIIGAIN0    | 57h     | R/W | 00h | VBI loop filter gain for close-caption& teletext |
| VBIIGAIN1    | 58h     | R/W | 00h | VBI loop filter gain for wss625                  |
| CCDTOINC     | 59h&5Ah | R/W | 00h | DTO incremental value for close-caption clock    |

|                |         |     |     |                                                           |
|----------------|---------|-----|-----|-----------------------------------------------------------|
|                |         |     |     | recovery circuit                                          |
| TELDTOINC      | 5Bh&5Ch | R/W | 00h | DTO incremental value for teletext clock recovery circuit |
| WSSDTOINC      | 5Dh&5Eh | R/W | 00h | DTO incremental value for wss625 clock recovery circuit   |
| CCFSTART       | 5Fh     | R/W | 00h | Frame start for the close caption                         |
| WSSFSTART      | 60h     | R/W | B4h | Frame start for wss625                                    |
| TELFSTART      | 61h     | R/W | 00h | Frame start for TELETEXT                                  |
| CCDATA1        | 62h     | R   | 00h | Close captioning data byte 1                              |
| CCDATA2        | 63h     | R   | 00h | Close captioning data byte 2                              |
| VBINOISETH     | 64h     | R/W | 00h | Noise level for the VBI line                              |
| VBISTATUS      | 65h     | R   | 00h | VBI data status                                           |
| CCSTART        | 66h     | R/W | 00h | Close caption start                                       |
| WSSSTART       | 67h     | R/W | 64h | WSS625 start                                              |
| TELSTART       | 68h     | R/W | 5Ah | Teletext start                                            |
| HSSTART        | 69h     | R/W | 01h | Output hsync start position                               |
| HSWIDTH        | 6Ah     | R/W | 40h | Output hsync width                                        |
| VSSTART        | 6Bh     | R/W | 01h | Output vsync start line                                   |
| VSWIDTH        | 6Ch     | R/W | 04h | Output vsync width                                        |
| WSSDATA2       | 6Dh     | R   | 00h | Wide screen signaling data byte 2                         |
| WSSDATA1       | 6Eh     | R   | 00h | Wide screen signaling data byte 1                         |
| WSSDATA0       | 6Fh     | R   | 00h | Wide screen signaling data byte 0                         |
| HSDTOINCSTATUS | 70h~73h | R   | 00h | Hsync DTO increment status                                |
| CSDTOINCSTATUS | 74h~77h | R   | 00h | Chrom DTO increment status                                |
| AGCSTATUS      | 78h&79  | R   | 00h | AGC gain value                                            |
| CMAGSTAUS      | 7Ah     | R   | 00h | Chroma magnitude                                          |
| CGAINSTATUS    | 7Bh&7Ch | R   | 00h | Chroma gain                                               |
| CORDICFSTATUS  | 7Dh     | R   | 00h | SECAM cordic frequency                                    |
| NOISESTATUS    | 7Fh     | R   | 00h | Noise status                                              |
| COMBFLTTH      | 80h     | R/W | 04h | Comb filter threshold                                     |
| COMBFLTCONFIG  | 82h     | R/W | 42h | Comb filter configuration                                 |
| CHROLKCONFIG   | 83h     | R/W | 6Fh | For manufacture use only                                  |
| COMBFLTTH1     | 84h     | R/W | 07h | For manufacture use only                                  |
| COMBFLTTH2     | 85h     | R/W | 20h | For manufacture use only                                  |
| COMBFLTTH3     | 86h     | R/W | 03h | For manufacture use only                                  |
| COMBFLTTH4     | 87h     | R/W | 10h | For manufacture use only                                  |
| CHROLOOPFLT    | 8Ah     | R/W | 0Ah | For manufacture use only                                  |
| CHROHRECTRL    | 8Bh     | R/W | 01h | For manufacture use only                                  |
| CPUMPDLYCTRL   | 8Dh     | R/W | 28h | For manufacture use only                                  |
| CPUMPADJUST    | 8Eh     | R/W | C8h | For manufacture use only                                  |
| CPUMPDLY       | 8Fh     | R/W | B9h | For manufacture use only                                  |
| VERSION        | B0h     | R   | 42h | Chip version                                              |
| OFORMAT        | B1h     | R/W | 10h | Digital output format control                             |

|                |        |     |     |                                                                                                                                                                                                                                           |
|----------------|--------|-----|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RTSO[0]&TSTPAT | B2h    | R/W | 02h | Control RTSO[0] output signal as Hsync, Vsync, Field or others. Default output signal for RTSO[0] is Hsync signal.                                                                                                                        |
| RTSO[1]        | B3h    | R/W | 03h | Control RTSO[1] output signal as Hsync, Vsync, Field or others. Default output signal for RTSO[1] is Vsync signal.                                                                                                                        |
| RTSO[2]        | B4h    | R/W | 04h | Control RTSO[2] output signal as Hsync, Vsync, Field or others. Default output signal for RTSO[2] is Field signal.                                                                                                                        |
| RTSO[3]        | B5h    | R/W | 07h | Control RTSO[3] output signal as Hsync, Vsync, Field or others. Default output signal for RTSO[0] is “Hactive ANDs Vactive” signal.                                                                                                       |
| RTSO[4]        | B6h    | R/W | 08h | Control RTSO[4] output signal as Hsync, Vsync, Field or others. Default output signal for RTSO[4] is VBI valid signal.                                                                                                                    |
| AFEIN&FSW      | B7h[4] | R/W | 00h | Selects four analog inputs AI0, AI1, AI2 and AI3 for the combinations of 4 CVBS, 2 S-video, 2 CVBS/1 S-video or 1 YPbPr inputs. And enable FSW0 and FSW1 Hardware switching control signals output from RTSO[3] and RTSO[4] respectively. |
| PLLCTRL 0      | B8h    | R/W | 00h | PLL enable/power down and LLC circuit divider values                                                                                                                                                                                      |
| PLLCTRL1       | B9h    | R/W | 22h | For manufacture use only                                                                                                                                                                                                                  |
| PLLCTRL2       | BAh    | R/W | 10h | PLL feedback divider settings                                                                                                                                                                                                             |
| LLCDTOINC 3    | BBh    | R/W | 38h | LLC DTO increment value <31:24>                                                                                                                                                                                                           |
| LLCDTOINC 2    | BCh    | R/W | E3h | LLC DTO increment value <23:16>                                                                                                                                                                                                           |
| LLCDTOINC 1    | BDh    | R/W | 8Eh | LLC DTO increment value <15:8> (unused)                                                                                                                                                                                                   |
| LLCDTOINC 0    | BEh    | R/W | 38h | LLC DTO increment value <7:0> (unused)                                                                                                                                                                                                    |
| FIFOGAIN       | BFh    | R/W | 03h | 4 bit <3:0> FIFO gain level adjustment<br>Max: 8<br>Min: 0<br>For FIFO level > 8: Fixed DTO, LLC output frequency depend on the value of registers BBh and BCh                                                                            |
| DCRSTOCTRL 0   | C0h    | R/W | D4h | DC restore circuit filter and gain control                                                                                                                                                                                                |
| DCRSTOCTRL 1   | C1h    | R/W | 1Bh | DC restore circuit accumulate width adjustment                                                                                                                                                                                            |
| MANUALGAIN     | C2h    | R/W | 40h | Manual Gain adjustment                                                                                                                                                                                                                    |
| PBKILLTH       | C3h    | R/W | C0h | For manufacture use only                                                                                                                                                                                                                  |
| DCRSTOHMID     | C4h    | R/W | 7h  | Set the horizontal mid-point used to reset the DC-restore accumulators.                                                                                                                                                                   |
| MINSYNCEHEIGHT | C5h    | R/W | 10h | For manufacture use only                                                                                                                                                                                                                  |
| SLEWCTRL       | C8h    | R/W | 51h | For manufacture use only                                                                                                                                                                                                                  |

|                |           |     |             |                                                                            |
|----------------|-----------|-----|-------------|----------------------------------------------------------------------------|
| SLEWINC        | C9h ~ CBh | R/W | 3126EA<br>h | For manufacture use only                                                   |
| SLEWPERIOD     | CCh       | R/W | 10h         | For manufacture use only                                                   |
| SLEWPOLTH      | CDh       | R/W | C8h         | For manufacture use only                                                   |
| FIFOLEVEL      | D0h       | R   |             | Output data FIFO level status; Read only value around 0x80h while DTO lock |
| AFETSTMODCTRL1 | D2h       | R/W | 10h         | For manufacture use only                                                   |
| AFETSTMODCTRL2 | D3h       | R/W | FC          | For manufacture use only                                                   |
| DATASWAP       | D4h       | R/W | 00h         | Output data swap                                                           |
| YCGAIN         | D5h       | R/W | 05h         | Adjust PGA amplifier gain level                                            |
| WRITEENABLE    | FEh       | R/W | 00h         | Register write enable                                                      |

## 9.2 Register Description

### INDEX Register Description

| (HEX) | Register Name | BITS | Function Description |
|-------|---------------|------|----------------------|
|-------|---------------|------|----------------------|

#### Standard Control Register

| 00 | System Configuration 0 (R/W) [CTRL0] |  |  |
|----|--------------------------------------|--|--|
|----|--------------------------------------|--|--|

|             |       |                                                                                                                                                                                                                                        |
|-------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| yc_src      | <0>   | Input video format<br>0 Composite (default)<br>1 S-Video (separated Y/C)                                                                                                                                                               |
| colour_mode | <3:1> | Video color standard<br>000 NTSC (default)<br>001 PAL (I,B,G,H,D,N)<br>010 PAL (M)<br>011 PAL (CN)<br>100 SECAM                                                                                                                        |
| vline_625   | <4>   | The number of scan lines per frame<br>0 525 (default)<br>1 625                                                                                                                                                                         |
| hpixel      | <6:5> | Output display format<br>00 NTSC, PAL(M); 858 pixels/line (default)<br>01 PAL(B,D,G,H,I,CN), SECAM; 864 pixels/line<br>10 NTSC Square Pixel, PAL(M) Square Pixel; 780 pixels/line<br>11 PAL(B,D,G,H,I,N) Square Pixel; 944 pixels/line |
| hv_delay    | <7>   | Emulate the HV-delay found on Sony studio monitor<br>0 Disabled (default)                                                                                                                                                              |

1 Enabled

## 01 System Configuration 1 (R/W) [CTRL1]

|                  |       |                                                                        |
|------------------|-------|------------------------------------------------------------------------|
| ped              | <0>   | Enables black level correction for 7.5 blank-to-blank setup (pedestal) |
|                  | 0     | No pedestal subtraction                                                |
|                  | 1     | Pedestal subtraction (default)                                         |
| chroma_burst5to1 | <1>   | The burst gate width                                                   |
|                  | 0     | 5 subcarrier clock cycles (default)                                    |
|                  | 1     | 10 subcarrier clock cycles                                             |
| chroma_bw_lo     | <3:2> | Chroma low pass filter to wide or narrow                               |
|                  | 00    | Narrow                                                                 |
|                  | 01    | Wide                                                                   |
|                  | 10    | Extra wide                                                             |
| luma_notcha_bw   | <5:4> | Luma notch width                                                       |
|                  | 00    | None (default)                                                         |
|                  | 01    | Narrow                                                                 |
|                  | 10    | Medium                                                                 |
|                  | 11    | Wide                                                                   |
| Reserved         | <7:6> | Default '000' for normal operation                                     |

## 02 AGC Configuration (R/W) [CTRL2]

|               |       |                                                                                                                        |
|---------------|-------|------------------------------------------------------------------------------------------------------------------------|
| hagc_en       | <0>   | The luma/composite AGC enable. If disabled, then the AGC target (Register 04h) is used to drive the AGC gain directly. |
|               | 0     | Off                                                                                                                    |
|               | 1     | On (default)                                                                                                           |
| cagc_en       | <1>   | The chroma AGC enables. If disabled, then the AGC target is used to drive the AGC gain directly.                       |
|               | 0     | Off                                                                                                                    |
|               | 1     | On (default)                                                                                                           |
| agc_half_en   | <2>   | The half gain mode enable, when unlocked, for the analog front end.                                                    |
|               | 0     | Off                                                                                                                    |
|               | 1     | On (default)                                                                                                           |
| dagc_en       | <3>   | The digital AGC enable. The digital AGC is used in series with the analog gain.                                        |
|               | 0     | Off                                                                                                                    |
|               | 1     | On (default)                                                                                                           |
| dc_clamp_mode | <5:4> | The analog front end DC clamping mode                                                                                  |
|               | 00    | Auto; use backporch when a signal exists; use syntip if no signal exists (default)                                     |
|               | 01    | Backporch only                                                                                                         |
|               | 10    | Syntip only                                                                                                            |

|            |     |                                                                                                          |                                                           |
|------------|-----|----------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|
| mv_hagc    | <6> | 11                                                                                                       | Off                                                       |
|            |     | Automatically reduces the gain (set in Register 4) by 25% when macro-vision encoded signals are detected |                                                           |
| hagc_field | <7> | 0                                                                                                        | Off                                                       |
|            |     | 1                                                                                                        | On (default)                                              |
|            |     | The gain update                                                                                          |                                                           |
|            |     | 0                                                                                                        | Off (default); updated once per line after DC clamping    |
|            |     | 1                                                                                                        | On; updated once per field at the start of vertical blank |

### YC-Separation Control Registers

#### 03 YC Separation Control (R/W) [YCSEPCTRL]

|               |       |                                                                                                                                                |                                                                     |
|---------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|
| adaptive_mode | <2:0> | Composite signal's Y/C separation adaptive mode before color demodulation.                                                                     |                                                                     |
|               |       | 000                                                                                                                                            | Fully adaptive (default)                                            |
|               |       | 001                                                                                                                                            | Vertical adaptive (vertical only)                                   |
|               |       | 010                                                                                                                                            | 5-tap adaptive comb filter (PAL mode only)                          |
|               |       | 011                                                                                                                                            | Basic luma notch filter mode (for very noisy and unstable pictures) |
|               |       | 100                                                                                                                                            | Simple 2-tap comb                                                   |
|               |       | 101                                                                                                                                            | Simple 3-tap comb                                                   |
|               |       | 110                                                                                                                                            | 5-tap hybrid adaptive comb filter (PAL mode only)                   |
| colour_trap   | <3>   | Enables the notch-filter at the luma path after the comb filter. This filter can be turned on or off irrespective of the adaptive mode setting |                                                                     |
|               |       | 0                                                                                                                                              | Disabled (default)                                                  |
|               |       | 1                                                                                                                                              | Enabled                                                             |
| Reserved      | <7:4> | Reserved                                                                                                                                       |                                                                     |

### Horizontal Acquisition Registers

#### 04 Luma AGC Value (R/W) [HAGC]

|      |       |                                                                                                                 |                          |
|------|-------|-----------------------------------------------------------------------------------------------------------------|--------------------------|
| hagc | <7:0> | Luma AGC target value. The gain of the AGC is modified until the horizontal sync height is equal to this value. |                          |
|      |       | <u>Standard</u>                                                                                                 | <u>Programming Value</u> |
|      |       | NTSC M                                                                                                          | DDh (221d) (default)     |
|      |       | NTSC J                                                                                                          | CDh (205d)               |
|      |       | PAL B,D,G,H,I, COMB N, SECAM                                                                                    | DCh (220d)               |
|      |       | PAL M,N                                                                                                         | DDh (221d)               |
|      |       | NTSC M (MACROVISION)                                                                                            | A6h (166d)               |

PAL B,D,G,H,I, COMB N AEh (174d)  
(MACROVISION)

Note:

- When a MacroVision signal is detected, luma AGC target value is automatically reduced by 25%.
- If “hagc\_en” (02h<0>) is “0”, then “hagc” is used to directly drive the analog gain. In this case, a value of 64 represents a unity gain, 32 represents a one-half gain, and 128 denotes a double gain.

#### 05 Noise Threshold (R/W) [NOISETH]

|              |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| noise_thresh | <7:0> | <p>This value sets the noise value at which the circuit considers a signal noisy. The detected noise value may be read back through register 7Fh (“status_noise”). If the detected noise value is greater than “noise_thresh”, then register 3Ch&lt;3&gt; (“noisy”) is set. Larger values of “status_noise” indicate noisier signals, so larger values of “noise_thresh” decreases the likelihood of “noisy” being set while smaller values of “noise_thresh” increases the likelihood of “noisy” being set.</p> <p>(default = 32h)</p> |
|--------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

#### 06 ADC Swap (R/W) [ADCSWAP]

|                   |       |                                                                                                                 |
|-------------------|-------|-----------------------------------------------------------------------------------------------------------------|
| Reserved          | <4:0> | Reserved                                                                                                        |
| adc_cbr_pump_swap | <5>   | <p>Swap the Pb/Pr charge pump pairs to the analog front-end</p> <p>0 Disabled (default)</p> <p>1 Enabled</p>    |
| adc_input_swap    | <6>   | <p>Swap the MSBs and LSBs from the analog front-end's ADC</p> <p>0 Disabled (default)</p> <p>1 Enabled</p>      |
| adc_updn_swap     | <7>   | <p>Swap the DC clamp up/down controls to the analog front-end.</p> <p>0 Disabled (default)</p> <p>1 Enabled</p> |

### Output Control Register

#### 07 Output Control (R/W) [OUTPUTCTRL]

|          |       |                                                                                                                                                                                                                             |
|----------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| yc_delay | <3:0> | <p>This 2's complement number controls the output delay between luma and chroma. Negative values shift luma outputs to the left while positive values shift luma values to the right. The range is [-5, 7]. Default = 0</p> |
|----------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

|           |       |                            |
|-----------|-------|----------------------------|
| blue-mode | <5:4> | Blue screen mode control   |
|           | 00    | Disabled                   |
|           | 01    | Enabled                    |
|           | 10    | Auto (default)             |
|           | 11    | Reserved                   |
| cbr_swap  | <6>   | Swap Cb/Cr output          |
|           | 0     | Don't swap Cb/Cr (default) |
|           | 1     | Swap Cb/Cr                 |
| Reserved  | <7>   | Reserve                    |

### Luma Adjustment Registers

#### 08 Luma Contrast Adjustment (R/W) [LUMAC]

|          |       |                                                                 |
|----------|-------|-----------------------------------------------------------------|
| contrast | <7:0> | The adjustable gain to the luma output path.<br>(default = 80h) |
|----------|-------|-----------------------------------------------------------------|

#### 09 Luma Brightness Adjustment (R/W) [LUMAB]

|            |       |                                                                                                                                                                                                          |
|------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| brightness | <7:0> | The adjustable brightness level to the luma output path. This value is offset by -32, i.e., a value of 32 (default) implies a brightness level of 0, and a value of 0 implies a brightness level of -32. |
|------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

### Chroma Adjustment Registers

#### 0A Chroma Saturation Adjustment (R/W) [CHROMAS]

|            |       |                                                   |
|------------|-------|---------------------------------------------------|
| saturation | <7:0> | Color saturation adjustment value (default = 80h) |
|------------|-------|---------------------------------------------------|

#### 0B Chroma Hue Phase Adjustment (R/W) [CHROMAHPHASE]

|     |       |                                                                        |
|-----|-------|------------------------------------------------------------------------|
| hue | <7:0> | This 2's complement number adjusts the hue phase offset (default = 0h) |
|-----|-------|------------------------------------------------------------------------|

#### 0C Chroma AGC (R/W) [CHROMAAGC]

|      |       |                                   |
|------|-------|-----------------------------------|
| cagc | <7:0> | Chroma AGC target (default = 8Ah) |
|------|-------|-----------------------------------|

#### 0D Chroma Kill (R/W) [CHROMAKILL]

|                |       |                                                                            |
|----------------|-------|----------------------------------------------------------------------------|
| chroma_kill    | <3:0> | Chroma kill level (default = 7h)                                           |
| hlock_kill     | <4>   | When set, chroma is killed whenever horizontal lock is lost (default = 0h) |
| vbi_kill       | <5>   | When set, chroma is killed during VBI (default = 0h)                       |
| user_kill_mode | <7:6> | User chroma kill mode                                                      |
|                | 00    | Auto hardware chroma kill (default)                                        |
|                | 01    | Forces chroma kill on                                                      |
|                | 10    | Forces chroma off                                                          |

---

**0F Chroma Autoposition (R/W) [CHROMAPOS]**


---

|                 |       |                                                                                                                                                                                        |
|-----------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| cautopos        | <4:0> | The chroma burst gate position relative to the auto centre position (default = 0Ch)                                                                                                    |
| fixed_burstgate | <5>   | When set, this bit disables the burst gate autoposition. The manual burstgate window position is defined by the burst_gate_start(2Ch) and burst_gate_end(2Dh) register. (default = 1h) |
|                 | <7:6> | Reserved                                                                                                                                                                               |

**Blue Screen**


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**12 Blue Screen Y (R/W) [BLUESCRY]**


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|               |       |                                                                                                      |
|---------------|-------|------------------------------------------------------------------------------------------------------|
| blue_screen_y | <7:0> | This register controls the blue screen (no video) luma value. The range is [16,235]. (default = 10h) |
|---------------|-------|------------------------------------------------------------------------------------------------------|

---

**13 Blue Screen Cb (R/W) [BLUESCRCB]**


---

|                |       |                                                                                                          |
|----------------|-------|----------------------------------------------------------------------------------------------------------|
| blue_screen_cb | <7:0> | This register controls the blue screen (no video) Cb chroma value. The range is [16,240] (default = B4h) |
|----------------|-------|----------------------------------------------------------------------------------------------------------|

---

**14 Blue screen Cr (R/W) [BLUESCRCR]**


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|                |       |                                                                                                            |
|----------------|-------|------------------------------------------------------------------------------------------------------------|
| blue_screen_cr | <7:0> | This registers controls the blue screen (no video) Cr chroma value. The range is [16,240]. (default = 80h) |
|----------------|-------|------------------------------------------------------------------------------------------------------------|

**Chroma DTO Registers**

Note: Following formula applies to determine the setting values of chroma DTO registers,

$$cdto\_inc = 4f_{SC} / f_{INPUT} \times 2^{30}, \text{ where } f_{SC} \text{ is the chroma sub-carrier frequency}$$

Where,

$f_{INPUT}$ : is 20Mhz input clock

$4f_{SC}$  is sub-carrier frequency. And their corresponding frequencies in different standard are,

| Standard        | $4f_{SC}$ (Mhz) |
|-----------------|-----------------|
| NTSC 3.58       | 14.31818182     |
| NTSC 4.43       | 17.734475       |
| PAL B,D,G,H,I,N | 17.734475       |
| PAL M           | 14.30244596     |
| PAL CN          | 14.328225       |
| SECAM           | 17.144          |

---

**18 Chroma DTO Increment [29:24] (R/W) [CHROMADTOINC]**


---

|          |       |                                                    |
|----------|-------|----------------------------------------------------|
| cdto_inc | <5:0> | These bits contain bits [29:24] of the 30-bit-wide |
|----------|-------|----------------------------------------------------|

|               |                                                         |                                                                                                                                                                                                                                                     |                      |
|---------------|---------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
|               |                                                         |                                                                                                                                                                                                                                                     | chroma DTO increment |
| Reserved      | <6>                                                     | Reserved                                                                                                                                                                                                                                            |                      |
| cdto_fixed    | <7>                                                     | Fixes the chroma DTO at its centre frequency                                                                                                                                                                                                        |                      |
|               |                                                         | 0                                                                                                                                                                                                                                                   | Disabled (default)   |
|               |                                                         | 1                                                                                                                                                                                                                                                   | Enabled              |
| 19            | Chroma DTO Increment [23:16] (R/W) [CHROMADTOINC]       |                                                                                                                                                                                                                                                     |                      |
| cdto_inc      | <7:0>                                                   | BitS <23:16> of 30-bit-wide chroma DTO increment                                                                                                                                                                                                    |                      |
| 1A            | Chroma DTO Increment [15:8] (R/W) [CHROMADTOINC]        |                                                                                                                                                                                                                                                     |                      |
| cdto_inc      | <7:0>                                                   | Bit <15:8> of 30-bit-wide chroma DTO increment                                                                                                                                                                                                      |                      |
| 1B            | Chroma DTO Increment [7:0] (R/W) [CHROMADTOINC]         |                                                                                                                                                                                                                                                     |                      |
| cdto_inc      | <7:0>                                                   | Bit <7:0> of 30-bit-wide chroma DTO increment                                                                                                                                                                                                       |                      |
| 2E            | Active Video Horizontal Start Time (R/W) [ACTIVEHSTART] |                                                                                                                                                                                                                                                     |                      |
| hactive_start | <7:0>                                                   | This bits control the active video line time interval. This specifies the beginning of active line. This register is used to centre the horizontal position, and should <i>not</i> be used to crop the image to a smaller size. (default = 82h)     |                      |
| 2F            | Active Video Horizontal Width (R/W) [HACTIVEWIDTH]      |                                                                                                                                                                                                                                                     |                      |
| hactive_width | <7:0>                                                   | The active video line time interval control. It specifies the width of the active line, and should <i>not</i> be used to crop the image to a smaller size. The value 640 is added to this register. (default = 50h (80) $\Rightarrow$ 640+80 = 720) |                      |

### Vertical Sync and Field Detection Registers

|                |                                                    |                                                                                                                                                                                           |  |
|----------------|----------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| 30             | Active Video Vertical Start (R/W) [VACTIVESTART]   |                                                                                                                                                                                           |  |
| vactive_start  | <7:0>                                              | Controls the first active video line in a field. It specifies the number of half-lines from the start of a field. (default = 22h)                                                         |  |
| 31             | Active Video Vertical Height (R/W) [VACTIVEHEIGHT] |                                                                                                                                                                                           |  |
| vactive_height | <7:0>                                              | The active video height control. It specifies the height by the number of half-lines. The value 384 is added to this register. (default = 61h (97) $\Rightarrow$ 97+394 = 481 half-lines) |  |

---

39 Vsync Time Constant (R/W) [VSYNC TIMECNT]

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|                   |       |                                                                                      |
|-------------------|-------|--------------------------------------------------------------------------------------|
| vloop_tc          | <1:0> | Vertical PLL time constant                                                           |
|                   | 00    | Fast. Only useful if the vloop_cntl register is not 11. Internal values are 2 and 1. |
|                   | 01    | Moderate. Internal values are 1 and 1/4.                                             |
|                   | 10    | Slow. Internal values are 1/2 and 1/16 (default)                                     |
|                   | 11    | Very slow. Most useful for noisy signals. Internal values are 1/4 and 1/2.           |
| field_detect_mode | <3:2> | The field detection logic control. (default = 2)                                     |
| vodd_delayed      | <4>   | Delays detection of odd field by 1 vertical line                                     |
|                   | 0     | Disabled (default)                                                                   |
|                   | 1     | Enabled                                                                              |
| veven_delayed     | <5>   | Delays detection of even field by 1 vertical line                                    |
|                   | 0     | Disabled (default)                                                                   |
|                   | 1     | Enabled                                                                              |
| flip_field        | <6>   | Flips even/odd fields                                                                |
|                   | 0     | Disabled                                                                             |
|                   | 1     | Enabled                                                                              |
| field_polarity    | <7>   | Output field polarity                                                                |
|                   | 0     | Field = 1 for odd fields, field = 0 for even fields (default)                        |
|                   | 1     | Field = 0 for odd fields, field = 1 for even fields                                  |

---

3A Status Register 1 (R) [STATUS1]

---

|            |       |                                  |
|------------|-------|----------------------------------|
| no_signal  | <0>   | No signal detection              |
|            | 0     | Signal detected                  |
|            | 1     | No signal detected               |
| hlock      | <1>   | Horizontal line locked           |
|            | 0     | Unlocked                         |
|            | 1     | Locked                           |
| vlock      | <2>   | Vertical lock                    |
|            | 0     | Unlocked                         |
|            | 1     | Locked                           |
| chromalock | <3>   | Chroma PLL locked to color burst |
|            | 0     | Unlocked                         |
|            | 1     | Locked                           |
| Reserved   | <7:4> | Reserved                         |

---

3B Status Register 2 (R) [STATUS2]

---

|                  |       |                           |
|------------------|-------|---------------------------|
| proscan_detected | <0>   | Progressive scan detected |
|                  | 0     | Undetected                |
|                  | 1     | Detected                  |
| Reserved         | <7:1> | Reserved                  |

**3C Status Register 3 (R) [STATUS3]**

|                   |     |                                                                                                                                                                   |
|-------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PAL_detected      | <0> | PAL Color Mode detected                                                                                                                                           |
| SECAM_detected    | <1> | SECAM Color Mode detected                                                                                                                                         |
| 625lines_detected | <2> | 625 Scan Lines detected                                                                                                                                           |
| noisy             | <3> | Noisy signal detected. It is set when the detected noisy value (status register 7Fh) is greater than the value programmed into the “noise_thresh” register (05h). |
| vcr               | <4> | VCR detected                                                                                                                                                      |
| vcr_trick         | <5> | VCR Trick-Mode detected                                                                                                                                           |
| vcr_ff            | <6> | VCR Fast-Forward detected                                                                                                                                         |
| vcr_rew           | <7> | VCR Rewind detected                                                                                                                                               |

**Reset Register**
**3F Reset Register (W) [SOFTRST]**

|          |       |                    |
|----------|-------|--------------------|
| soft_rst | <0>   | Soft Reset         |
|          |       | 0 Normal operation |
|          |       | 1 Software reset   |
| Reserved | <7:1> | Reserved           |

**VBI Decoder Registers**
**40 Teletext VBI Frame Code Register (R/W) [VBICODECTRL]**

|                    |       |                                                                                                                                                                                                       |
|--------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| vbi_en             | <0>   | VBI decoder enable                                                                                                                                                                                    |
|                    |       | 0 Off (default)                                                                                                                                                                                       |
|                    |       | 1 On                                                                                                                                                                                                  |
| vbi_st_err_ignored | <1>   | When this is “1”, it will allow one bit error in the start code detection. When this bit is “0”, all the start-code-bits must be correct during VBI line detection                                    |
|                    |       | 0 Off (default)                                                                                                                                                                                       |
|                    |       | 1 On                                                                                                                                                                                                  |
| adap_slvl_en       | <2>   | Adaptive slicer enables. When it is enabled, the slicer level is determined by the built-in adaptive slicer generator. When is disabled, the slicer level is specified in the vbi_data_hlvl register. |
|                    |       | 0 Off                                                                                                                                                                                                 |
|                    |       | 1 On (default)                                                                                                                                                                                        |
| Reserved           | <7:3> | Reserved                                                                                                                                                                                              |

**41 Teletext VBI Frame Code Register (R/W) [VBISTARTCODE]**

|            |       |                                                              |
|------------|-------|--------------------------------------------------------------|
| Start_code | <7:0> | The Frame Code used in the teletext for byte synchronization |
|------------|-------|--------------------------------------------------------------|

|    |                                                                    |                                                                                           |
|----|--------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| 42 | Data High Level Register (R/W) [VBIDATAHL]                         |                                                                                           |
|    | vbi_data_hlvl                                                      | <7:0> The VBI data high level                                                             |
| 43 | VBI Data Type Configuration Register For Line 7 (R/W) [VBILINE7]   |                                                                                           |
|    | vbi7o                                                              | <3:0> Set VBI data type for odd field                                                     |
|    | vbi7e                                                              | <7:4> Set VBI data type for even field (Line 270 for 525 system. Line 320 for 625 system) |
| 44 | VBI Data Type Configuration Register for Line 8 (R/W) [VBILINE8]   |                                                                                           |
|    | vbi8o                                                              | <3:0> Set VBI data type for odd field                                                     |
|    | vbi8e                                                              | <7:4> Set VBI data type for even field (Line 271 for 525 system. Line 321 for 625 system) |
| 45 | VBI Data Type Configuration Register for Line 9 (R/W) [VBILINE9]   |                                                                                           |
|    | vbi9o                                                              | <3:0> Set VBI data type for odd field                                                     |
|    | vbi9e                                                              | <7:4> Set VBI data type for even field (Line 272 for 525 system. Line 322 for 625 system) |
| 46 | VBI Data Type Configuration Register for Line 10 (R/W) [VBILINE10] |                                                                                           |
|    | vbi10o                                                             | <3:0> Set VBI data type for odd field                                                     |
|    | vbi10e                                                             | <7:4> Set VBI data type for even field (Line 273 for 525 system. Line 323 for 625 system) |
| 47 | VBI Data Type Configuration register Line 11 (R/W) [VBILINE11]     |                                                                                           |
|    | vbi11o                                                             | <3:0> Set VBI data type for odd field                                                     |
|    | vbi11e                                                             | <7:4> Set VBI data type for even field (Line 274 for 525 system. Line 324 for 625 system) |
| 48 | VBI Data Type Configuration register Line 12 (R/W) [VBILINE12]     |                                                                                           |
|    | vbi12o                                                             | <3:0> Set VBI data type for odd field                                                     |
|    | vbi12e                                                             | <7:4> Set VBI data type for even field (Line 275 for 525 system. Line 325 for 625 system) |
| 49 | VBI Data Type Configuration register Line 13 (R/W) [VBILINE13]     |                                                                                           |
|    | vbi13o                                                             | <3:0> Set VBI data type for odd field                                                     |
|    | vbi13e                                                             | <7:4> Set VBI data type for even field (Line 276 for 525 system. Line 326 for 625 system) |
| 4A | VBI Data Type Configuration register Line 14 (R/W) [VBILINE14]     |                                                                                           |
|    | vbi14o                                                             | <3:0> Set VBI data type for odd field                                                     |
|    | vbi14e                                                             | <7:4> Set VBI data type for even field (Line 277 for 525 system. Line 327 for 625 system) |
| 4B | VBI Data Type Configuration register Line 15 (R/W) [VBILINE15]     |                                                                                           |
|    | vbi15o                                                             | <3:0> Set VBI data type for odd field                                                     |

|    |                                                                            |       |                                                                                     |
|----|----------------------------------------------------------------------------|-------|-------------------------------------------------------------------------------------|
|    | vbi15e                                                                     | <7:4> | Set VBI data type for even field (Line 278 for 525 system. Line 328 for 625 system) |
| 4C | VBI Data Type Configuration register Line 16 (R/W) [VBILINE16]             |       |                                                                                     |
|    | vbi16o                                                                     | <3:0> | Set VBI data type for odd field                                                     |
|    | vbi16e                                                                     | <7:4> | Set VBI data type for even field (Line 279 for 525 system. Line 329 for 625 system) |
| 4D | VBI Data Type Configuration register Line 17 (R/W) [VBILINE17]             |       |                                                                                     |
|    | vbi17o                                                                     | <3:0> | Set VBI data type for odd field                                                     |
|    | vbi17e                                                                     | <7:4> | Set VBI data type for even field (Line 280 for 525 system. Line 330 for 625 system) |
| 4E | VBI Data Type Configuration register Line 18 (R/W) [VBILINE18]             |       |                                                                                     |
|    | vbi18o                                                                     | <3:0> | Set VBI data type for odd field                                                     |
|    | vbi18e                                                                     | <7:4> | Set VBI data type for even field (Line 281 for 525 system. Line 331 for 625 system) |
| 4F | VBI Data Type Configuration register Line 19 (R/W) [VBILINE19]             |       |                                                                                     |
|    | vbi19o                                                                     | <3:0> | Set VBI data type for odd field                                                     |
|    | vbi19e                                                                     | <7:4> | Set VBI data type for even field (Line 282 for 525 system. Line 332 for 625 system) |
| 50 | VBI Data Type Configuration register Line 20 (R/W) [VBILINE20]             |       |                                                                                     |
|    | vbi20o                                                                     | <3:0> | Set VBI data type for odd field                                                     |
|    | vbi20e                                                                     | <7:4> | Set VBI data type for even field (Line 283 for 525 system. Line 333 for 625 system) |
| 51 | VBI Data Type Configuration register Line 21 (R/W) [VBILINE21]             |       |                                                                                     |
|    | vbi21o                                                                     | <3:0> | Set VBI data type for odd field                                                     |
|    | vbi21e                                                                     | <7:4> | Set VBI data type for even field (Line 284 for 525 system. Line 334 for 625 system) |
| 52 | VBI Data Type Configuration register Line 22 (R/W) [VBILINE22]             |       |                                                                                     |
|    | vbi22o                                                                     | <3:0> | Set VBI data type for odd field                                                     |
|    | vbi22e                                                                     | <7:4> | Set VBI data type for even field (Line 285 for 525 system. Line 335 for 625 system) |
| 53 | VBI Data Type Configuration register Line 23 (R/W) [VBILINE23]             |       |                                                                                     |
|    | vbi23o                                                                     | <3:0> | Set VBI data type for odd field                                                     |
|    | vbi23e                                                                     | <7:4> | Set VBI data type for even field (Line 286 for 525 system. Line 336 for 625 system) |
| 54 | VBI Data Type Configuration register for remaining lines (R/W) [VBILINE24] |       |                                                                                     |
|    | vbi24o                                                                     | <3:0> | Set VBI data type for odd field                                                     |

|    |                                                                            |        |                                                                                                                                  |
|----|----------------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------|
|    | vbi124e                                                                    | <7:4>  | Set VBI data type for even field (line 287 for 525 system, line 338 for 625 system)                                              |
| 55 | VBI Data Type Configuration register for remaining lines (R/W) [VBILINE25] |        |                                                                                                                                  |
|    | vbi125o                                                                    | <3:0>  | Set VBI data type for odd field                                                                                                  |
|    | vbi125e                                                                    | <7:4>  | Set VBI data type for even field (line 288 for 525 system, line 338 for 625 system)                                              |
| 56 | VBI Data Type Configuration register for remaining lines (R/W) [VBILINE26] |        |                                                                                                                                  |
|    | vbi126o                                                                    | <3:0>  | Set VBI data type for the lines in the odd field except line 7 to line 25                                                        |
|    | vbi126e                                                                    | <7:4>  | Set VBI data type for all the lines in the even field except lines 270 to 288 for 525 system, or lines 329 to 338 for 625 system |
| 57 | VBI Loop Filter I Gain Register 0 (R/W) [VBIIGAIN0]                        |        |                                                                                                                                  |
|    | vbi_cc_lpfil_gain                                                          | <23:0> | Loop filter gain for close-caption<br>Recommend Setting: Close Caption = 6<br>Gemstar Close Caption = 5                          |
|    | Reserved                                                                   | <3>    | Reserved                                                                                                                         |
|    | vbi_tele_lpfil_gain                                                        | <6:4>  | Loop filter gain for teletext                                                                                                    |
| 58 | VBI Loop Filter I Gain Register 1 (R/W) [VBIIGAIN1]                        |        |                                                                                                                                  |
|    | vbi_wss625_lpfil_gain                                                      | <2:0>  | Loop filter gain for wss625                                                                                                      |
|    | Reserved                                                                   | <7:3>  | Reserved                                                                                                                         |
| 59 | Upper Byte VBI Close Caption DTO Register (R/W) [CCDTOINC]                 |        |                                                                                                                                  |
|    | vbi_caption_dto                                                            | <7:0>  | Bit <15:8> of the 16-bit DTO incremental value for close-caption clock recovery circuit.                                         |
| 5A | Lower Byte VBI Close Caption DTO Register (R/W) [CCDTOINC]                 |        |                                                                                                                                  |
|    | vbi_caption_dto                                                            | <7:0>  | Bit <7:0> of the 16-bit DTO incremental value for close-caption clock recovery circuit                                           |
| 5B | Upper Byte VBI Teletext DTO Register (R/W) [TELDTOINC]                     |        |                                                                                                                                  |
|    | vbi_teletext_dto                                                           | <7:0>  | Bits<15:8> of the 16-bit DTO incremental value for teletext clock recovery circuit.<br>(default = 12DBh)                         |
| 5C | Lower Byte VBI Teletext DTO Register (R/W) [TELDTOINC]                     |        |                                                                                                                                  |
|    | vbi_teletext_dto                                                           | <7:0>  | Bits<7:0> of 16-bit DTO incremental value for teletext clock recovery circuit                                                    |

| 5D                                                                                                                                                                                                                                                                                                                                                                                               | Upper Byte VBI WSS625/WSSJ DTO Register (R/W) [WSSDTOINC]                                                                                                                                |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------------------|----------|-----|----------|-----|----------|-----|----------|-----|----------|-----|----------|-----|----------|-----|
| vbi_wss625_dto                                                                                                                                                                                                                                                                                                                                                                                   | <7:0> Bits<15:8> of 16-bit DTO incremental value for wss625 or wssj clock recovery circuit.                                                                                              |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| 5E                                                                                                                                                                                                                                                                                                                                                                                               | Lower Byte VBI WSS625/WSSJ DTO Register (R/W) [WSSDTOINC]                                                                                                                                |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| vbi_wss625_dto                                                                                                                                                                                                                                                                                                                                                                                   | <7:0> Bits<7:0> of 16-bit DTO incremental value for wss625/wssj clock recovery circuit.                                                                                                  |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| 5F                                                                                                                                                                                                                                                                                                                                                                                               | VBI Close Caption Data 1 Register (R/W) [CCFSTART]                                                                                                                                       |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| caption_frame_start                                                                                                                                                                                                                                                                                                                                                                              | <7:0> The frame start for the close caption                                                                                                                                              |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| 60                                                                                                                                                                                                                                                                                                                                                                                               | VBI Close Caption Data 1 Register (R/W) [WSSFSTART]                                                                                                                                      |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| wss625_frame_start                                                                                                                                                                                                                                                                                                                                                                               | <7:0> The frame start for the wss625 or wssj Recommend Setting: wss625 = B4h (default)                                                                                                   |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| 61                                                                                                                                                                                                                                                                                                                                                                                               | VBI Close Caption Data 1 Register (R/W) [TELFSTART]                                                                                                                                      |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| teletext_frame_start                                                                                                                                                                                                                                                                                                                                                                             | <7:0> The frame start for the TELETEXT                                                                                                                                                   |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| <table> <thead> <tr> <th>Standard</th><th>Programming Value</th></tr> </thead> <tbody> <tr> <td>TELE625A</td><td>34h</td></tr> <tr> <td>TELE625B</td><td>34h</td></tr> <tr> <td>TELE625C</td><td>34h</td></tr> <tr> <td>TELE625D</td><td>34h</td></tr> <tr> <td>TELE525B</td><td>35h</td></tr> <tr> <td>TELE525C</td><td>35h</td></tr> <tr> <td>TELE525D</td><td>35h</td></tr> </tbody> </table> |                                                                                                                                                                                          | Standard | Programming Value | TELE625A | 34h | TELE625B | 34h | TELE625C | 34h | TELE625D | 34h | TELE525B | 35h | TELE525C | 35h | TELE525D | 35h |
| Standard                                                                                                                                                                                                                                                                                                                                                                                         | Programming Value                                                                                                                                                                        |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| TELE625A                                                                                                                                                                                                                                                                                                                                                                                         | 34h                                                                                                                                                                                      |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| TELE625B                                                                                                                                                                                                                                                                                                                                                                                         | 34h                                                                                                                                                                                      |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| TELE625C                                                                                                                                                                                                                                                                                                                                                                                         | 34h                                                                                                                                                                                      |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| TELE625D                                                                                                                                                                                                                                                                                                                                                                                         | 34h                                                                                                                                                                                      |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| TELE525B                                                                                                                                                                                                                                                                                                                                                                                         | 35h                                                                                                                                                                                      |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| TELE525C                                                                                                                                                                                                                                                                                                                                                                                         | 35h                                                                                                                                                                                      |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| TELE525D                                                                                                                                                                                                                                                                                                                                                                                         | 35h                                                                                                                                                                                      |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| 62                                                                                                                                                                                                                                                                                                                                                                                               | VBI Close Caption Data 1 Register (R) [CCDATA1]                                                                                                                                          |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| ccddata1                                                                                                                                                                                                                                                                                                                                                                                         | <7:0> Close caption data byte 1                                                                                                                                                          |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| 63                                                                                                                                                                                                                                                                                                                                                                                               | VBI Close Caption Data 2 Register (R) [CCDATA2]                                                                                                                                          |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| ccddata2                                                                                                                                                                                                                                                                                                                                                                                         | <7:0> Close caption data byte 2                                                                                                                                                          |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| 64                                                                                                                                                                                                                                                                                                                                                                                               | VBI Close Caption Data 1 Register (R/W) [VBINOISETH]                                                                                                                                     |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| vbi_noise_th                                                                                                                                                                                                                                                                                                                                                                                     | <7:0> The noise level for the VBI line thus anything below the threshold is zero for data slicing. It specified the lowest level of the adaptive slicer level when there is no VBI data. |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| 65                                                                                                                                                                                                                                                                                                                                                                                               | VBI Data Status Register (R) [VBISTATUS]                                                                                                                                                 |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |
| cc_rdy                                                                                                                                                                                                                                                                                                                                                                                           | <0> Close caption data register data. This bit is set to 1 if both CCDATA registers contain the valid close                                                                              |          |                   |          |     |          |     |          |     |          |     |          |     |          |     |          |     |

|    |                                                 |                 |                                                                                                                                                                                                                   |
|----|-------------------------------------------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                                                 |                 | caption data. This bit will be reset to 0 during system reset. It will also be cleared at the beginning of a new field.                                                                                           |
|    | wss_rdy                                         | <1>             | WSS data register data valid. This bit is set to 1 if all the WSS registers contain the valid WSS data. This bit will be reset to 0 during system reset. It will also be cleared at the beginning of a new field. |
|    | Reserved                                        | <7:2>           | Reserved                                                                                                                                                                                                          |
| 66 | VBI Caption Start Register (R/W) [CCSTART]      |                 |                                                                                                                                                                                                                   |
|    | caption_start                                   | <7:0>           | Close caption start. The unit is hcount value.                                                                                                                                                                    |
| 67 | VBI WSS625/WSSJ Start Register (R/W) [WSSSTART] |                 |                                                                                                                                                                                                                   |
|    | wss625_start                                    | <7:0>           | Wide screen signaling 625 or WSSJ/CGMS start. The Unit is hcount value.<br>Recommend Setting: WSS625 = 64h (default)<br>WSSJ = 5Ah                                                                                |
| 68 | VBI Teletext Start Register (R/W) [TELSTART]    |                 |                                                                                                                                                                                                                   |
|    | teletext_start                                  | <7:0>           | Teletext start. The unit is hcount value. (default = 5Ah)                                                                                                                                                         |
|    |                                                 | <u>Standard</u> | <u>Programming Value</u>                                                                                                                                                                                          |
|    |                                                 | TELE625A        | 32h                                                                                                                                                                                                               |
|    |                                                 | TELE625B        | 32h                                                                                                                                                                                                               |
|    |                                                 | TELE625C        | 32h                                                                                                                                                                                                               |
|    |                                                 | TELE625D        | 32h                                                                                                                                                                                                               |
|    |                                                 | TELE525B        | 28h                                                                                                                                                                                                               |
|    |                                                 | TELE525C        | 28h                                                                                                                                                                                                               |
|    |                                                 | TELE525D        | 28h                                                                                                                                                                                                               |
| 69 | Horizontal Sync Start (R/W) [HSSTART]           |                 |                                                                                                                                                                                                                   |
|    | hs_start                                        | <7:0>           | Bits<7:0> of output Hsync starting point                                                                                                                                                                          |
| 6A | Horizontal Sync Width (R/W) [HSWIDTH]           |                 |                                                                                                                                                                                                                   |
|    | hs_width                                        | <7:0>           | Bits<7:0> of output Hsync width                                                                                                                                                                                   |
| 6B | Vertical Sync Start (R/W) [VSSTART]             |                 |                                                                                                                                                                                                                   |
|    | vs_start                                        | <7:0>           | Bits<7:0> of output Vsync starting line                                                                                                                                                                           |
| 6C | Vertical Sync Width (R/W) [VSWIDTH]             |                 |                                                                                                                                                                                                                   |
|    | vs_width                                        | <7:0>           | Bits<7:0> of output Vsync width                                                                                                                                                                                   |
| 6D | VBI WSS Data 2 Register (R) [WSSDATA2]          |                 |                                                                                                                                                                                                                   |

|    |                                                           |       |                                                           |
|----|-----------------------------------------------------------|-------|-----------------------------------------------------------|
|    | wssdata2                                                  | <7:0> | Wide screen signaling data (WSSJ) byte 2                  |
| 6E | VBI WSS Data 1 Register (R) [WSSDATA1]                    |       |                                                           |
|    | wssdata1                                                  | <7:0> | Wide screen signaling data (WSS625/WSSJ) byte 1           |
| 6F | VBI WSS Data 0 Register (R) [WSSDATA0]                    |       |                                                           |
|    | wssdata0                                                  | <7:0> | Wide screen signaling data (WSS625/WSSJ) byte 0           |
| 70 | Horizontal Sync DTO Increment Status (R) [HSDTOINCSTATUS] |       |                                                           |
|    | status_hdto_inc                                           | <5:0> | Bits<29:24> of 30-bit-wide horizontal sync DTO increment. |
|    | Reserved                                                  | <7:6> | Reserved                                                  |
| 71 | Horizontal Sync DTO Increment Status (R) [HSDTOINCSTATUS] |       |                                                           |
|    | status_hdto_inc                                           | <7:0> | Bits<23:16> of 30-bit-wide horizontal sync DTO increment. |
| 72 | Horizontal sync DTO Increment Status (R) [HSDTOINCSTATUS] |       |                                                           |
|    | status_hdto_inc                                           | <7:0> | Bits<15:8> of 30-bit-wide horizontal sync DTO increment.  |
| 73 | Horizontal Sync DTO Increment Status (R) [HSDTOINCSTATUS] |       |                                                           |
|    | status_hdto_inc                                           | <7:0> | Bits<7:0> of 30-bit-wide horizontal sync DTO increment.   |
| 74 | Chroma Sync DTO Increment Status (R) [CSDTOINCSTATUS]     |       |                                                           |
|    | status_cdto_inc                                           | <5:0> | Bits<29:24> of the 30-bit-wide chroma sync DTO increment. |
|    | Reserved                                                  | <7:6> | Reserved                                                  |
| 75 | Chroma Sync DTO Increment Status (R) [CSDTOINCSTATUS]     |       |                                                           |
|    | status_cdto_inc                                           | <7:0> | Bits<23:16> of the 30-bit-wide chroma sync DTO increment. |
| 76 | Chroma Sync DTO Increment Status (R) [CSDTOINCSTATUS]     |       |                                                           |
|    | status_cdto_inc                                           | <7:0> | Bits<15:8> of the 30-bit-wide chroma sync DTO increment.  |
| 77 | Chroma Sync DTO Increment Status (R) [CSDTOINCSTATUS]     |       |                                                           |
|    | status_cdto_inc                                           | <7:0> | Bits<7:0> of the 30-bit-wide chroma sync DTO increment.   |
| 78 | AGC Gain Status MSB (R) [AGCSTATUS]                       |       |                                                           |
|    | status_agc_gain                                           | <7:0> | These bits contain the MSB of the AGC gain value.         |

|    |                                             |                                                                                                                                                                                          |
|----|---------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 79 | AGC Gain Status LSB (R) [AGCSTATUS]         |                                                                                                                                                                                          |
|    | status_agc_dgain                            | <7:0> These bits contain the LSB of the AGC gain value.                                                                                                                                  |
| 7A | Chroma Magnitude Status (R) [CMAGSTATUS]    |                                                                                                                                                                                          |
|    | status_cmag                                 | <7:0> This bits contain the chroma magnitude                                                                                                                                             |
| 7B | Chroma Gain Status MSB (R) [CGAINSTATUS]    |                                                                                                                                                                                          |
|    | status_cgain                                | <5:0> Bits<13:8> of the chroma gain                                                                                                                                                      |
|    | Reserved                                    | <7:6> Reserved                                                                                                                                                                           |
| 7C | Chroma Gain Status LSB (R) [CGAINSTATUS]    |                                                                                                                                                                                          |
|    | status_cgain                                | <7:0> Bits<7:0> of the chroma gain                                                                                                                                                       |
| 7D | Cordic Frequency Status (R) [CORDICFSTATUS] |                                                                                                                                                                                          |
|    | status_cordic_freq                          | <7:0> SECAM cordic frequency                                                                                                                                                             |
| 7F | Noise Status (R) [NOISESTATUS]              |                                                                                                                                                                                          |
|    | status_noise                                | <7:0> Indicates how noisy the signal is. Larger values indicate noisier signals. It is used in conjunction with programmable register 05h, "noise_thresh" and status bit 3C<3>h, "noisy" |

### Luma Peaking Register

|    |                                           |                                                                                                                                                                                        |
|----|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 80 | Comb Filter Threshold 1 (R/W) [COMBFLTTH] |                                                                                                                                                                                        |
|    | peak_en                                   | <0> The luma horizontal peaking control around the color subcarrier frequency<br>0 Disabled (default)<br>1 Enabled                                                                     |
|    | peak_gain                                 | <3:1> The gain for the horizontal peaking control. It allows adjustable gain to the luma around the color subcarrier frequency (default = 2).                                          |
|    | peak_range                                | <5:4> The range of peak_gain.<br>00 1 (default)<br>01 2<br>10 4<br>11 8<br>$Y_{peak} = Y + YH * (peak\_gain / peak\_range)$ where Y is the luma and YH is the high frequency luma only |
|    | Reserved                                  | <7:6> Reserved                                                                                                                                                                         |

## Adaptive Comb Filter Configuration Register

### 82 Comb Filter Configuration (R/W) [COMBFLTCONFIG]

|                  |       |                                                                                                                                                       |
|------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| palsw_level      | <1:0> | Used to determine how many incorrect lines are used for the PAL switch circuit before switching. Use a higher level for noisy signals. (default = 2h) |
| Reserved         | <3:2> | Reserved                                                                                                                                              |
| comb_wide_band   | <4>   | Used to select the bandpass filter used in the comb-filter. It should be set to 1 for PAL mode. (default = 0h)                                        |
| pal_perr_auto_en | <5>   | Turn on the pal_perr when VCR signals are detected.<br>0 Off (default)<br>1 On                                                                        |
| pal_perr         | <6>   | Used to reduce phase-error artifacts in the comb filter's luma-path. It should be set for VCR signals (default = 1).                                  |
| Reserved         | <7>   | Reserved                                                                                                                                              |

### B0 Chip Version (R) [VERSION]

|              |       |              |
|--------------|-------|--------------|
| Version      | <3:0> | Chip version |
| Fixed number | <7:4> | 4            |

### B1 Output Format Control (R/W) [OFORMAT]

|          |       |                                                                         |
|----------|-------|-------------------------------------------------------------------------|
| Oformat  | <3:0> | Output format & Test mode select                                        |
| YC_OE    | <4>   | DO[7:0] bus output enable control<br>0 Enable<br>1 Disable              |
| Reserved | <6:5> | Reserved                                                                |
| llc_inv  | <7>   | Invert llc output (default = 0)<br>0 LLC<br>1 LLC delayed by 180 degree |

### B2 RTSO[0] output enable (R/W) [RTSO[0]&TSTPAT]

|             |       |                                                      |
|-------------|-------|------------------------------------------------------|
| RTSO[0]_CTL | <4:0> | Control RTSO[0] output. It works when oformat<2> = 0 |
| Reserved    | <7:5> | Default '000' for normal operation                   |

### B3 RTSO[1] output control (R/W) [RTSO[1]]

|             |       |                                                      |
|-------------|-------|------------------------------------------------------|
| RTSO[1]_CTL | <4:0> | Control RTSO[1] output. It works when oformat[2] = 0 |
| Reserved    | <7:5> | Reserved                                             |

### B4 RTSO[2] output control (R/W) [RTSO[2]]

RTSO[2]\_CTL <4:0> Control RTSO[2] output. It works when oformat[2] = 0  
Reserved <7:5> Reserved

#### B5 RTSO[3] output control (R/W) [RTSO[3]]

RTSO[3]\_CTL <4:0> Control RTSO[3] output. It works when oformat[2] = 0  
Reserved <7:5> Reserved

#### B6 RTSO[4] output control (R/W) [RTSO[4]]

RTSO[4]\_CTL <4:0> Control RTSO[4] output. It works when oformat[2] = 0  
Reserved <7:5> Reserved

#### B7 AFE Input & Fast switch control (R/W) [AFEIN&FSW]

afe\_in\_sel <1:0> Afe\_in\_sel , and yc\_reg select analog input pins when hardware switching pin is disabled (B7h bit 3 fast\_sw = 0). The selections are:

| yc_src | afe_in_sel | Input pin name |
|--------|------------|----------------|
| 0      | 00         | AI0            |
| 0      | 01         | AI1            |
| 0      | 10         | AI2            |
| 0      | 11         | AI3            |
| 1      | 00         | AI0/AI2 (Y/C)  |
| 1      | 01         | AI1/AI3 (Y/C)  |

Note: for S-video input, set adaptive\_mode (03h<bit2:0>) to "011"

Reserved <2>  
Fast\_sw <3>

When this bit is set to '1', AL240 turns into "Hardware switch" mode. In this mode, AL240 assumes input sources are CVBS signals (CVBS1~4) and selected by FSW[1:0] pins  
0 Software switching for input  
1 FSW[1] and FSW[0] input switching control

Reserved <7:4> Reserved

#### PLL Registers

##### B8 PLL control 0 (R/W) [PLLCTRL0]

PLL\_OE <0> Output enable  
0 Normal operation  
1 No output  
PLL\_Pd <1> Power down PLL  
0 Normal operation  
1 Power down  
PLL\_Bp <2> Bypass PLL, i.e. fout = fin

|            |       |                           |                  |
|------------|-------|---------------------------|------------------|
|            |       | 0                         | Normal operation |
|            |       | 1                         | Bypass           |
| LLC_Divide | <6:3> | LLC circuit divider Value |                  |
| Reserved   | <7:4> | Reserved                  |                  |

**BA PLL control 2 (R/W) [PLLCTRL 2]**

|          |       |                          |              |
|----------|-------|--------------------------|--------------|
| PLL_NF   | <5:0> | Feedback divider setting |              |
| PLL_OD   | <6>   | Output divided by 2      |              |
|          |       | 0                        | No divided   |
|          |       | 1                        | Divided by 2 |
| Reserved | <7>   | Reserved                 |              |

**BB LLC DTO increment (R/W) [LLCDTOINC 3]**

|                    |       |                                |  |
|--------------------|-------|--------------------------------|--|
| llc_dto_inc[31:24] | <7:0> | LLC DTO increment bit <31: 24> |  |
|--------------------|-------|--------------------------------|--|

**BC LLC DTO increment (R/W) [LLCDTOINC 2]**

|                    |       |                                |  |
|--------------------|-------|--------------------------------|--|
| llc_dto_inc[23:16] | <7:0> | LLC DTO increment bit <23: 16> |  |
|--------------------|-------|--------------------------------|--|

**BD LLC DTO increment (R/W) [LLCDTOINC 1]**

|                   |       |                               |  |
|-------------------|-------|-------------------------------|--|
| llc_dto_inc[15:8] | <7:0> | LLC DTO increment bit <15: 8> |  |
|-------------------|-------|-------------------------------|--|

**BE LLC DTO increment (R/W) [LLCDTOINC 0]**

|                  |       |                              |  |
|------------------|-------|------------------------------|--|
| llc_dto_inc[7:0] | <7:0> | LLC DTO increment bit <7: 0> |  |
|------------------|-------|------------------------------|--|

**BF FIFO Gain Level (R/W) [FIFOGAIN]**

|                 |       |                                               |  |
|-----------------|-------|-----------------------------------------------|--|
| fifo_level_gain | <3:0> | Output data FIFO level gain adjustment <3: 0> |  |
|-----------------|-------|-----------------------------------------------|--|

**AFE Registers**
**C0 DC restore circuit control 0 (R/W) [DCRSTOCTRL 0]**

|                    |       |                                                                                 |                     |
|--------------------|-------|---------------------------------------------------------------------------------|---------------------|
| dcrestore_gain     | <1:0> | DC-restore gain                                                                 |                     |
|                    |       | 00:                                                                             | 1x gain (default)   |
|                    |       | 01:                                                                             | 1/2x gain           |
|                    |       | 10:                                                                             | 1/4x gain           |
|                    |       | 11:                                                                             | 1/8x gain           |
| syncmid_filter_en  | <2>   | Filtering of the sync mid-point                                                 |                     |
|                    |       | 0:                                                                              | no filter           |
|                    |       | 1:                                                                              | filter (default)    |
| syncmid_nobp_en    | <3>   | Sampling of sync mid-points when back-porches are not detected                  |                     |
|                    |       | 0:                                                                              | no sample (default) |
|                    |       | 1:                                                                              | sample              |
| dcrestore_bp_delay | <5:4> | Relative sync-tip to back-porch delay adjustment. The unit bits are adjusted in |                     |

|                     |                                                   |       |                                                                                                                                                                      |
|---------------------|---------------------------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                     |                                                   |       | “dcrestore_accum_width” (register 0Ch).<br>01: (default)                                                                                                             |
| dcrestore_kill_en   | <6>                                               |       | Sampling of bad back-porch values<br>0: don't kill; sample bad back-porches<br>1: kill; don't sample bad back-porches (default)                                      |
| dcrestore_no_bad_bp |                                                   |       | Use accumulated bad back-porch values<br>0: use accumulated bad back-porch values<br>1: don't use accumulated bad back-porch values (default)                        |
| <hr/>               |                                                   |       |                                                                                                                                                                      |
| C1                  | DC restore circuit control 1 (R/W) [DCRSTOCTRL 1] |       |                                                                                                                                                                      |
|                     | dcrestore_accum_w                                 | <5:0> | Number of samples to be accumulated when calculating the sync-tip and back-porch levels (default= 1Bh).                                                              |
|                     | dcrestore_scale_ratio                             | <7:6> | Scaling of the input signal to the DC-restore and sync-slicing sub-modules.<br>00: 1x (default)<br>01: 2x<br>02: 4x<br>03: reserved                                  |
| C2                  | Manual gain control (R/W) [MANUALGAIN]            |       |                                                                                                                                                                      |
|                     | hmgc                                              | <7:0> | Manual gain adjustment (hagc_en= 0, register 02h). A value of 64 represents a unit gain, 32 represent a one-half gain, and 128 denote a double gain. (default = 40h) |
| C4                  | DC restore hmid (R/W) [DCRSTOHMID]                |       |                                                                                                                                                                      |
|                     | dcrestore_hmid                                    | <7:0> | Set the horizontal mid-point used to reset the DC-restore accumulators. The 2's complement values is relative to the actual horizontal mid-point (default=7h)        |
| D0                  | FIFO level (R) [FIFOLEVEL]                        |       |                                                                                                                                                                      |
|                     | fifo_leve                                         | <7:0> | Output data FIFO level status                                                                                                                                        |
| D4                  | Data path swap (R/W) [DATASWAP]                   |       |                                                                                                                                                                      |
|                     | Reserved                                          | <1:0> |                                                                                                                                                                      |
|                     | cbcr_updn_swap                                    | <2>   | Swap CbCr up/dn signals                                                                                                                                              |
|                     | crupdn_swap                                       | <3>   | Swap crup/crdn signals                                                                                                                                               |
|                     | cbupdn_swap                                       | <4>   | Swap cbup/cbdn signals                                                                                                                                               |
|                     | yupdn_swap                                        | <5>   | Swap Yup/Ydn signals                                                                                                                                                 |
|                     | yc_digital_swap                                   | <6>   | Swap yadcddata[9:0] and cadcddata[9:0]. External MUX, outside AFE                                                                                                    |

**D5 Y/C Gain control (R/W) [YCGAIN]**

|       |       |                                                                                                                                                                                                                             |
|-------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| cgain | <1:0> | Adjusts PGA amplifier for C input gain level<br>00: 0.5x ; input level > 1.5V (Vp-p)<br>01: 1x; input level between 0.75V ~ 1.5V (Vp-p)<br>10: 2x; input level between 0.375V ~ 1.5V (Vp-p)<br>11: 4x; input level < 0.375V |
| ygain | <3:2> | Adjusts PGA amplifier for Y input gain level<br>00: 0.5x; input level > 1.5V (Vp-p)<br>01: 1x; input level between 0.75V ~ 1.5V (Vp-p)<br>10: 2x; input level between 0.375V ~ 1.5V (Vp-p)<br>11: 4x; input level < 0.375V  |

**FE Write enable (R/W) [WRITEENABLE]**

|              |       |                                                                     |
|--------------|-------|---------------------------------------------------------------------|
| write_enable | <7:0> | For registers write operation, set register Feh = FFh (default = 0) |
|--------------|-------|---------------------------------------------------------------------|

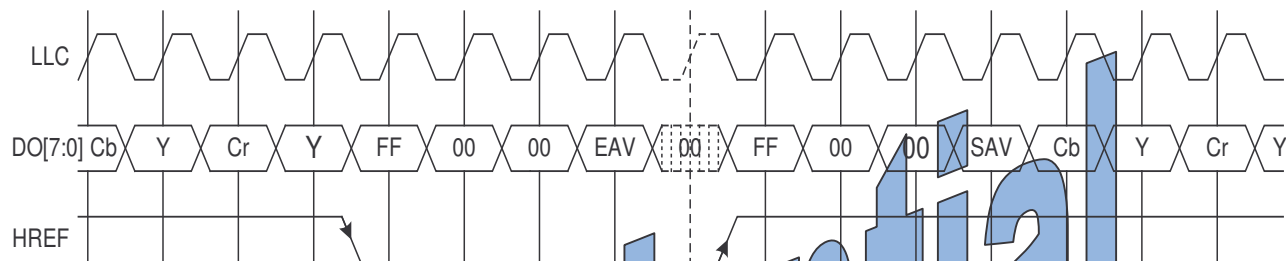
**9.3 Reference setting values**

| Register  | NTSC-M | NTSC-443 | PAL-I | PAL-M | PAL-CN | PAL-60 | SECAM |
|-----------|--------|----------|-------|-------|--------|--------|-------|
| RFE (Hex) | FF     | FF       | FF    | FF    | FF     | FF     | FF    |
| R00 (Hex) | 00     | 00       | 32    | 04    | 36     | 02     | 38    |
| R01 (Hex) | 01     | 01       | 00    | 00    | 00     | 00     | 00    |
| R02 (Hex) | 4E     | 4E       | 4E    | 4E    | 4E     | 4E     | 4E    |
| R03 (Hex) | 00     | 03       | 00    | 00    | 00     | 00     | 00    |
| R04 (Hex) | DD     | DD       | DC    | DD    | DC     | DC     | DC    |
| R07 (Hex) | 20     | 20       | 20    | 20    | 20     | 20     | 20    |
| R0C (Hex) | 8A     | 8A       | 67    | 67    | 67     | 67     | 67    |
| R0F (Hex) | 2C     | 2C       | 2C    | 2C    | 2C     | 2C     | 25    |
| R18 (Hex) | 2D     | 38       | 38    | 2D    | 2D     | 38     | 36    |
| R19 (Hex) | D1     | C0       | C0    | C4    | D9     | C0     | DC    |
| R1A (Hex) | 74     | 14       | 14    | 90    | AE     | 14     | 5D    |
| R1B (Hex) | 5D     | F8       | F8    | 50    | 92     | F8     | 63    |
| R1C (Hex) | 2B     | 2B       | 2B    | 2B    | 2B     | 2B     | 2B    |
| R1D (Hex) | 33     | 33       | 33    | 33    | 33     | 33     | 33    |
| R1E (Hex) | 33     | 33       | 33    | 33    | 33     | 33     | 33    |
| R1F (Hex) | 33     | 33       | 33    | 33    | 33     | 33     | 33    |
| R2E (Hex) | 82     | 82       | 84    | 82    | 84     | 82     | 84    |
| R30 (Hex) | 22     | 22       | 2A    | 22    | 2A     | 22     | 2A    |
| R31 (Hex) | 61     | 61       | C1    | 61    | C1     | 61     | C1    |
| R69 (Hex) | 48     | 48       | 48    | 48    | 48     | 48     | 48    |
| R6A (Hex) | 50     | 50       | 50    | 50    | 50     | 50     | 50    |
| R82 (Hex) | 42     | 42       | 52    | 42    | 42     | 42     | 42    |
| R83 (Hex) | 6F     | 6F       | 6F    | 6F    | 6F     | 6F     | EF    |
| RB1 (Hex) | 90     | 90       | 90    | 90    | 90     | 90     | 90    |
| RB7 (Hex) | 00     | 00       | 00    | 00    | 00     | 00     | 00    |
| RBA (Hex) | 18     | 18       | 18    | 18    | 18     | 18     | 18    |
| RBB (Hex) | 35     | 35       | 35    | 35    | 35     | 35     | 35    |

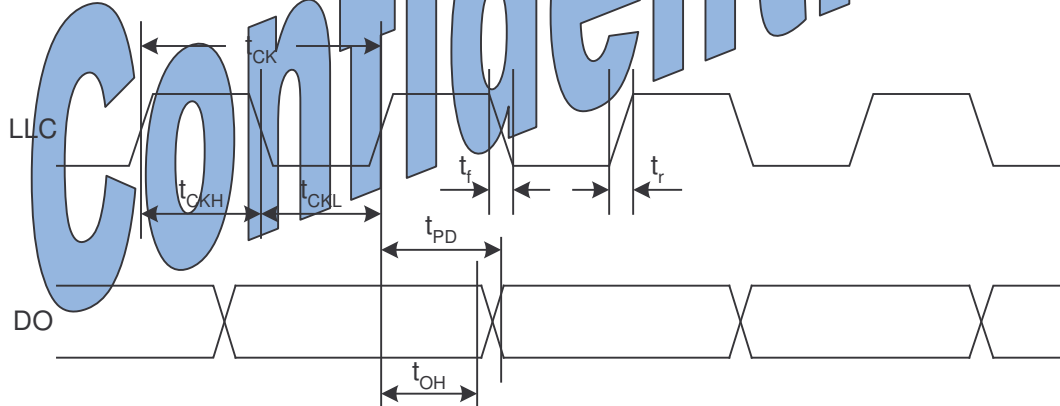
|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| RBC (Hex) | 2B | 2B | 2B | 2B | 2B | 2B | 2B |
| RBF (Hex) | 03 | 03 | 03 | 03 | 03 | 03 | 03 |
| RD4 (Hex) | 3C | 3C | 3C | 3C | 3C | 3C | 3C |
| RD5 (Hex) | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| R3F (Hex) | 00 | 00 | 00 | 00 | 00 | 00 | 00 |

## 10 Output Timing

### 10.1 Timing Diagram



**Figure 7: ITU-R.BT656 8-bit Output Timing**



**Figure 8: Data Output Timing**

## 11 Electrical Characteristics

### 11.1 Absolute Maximum Ratings Under Free-Air Temperature

(Excessive ratings are harmful to the lifetime. Only for user guidelines, not tested.)

| Parameter        |                                                | 1.8V/3.3V Rating               | Unit |
|------------------|------------------------------------------------|--------------------------------|------|
| AVDD33           | Analog front end supply voltage (AVDD to AGND) | -0.3 ~ +4.5                    | V    |
| DVDD33           | I/O supply voltage (DVDD to DGND)              | -0.3 ~ +4.5                    | V    |
| AVDD18           | Analog logic supply voltage (AVDD to AGND)     | -0.3 ~ +2.3                    | V    |
| DVDD18           | Digital core supply voltage (DVDD to DGND)     | -0.3 ~ +2.3                    | V    |
| V <sub>P</sub>   | Input pin voltage (V <sub>P</sub> to DGND)     | -0.3 ~ +(V <sub>DD</sub> +0.3) | V    |
| I <sub>O</sub>   | Output current                                 | -20 ~ +20                      | mA   |
| T <sub>AMB</sub> | Ambient operating temperature                  | 0 ~ +70                        | °C   |
| T <sub>stg</sub> | Storage temperature                            | -40 ~ +125                     | °C   |

### 11.2 Recommended Operating Conditions

| Parameter       |                                 | 1.8V/3.3V Rating    |         |                     | Unit |
|-----------------|---------------------------------|---------------------|---------|---------------------|------|
|                 |                                 | Min.                | Typical | Max.                |      |
| AVDD33          | Analog front end supply voltage | +3.0                | +3.3    | +3.6                | V    |
| DVDD33          | I/O supply voltage              | +3.0                | +3.3    | +3.6                | V    |
| AVDD18          | Analog logic supply voltage     | +1.65               | +1.8    | +2.0                | V    |
| DVDD18          | Digital core supply voltage     | +1.65               | +1.8    | +2.0                | V    |
| V <sub>IH</sub> | High level input voltage        | 0.7 V <sub>DD</sub> |         | V <sub>DD</sub>     | V    |
| V <sub>IL</sub> | Low level input voltage         | 0                   |         | 0.3 V <sub>DD</sub> | V    |
| T <sub>A</sub>  | Operating free-air temperature  | 0                   |         | +70                 | °C   |

### 11.3 Crystal Specifications

| Parameter | Rating  | Unit |
|-----------|---------|------|
| Frequency | 20.0000 | MHz  |

|                     |          |     |
|---------------------|----------|-----|
| Frequency Tolerance | $\pm 50$ | Ppm |
|---------------------|----------|-----|

#### 11.4 Analog Front End Processing and A/D Converters

| Parameter  |                               | 1.8V/3.3V Rating |         |      | Unit    |
|------------|-------------------------------|------------------|---------|------|---------|
|            |                               | Min.             | Typical | Max. |         |
| $V_i$ (pp) | Input range                   | 0.375            |         | 3    | Vpp     |
| $F_B$      | Band width                    |                  | 6       |      | MHz     |
| $F_S$      | ADC sample rate               |                  |         | 27   | MHz     |
| DNL        | DC differential non-linearity |                  | 0.5     |      | LSB     |
| INL        | DC integral non-linearity     |                  | 1       |      | LSB     |
| SNR        | Signal-to-noise ratio         | 50               |         |      | dB      |
| CS         | Channel separation            | 66               |         |      | dB      |
| DG         | Differential gain             |                  |         | 1    | %       |
| DP         | Differential Phase            |                  |         | 1    | Degrees |

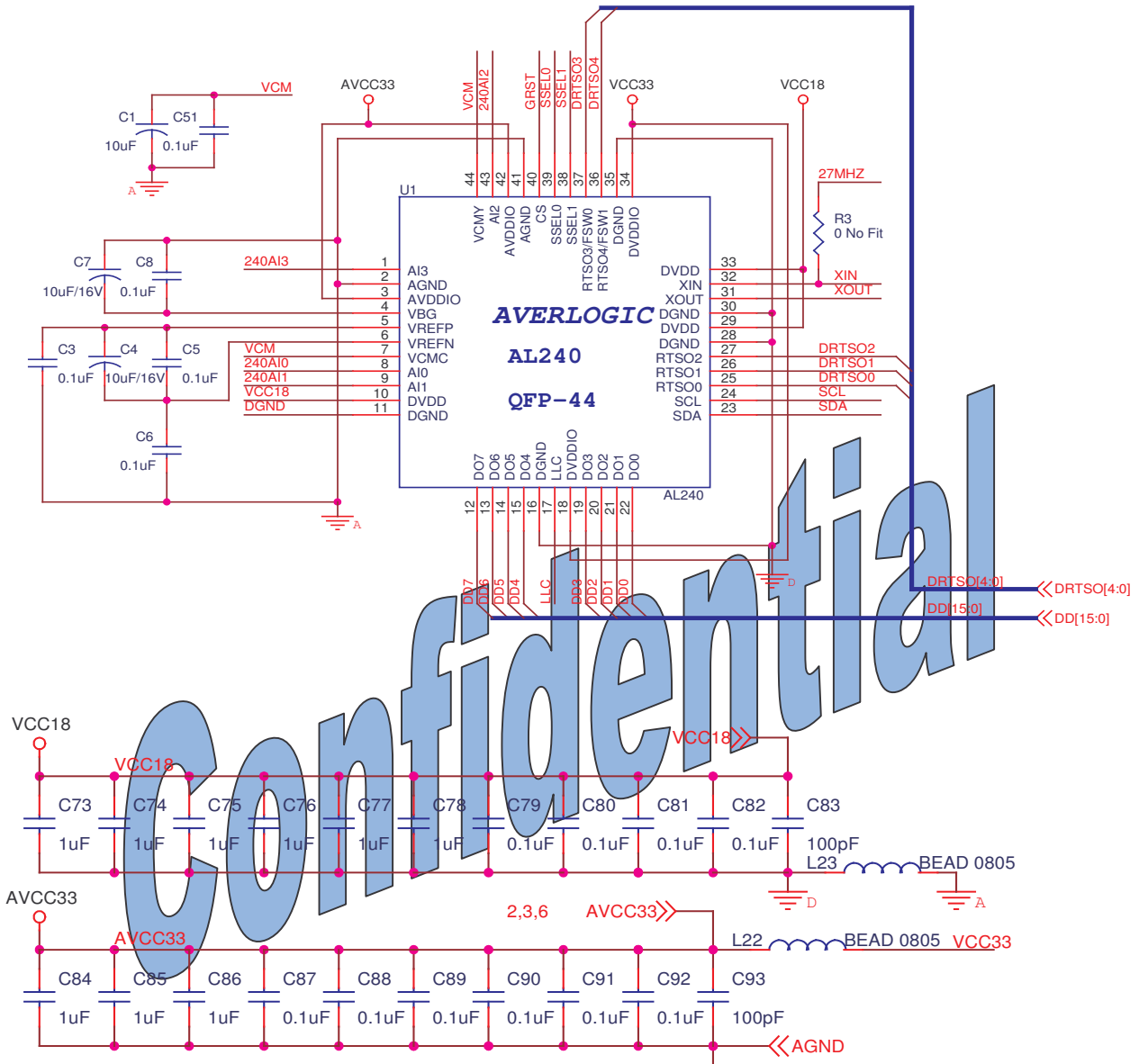
#### 11.5 AC Characteristics

( $V_{DD} = 1.8V/3.3V$ ,  $V_{SS} = 0V$ ,  $T_{AMB} = 0$  to  $70^\circ C$ ; Some parameters are guaranteed by design only, not production tested)

| Parameter               |                                               | 1.8V/3.3V Rating |         |      | Unit |
|-------------------------|-----------------------------------------------|------------------|---------|------|------|
|                         |                                               | Min.             | Typical | Max. |      |
| Power Supply Current    |                                               |                  |         |      |      |
| I <sub>DD</sub>         | Operating Current @27MHz                      |                  | TBD     |      | mA   |
| I <sub>DDS</sub>        | Standby Current                               |                  | TBD     |      | mA   |
| P                       | Power Consumption                             |                  | TBD     |      | mW   |
| Output interface timing |                                               |                  |         |      |      |
| t <sub>CK</sub>         | cycle time for data output (LLC)              |                  | 18      |      | ns   |
| t <sub>r</sub>          | Rising time for LLC                           |                  |         | 1.5  | ns   |
| t <sub>f</sub>          | Falling time for LLC                          |                  |         | 1.5  | ns   |
| t <sub>PD</sub>         | Propagation delay for DO in 8-bit output mode | 3                |         |      | ns   |
| t <sub>OH</sub>         | Hold time for DO in 8-bit output mode         | 2                |         |      | ns   |

## 12 Application Information:

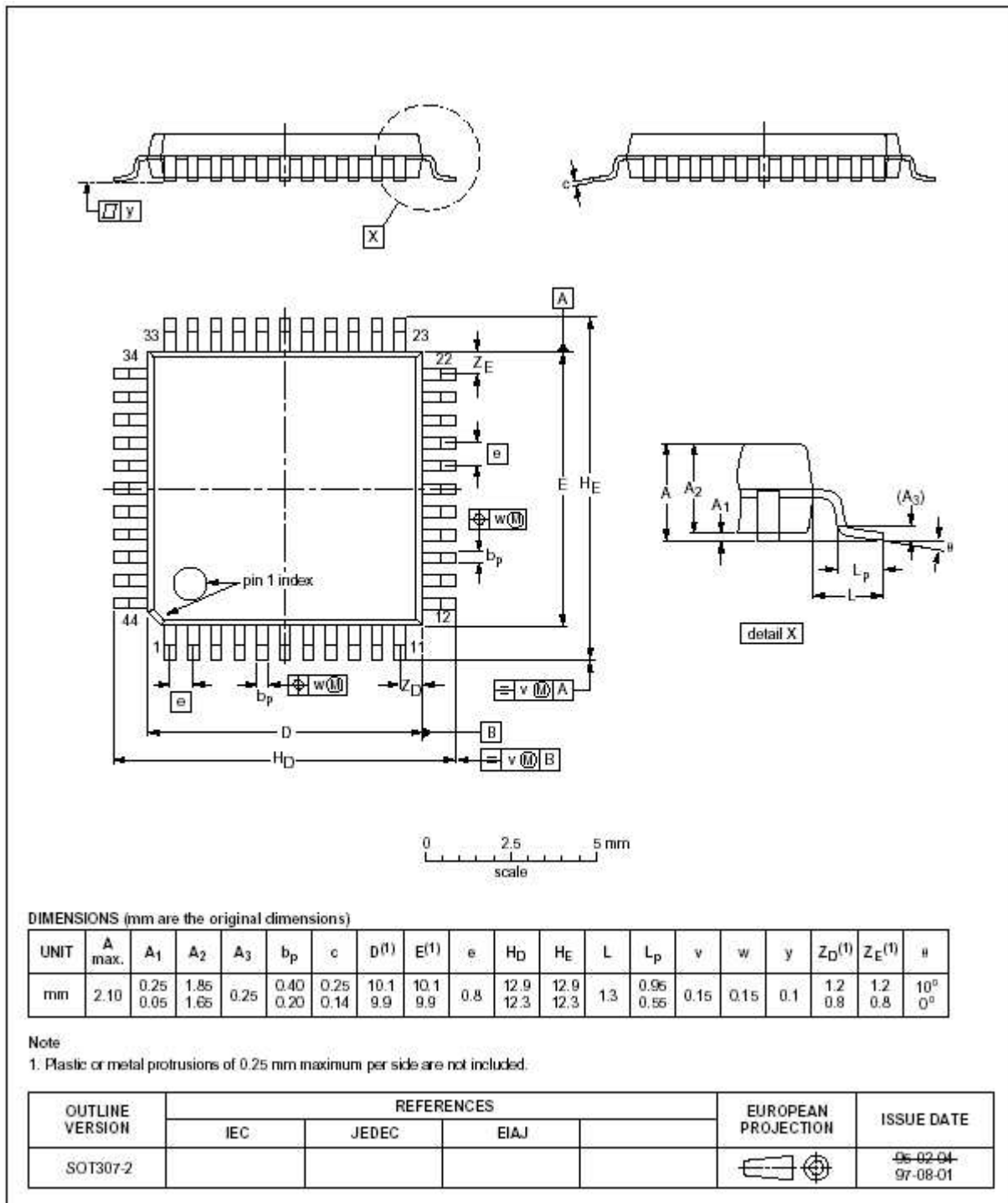
### 12.1 Analog Front End connection



**Figure 9: Analog Front End**

## 13 Mechanical Drawing 44-PIN QFP

### 13.1 10x10 mm 44-PIN QFP package



## CONTACT INFORMATION

Averlogic Technologies Corp. Taiwan

Email: [sales@averlogic.com.tw](mailto:sales@averlogic.com.tw)

URL: <http://www.averlogic.com.tw>

Averlogic Technologies, Inc. USA

Email: [sales\\_usa@averlogic.com.tw](mailto:sales_usa@averlogic.com.tw)

URL: <http://www.averlogic.com>

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