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OptoRec AL1402 Converter

General Description

The AL1402 OptoRec interface is designed to decode the ADAT® optical data stream and produce four stereo pairs of audio data. Alesis ADAT® U.S. patent number 5,297,181.

Use of this product requires a license agreement between manufacturer and Alesis Studio Electronics. Details and agreement information are available upon request from Alesis Semiconductor or Alesis Studio Electronics.

Features

- Compatible with ADAT® Type I and II formats
- 4 stereo pairs as outputs using standard ADC formats
- 4 user bit outputs to receive time-code, MIDI data, etc.
- Internal PLL generates required clocks from optical data.
- Word Clock input to synchronize outputs to user's system.

Applications

- Receive information from ADAT® compatible devices.

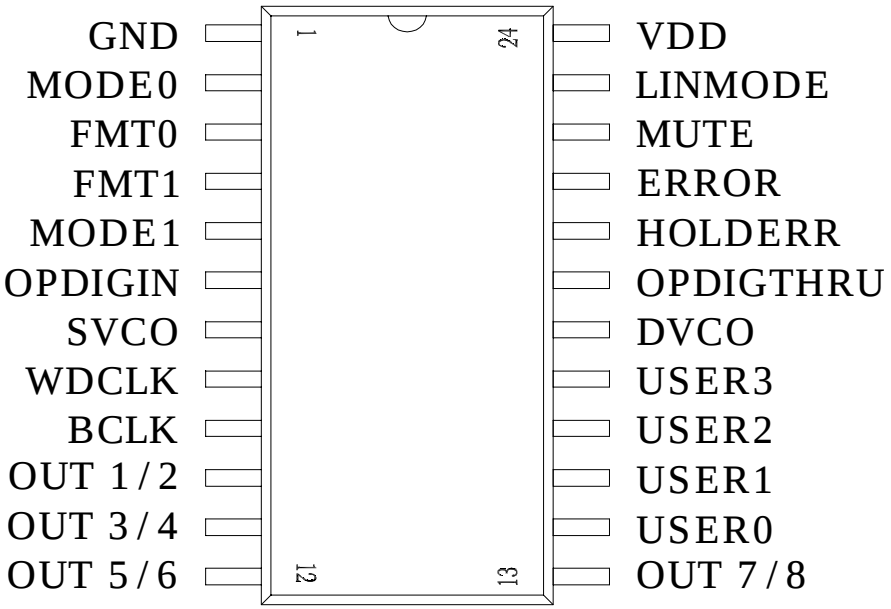

Figure A. 24 pin SOIC

DS1402-0702

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Table 1 Electrical Characteristics and Operating Conditions

Symbol	Description	Min	Typ	Max	Units
Recommended Operating Conditions					
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
I_{DD} Master	Supply Current, Master	-	7.7	-	mA
I_{DD} Slave	Supply Current, Slave	-	5.4	-	mA
GND	Ground	-	0.0	-	V
Fs	Sample rate	30	48	55	kHz
Temp	Temperature	0	25	70	°C
Inputs (WDCLK, FMT, OPDIGIN, MODE, LINMODE, MUTE, HOLDERR)					
V_{IH}	Logical "1" input voltage	0.75 V_{DD}	-	-	V_{DD}
V_{IL}	Logical "0" input voltage	-	-	0.25 V_{DD}	V_{DD}
I_{IH}	Logical "1" input current	-	-	1	uA
I_{IL}	Logical "0" input current	-	-	1	uA
C_{IN}	Logic Input Capacitance	-	5	-	pF
Outputs (WDCLK, DVCO, OPDIGTHRU, SVCO, BCLK, ERROR)					
V_{OH}	Logical "1" output voltage	0.9 V_{DD}	-	-	V_{DD}
V_{OL}	Logical "0" output voltage	-	-	0.1 V_{DD}	V_{DD}
I_{OH}	Logical "1" output current	-	-	-8	mA
I_{OL}	Logical "0" output current	-	-	8	mA
Outputs (OUT, USER)					
V_{OH}	Logical "1" output voltage	0.9 V_{DD}	-	-	V_{DD}
V_{OL}	Logical "0" output voltage	-	-	0.1 V_{DD}	V_{DD}
I_{OH}	Logical "1" output current	-	-	-2	mA
I_{OL}	Logical "0" output current	-	-	2	mA

Table 2 Pin Descriptions

Pin #	Name	Pin Type	Description
1	GND	Power	Ground pin
2	MODE0	Input	Mode select
3	FMT0	Input	Format select
4	FMT1	Input	Format select
5	MODE1	Input	Mode select
6	OPDIGIN	Input	Input from optical receiver
7	SVCO	Output	Derived clock from WDCLK in slave mode; derived from DVCO in Master mode (nominal 12.288MHz, 256x Fs)
8	WDCLK	I/O	Input or output word clock, see Table 4, Modes (nominal 48KHz, Fs)
9	BCLK	Output	Bit clock (nominal 3.072MHz, 64 x Fs)
10	OUT 1/2	Output	Channels 1 and 2 data output
11	OUT 3/4	Output	Channels 3 and 4 data output
12	OUT 5/6	Output	Channels 5 and 6 data output
13	OUT 7/8	Output	Channels 7 and 8 data output
14	USER0	Output	USER0 data bit output. Used to receive timecode
15	USER1	Output	USER1 data bit output. Used to receive MIDI data.
16	USER2	Output	USER2 data bit output. Reserved.
17	USER3	Output	USER3 data bit output. Reserved.
18	DVCO	Output	Recovered clock from data stream(nominal 12.288MHz, 256 x Fs)
19	OPDIGTHRU	Output	OPDIGIN is regenerated and clocked out on this pin to allow daisy-chaining
20	HOLDERR	Input	If high, the ERROR pin stays high until the cause of the error is removed AND the HOLDERR pin goes low.
21	ERROR	Output	Indicates lack of input or failure to synchronize to data stream, mutes data outputs but not clock outputs
22	MUTE	Input	If high, mutes outputs
23	LINMODE	Input	Tie high
24	V_{DD}	Power	+5V power pin

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Master and Slave Modes

Master Mode:
All outputs are derived from the input optical format data stream on the OPDIGIN (pin 6). WDCLK is an output.

Slave Mode:
DAC outputs, USER outputs, BCLK and SVCO outputs are synchronized to WDCLK, which is an input.

In Slave mode, WDCLK may be at an arbitrary phase with respect to the incoming samples of OPDIGIN, but if the frequencies aren't identical samples will be dropped, repeated, or garbled. Generally, identical frequencies are achieved by either: using DVCO (pin 18) as the source from which WDCLK is generated, or creating OPDIGIN from a source synchronized to WDCLK.

Use

The AL1402 OptoRec interface has been designed for ease of use and flexibility in systems designed to interface to the ADAT® protocol. It supports both left and right justified data formats for ease of integration into existing devices as well as new devices. These formats allow it to operate in parallel with many standard ADC's.

The designer uses the FMT0, FMT1, MODE0 and MODE1 pins to select the desired format and mode.

The format pins are summarized in Table 3, Formats. The AL1402 provides support for both the ADAT® Type I format (16-bit) and the ADAT® Type II format (20-bit). Data output is 24 bit. Data input lengths up to 24 bits is supported.

USER0 is used to receive the ADAT® format 32-bit timcode; USER1 is used to receive MIDI data (if the source device supports these features). USER2 and USER3 are reserved and should not be used.

Table 3 Formats

FMT1	FMT0	Format
0	0	OUT data is right justified, BCLK falls on changing WDCLK
0	1	OUT data is left justified, BCLK rises on changing WDCLK
1	0	Chip Reset
1	1	Gated BLCK, BCLK rises on changing WDCLK

Table 4 Modes

MODE1	MODE0	Mode
0	0	Master mode, WDCLK is an output
0	1	Slave mode, WDCLK is an input. WDCLK MUST be derived from the same clock supplying the source
1	0	Reserved
1	1	Reserved

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TIMING

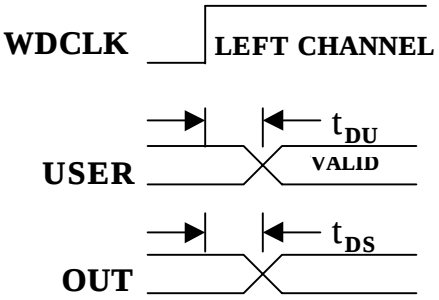

Figure B/Table 5 Output Delay

Symbol	Min	Typ	Max	Units
t_{DU}(Master)	-10	2	27	nsec
t_{DU}(Slave)	-7	5	30	nsec
t_{DS}(Master)	-10	0	25	nsec
t_{DS}(Slave)	-8	2	27	nsec

(Above specifications hold after 3900 WDCLK cycles of valid input at OPDIGIN)

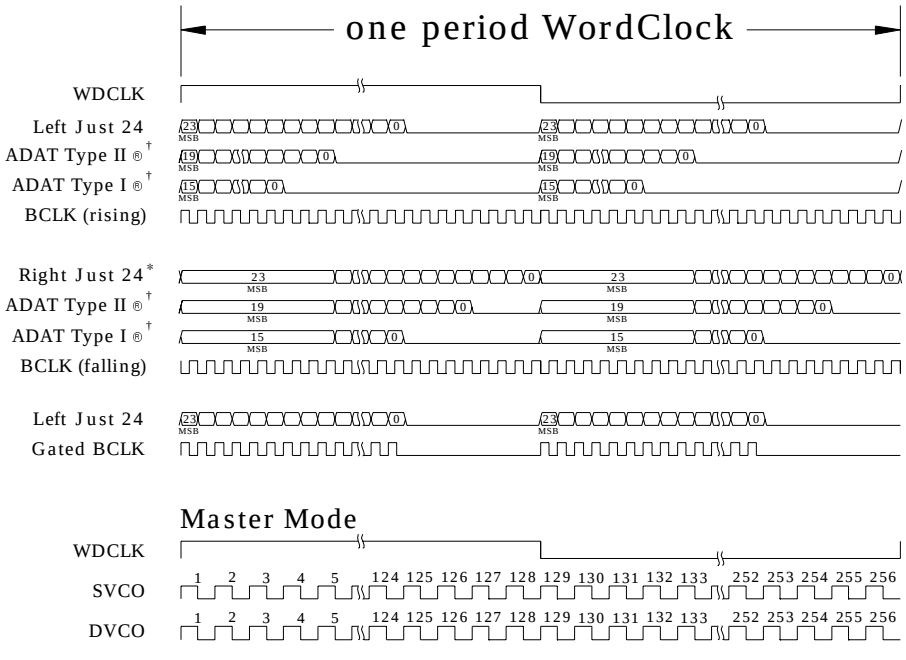

Figure C. Output Timing Diagram

In Slave mode DVCO is not phase aligned with WDCLK and SVCO.

* MSB bit is sign extended to left of frame.

† These diagrams represent how data would be framed from an ADAT type I or type II device. They are not actual modes of the AL1402. The Left Justified Mode is recommended for ADAT formats.

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Mechanical Specification

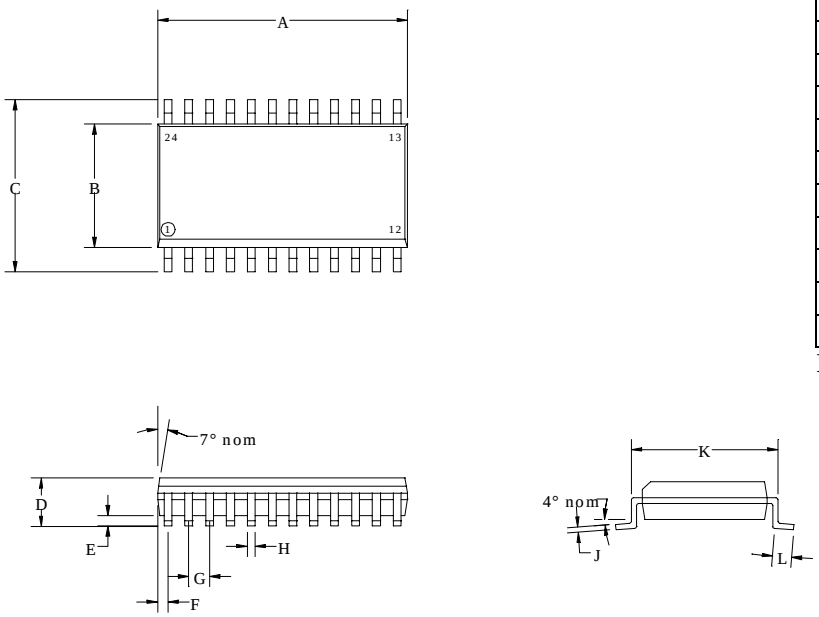

Figure D. Mechanical Drawing

Table 6 Package Dimensions

	Dimensions (Typical)	
	Inches	Millimeters
A	.606”	15.40
B	.295”	7.50
C	.406”	10.30
D	.100”	2.50
E	.008”	0.20
F	.025”	0.64
G	.050”	1.27
H	.017”	0.42
J	.011”	0.27
K	.352”	8.94
L	.033”	0.83

Notes:

1) Dimension “A” does not include mold flash, protrusions or gate burrs.

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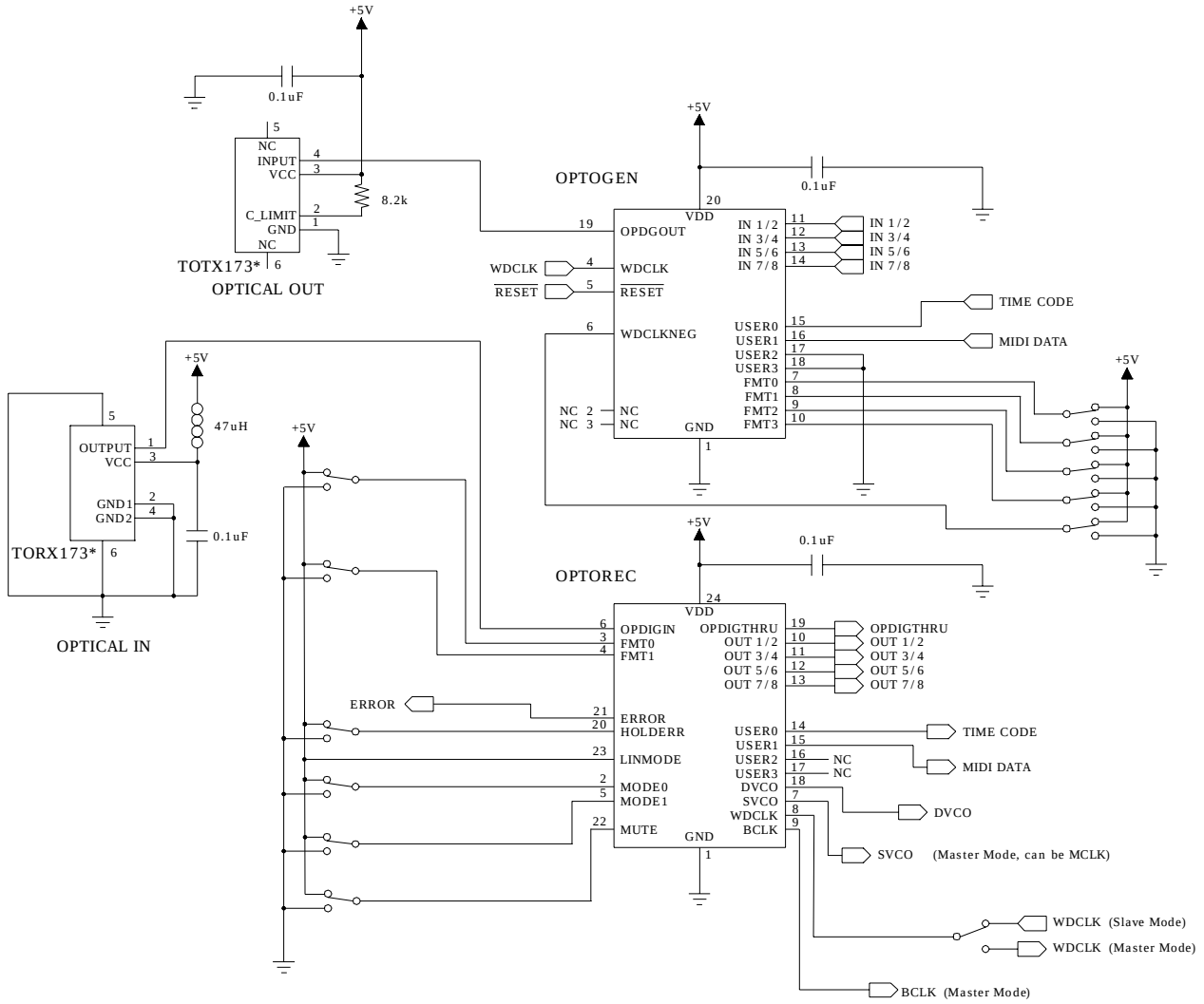
Sample Application Schematic



* Optical I/O parts shown are Toshiba parts. The Sharp GP1F33RT or equivalent is also compatible.

Figure E. OptoGen/OptoRec setup

The OptoGen accepts input from an ADC, then outputs the Alesis optical format. The OptoRec accepts input in Alesis optical format, then outputs to a DAC.

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The clock and data outputs of the AL1402 are undefined after power-up until a proper data stream is well established at OPDIGIN (pin 6). The clock outputs may be running at an uncontrolled frequency. In this case, the ERROR pin will be high, indicating that the outputs are invalid. This may be prevented by applying logic one to FORMAT1 (pin 4) and logic zero to FORMAT0 (pin 3) on power-up. This resets the AL1402, stopping the VCO clocks and muting the data output. The FORMAT pins may then be set to the value required in your system. Nevertheless the AL1402 will synchronize and produce proper outputs when proper and valid inputs are provided, whether this reset procedure is used or not.

The AL1402 in Master Mode can also produce clock outputs running at uncontrolled frequencies if the digital input becomes unstable after stable use, due mostly to poor connection of the optical cable to the optical connector. If this is unwanted in the system an external AND implementation can be used to correct this. The inverted error pin and the desired AL1402 output clock are inputs to the AND and the desired mutable clock is output. This AND function will mute the selected AL1402 clock when the error pin is high (i.e. when unstable input is present at OpDigIn). Care should be taken when running the AL1402 with the AL1201 DAC as the AL1201 DAC will output noise if the AL1402 WDCLK is at an uncontrolled VCO frequency that is beyond the AL1201 maximum frequency. The aforementioned AND function can be used to select the AL1402 WDCLK to be muted when invalid OpDigInput is present before proceeding as the AL1201 WDCLK. See Figure F. with the AND function implemented with NAND gates. In place of this circuit the ERROR pin can be used as a mute select for any audio output stage muting circuitry that may be present in the system.

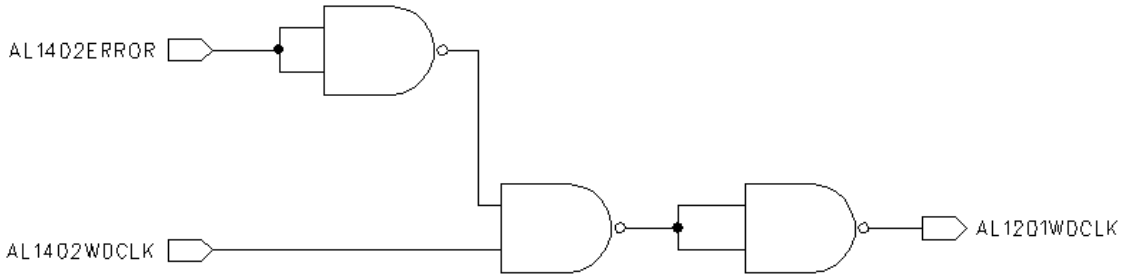

Figure F. AL1402 –AL1201 CLK MUTE CIRCUIT.

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