

Low Spurious Multiclock Generator with XO AK8138MV

Features

- 27MHz Crystal Input or External Input
- Four Frequency-Selectable Clock Outputs
- One 27MHz-Reference Output
- Selectable Clock out Frequencies:
 - CLK1: 24.576MHz
 - CLK2: 2.048,4.096,8.192,11.2896,12.288,
 - 22.5792MHz
 - CLK3: 6.144,8.192,11.2896,12.288, 16.9344,22.5792MHz
 - CLK4: 8.4672,11.2896,13.824, 16.9344MHz
- Built-in XO
- Low Jitter Performance
 - Period Jitter:
 - 30 psec (Typ.) at CLK1-4
 - Long Term Jitter:
 - 60 psec (Typ.) at CLK1-4
- Low Current Consumption:
 - 18.0mA (Typ.) at 3.3V, S[3:0]='HHHH'
- Supply Voltage:
 - 2.85V to 3.6V
- Operating Temperature Range:
 - -40°C to +85°C
- Package:
 - 16-pin SSOP (Lead free, Halogen free)

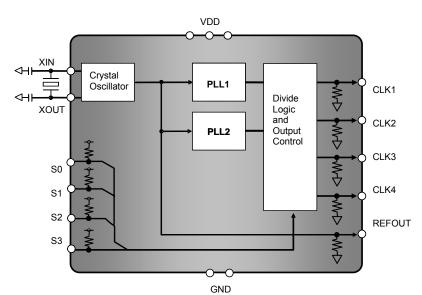
Description

The AK8138MV is a member of AKM's low power multi clock generator family designed for a high quality audio cock with high performance C/N. The AK8138MV generates different frequency clocks from a 27MHz crystal oscillator or external 27MHz clock input. It provides them to up to four outputs configured by pin-setting. Both circuitries of XO and PLL in AK8138MV are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption. The AK8138MV is available in a 16-pin SSOP package.

Applications

- Personal Video Recorders
- Set-Top-Boxes
- Multi Media Receivers

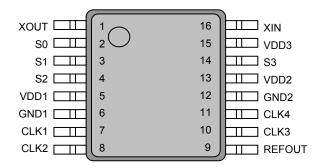
Block Diagram



AK8138MV Multi Clock Generator



Pin Descriptions



Package: 16-Pin SSOP(Top View)

Pin No.	Pin Name	Pin Type	Description	
1	XOUT	OUT	Crystal connection, Connect to 27.000MHz crystal	
'	XOUT	001	Please open when an external clock input is used	
2	S0	IN	Clock Out Frequency select 0, See Table 2 for the selection	(1)
3	S1	IN	Clock Out Frequency select 1, See Table 2 for the selection	(1)
4	S2	IN	Clock Out Frequency select 2, See Table 2 for the selection	(1)
5	VDD1	ŀ	Power Supply 1	
6	GND1		Ground 1	
7	CLK1	OUT	Clock output 1, See Table 1 for its selectable frequency	(2)
8	CLK2	OUT	Clock output 2, See Table 2 for its selectable frequency	(2)
9	REFOUT	OUT	Reference Clock Output of 27.000MHz Crystal or external clock	(2)
10	CLK3	OUT	Clock output 3, See Table 2 for its selectable frequency	(2)
11	CLK4	OUT	Clock output 4, See Table 2 for its selectable frequency	(2)
12	GND2		Ground 2	
13	VDD2		Power Supply 2	
14	S3	IN	Clock Out Frequency select 3, See Table 1 for the selection	(1)
15	VDD3		Power Supply 3	
			Crystal connection, Connect to 27.000MHz crystal	
16	XIN	IN	Or external clock input (minimum 1Vpp input).	
10	AIIN	IIN	Input becomes binary after passing an internal HPF.	
			Input Resistance is 37.5k-ohm.	

- (1) Internal pull up $360 k\Omega$
- (2) Internal pull down $510k\Omega$

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range	
AK8138MV	8138MV	Tape and Reel	16-pin SSOP	-40 to 85 °C	



Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I _{IN}	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Operating temperature	Та	AK8138MV	-40		85	°C
Supply voltage (1)	VDD		2.85	3.3	3.6	٧
Output Load Canacitance	Cp1	Pin: CLK1-4			15	pF
Output Load Capacitance	Cp2	Pin: REFOUT			25	pF

Note:

(1) Power to VDD1, VDD2 and VDD3 requires to be supplied from a single source. A decoupling capacitor of $0.1\mu F$ for power supply line should be installed close to each VDD pin.



DC Characteristics

All specifications at VDD: over 2.85 to 3.6V, Ta = -40 to 85 °C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High level input voltage	V _{IH}	Pin: S0,S1,S2,S3	0.7VDD			V
Low level input voltage	V _{IL}	Pin: S0,S1,S2,S3			0.3VDD	V
Input leak current	IL	Pin: S0,S1,S2,S3	-20		+10	μA
High Level output voltage	V _{OH}	Pin: CLK1-4, REFOUT I _{OH} =-4mA	0.8VDD			٧
Low level output Voltage	V _{OL}	Pin: CLK1-4, REFOUT I _{OL} =+4mA			0.2VDD	٧
Current consumption	I _{DD}	Ta=25°C, No load S[3:0] = 'HHHH'		18.0		mA

AC Characteristics

All specifications at VDD: over 2.85 to 3.6V, Ta = -40 to 85 °C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Crystal clock frequency		Pin: XIN, XOUT	26.9	27.0000	27.1	MHz
External clock frequency		Pin: XIN ⁽¹⁾	26.9	27.0000	27.1	MHz
Period jitter (4)		Pin: CLK1-4 ⁽²⁾ , REFOUT ⁽³⁾		30		ps
Long Term jitter (4)		Pin: CLK1-4 ⁽²⁾ , REFOUT ⁽³⁾ 1000cycles		60		ps
Output Clock duty		Pin: CLK1-4 (2)	45	50	55	%
Cycle		Pin: REFOUT (3)	40	50	60	%
Output clock rise time	t _{rise}	Pin: CLK1-4 (2), REFOUT (3)		2.5		ns
Output clock fall time	t _{fall}	Pin: CLK1-4 (2), REFOUT (3)		2.5		ns
Output Lock Time (4)		Pin: CLK1-4 (2)		5		ms

- (1) Amplitude is 1Vpp or more.
- (2) Measured with load capacitance of 15pF
- (3) Measured with load capacitance of 25pF
- (4) 1σ in 10000 sampling or more
- (5) The time that output reaches the target frequency within accuracy of $\pm 0.1\%$ from the point that the power supply reaches VDD.



Output clock frequency selection

The AK8138MV generates a range of low-jitter and high-accuracy clock frequencies with two built-in PLLs and provides to up to four assigned outputs. A frequency selection at assigned output pin is configured by pin-setting of S0 (Pin2), S1 (Pin3), S2(Pin4) and S3 (Pin14).

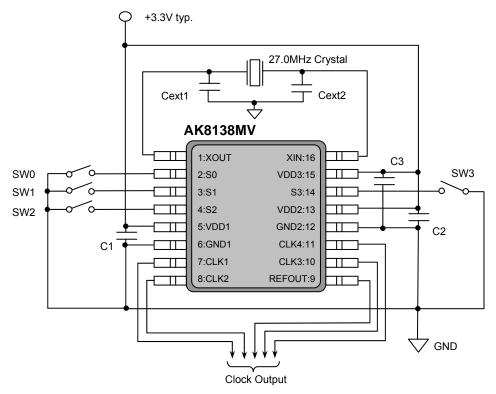
The selectable frequency is shown in Table1.

Committee	Selection Pin				Clock Output Frequency (MHz)			
Sampling Frequency (kHz)	S3 (Pin 14)	S2 (Pin 4)	S1 (Pin 3)	S0 (Pin 2)	CLK1 (Pin 7)	CLK2 256fs (Pin 8)	CLK3 384fs (Pin 10)	CLK4 (Pin 11)
48.0	L	L	L	L	24.576	12.288	OFF	OFF
44.1	L	L	L	Н	24.576	11.2896	16.9344	OFF
32.0	L	L	Н	L	24.576	8.192	12.288	OFF
88.2	L	L	Н	Н	24.576	22.5792	OFF	OFF
16/22.05	Н	Н	L	L	24.576	4.096	11.2896	8.4672
16/44.1	Н	Н	L	Н	24.576	4.096	22.5792	8.4672
8/16	Н	Н	Н	L	24.576	2.048	6.144	16.9344
8/16	Н	Н	Н	Н	24.576	4.096	11.2896	11.2896
EXT1	L	L	L	L	24.576	2.048	8.192	13.824
EXT2	L	L	L	Н	24.576	OFF	OFF	13.824
Reserved	L	L	Н	L	OFF	OFF	OFF	OFF
Reserved	L	L	Н	Н	OFF	OFF	OFF	OFF
Reserved	L	Н	L	L	OFF	OFF	OFF	OFF
Reserved	L	Н	L	Н	OFF	OFF	OFF	OFF
Reserved	L	Н	Н	L	OFF	OFF	OFF	OFF
Reserved	L	Н	Н	Н	OFF	OFF	OFF	OFF

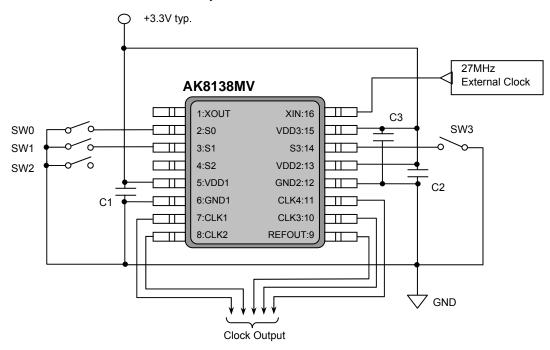
Table 1: CLK1-4 Clock output Frequency



Typical Connection Diagram



A: Crystal connection



B: External clock input

Figure 1: Typical Connection Diagram

C1-3 : 0.1µF

Cext1-2 : Depends on crystal characteristics. Refer the specification of the crystal.

SW0-3: Open is "H" and tied to GND is "L" for S0, S1, S2 and S3, because these pins

have internal pull up resister.



PCB Layout Consideration

The AK8138MV is a high-accuracy and low-jitter multi clock generator. For proper performances specified in this datasheet, careful PCB layout should be taken. The followings are layout guidelines based on the typical connection diagram shown in Figure 1

Power supply line – AK8138MV has three power supply pins (VDD1-3) which deliver power to internal circuitry segments. A 0.1μF decoupling capacitor should be placed as close to each VDD pin as possible.

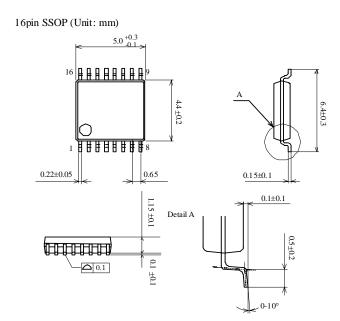
Ground pin connection – AK8138MV has two ground pins (GND1-2). These pin require connecting to plane ground which will eliminate any common impedance with other critical switching signal return. $0.1\mu F$ decoupling capacitors placed at VDD1, VDD2, and VDD3 should be grounded at close to the GND1pin, the GND2 pin, and the GND2, respectively.

Crystal connection – Proper oscillation performance are susceptible to stray or parasitic capacitors around crystal. The wiring traces to a crystal form XIN (Pin 16) and XOUT (Pin 1) have equal lengths with no via and as short in length as possible. These traces should be also located away from any traces with switching signal.

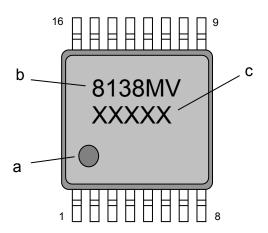


Package Information

• Mechanical data



Marking



- a: #1 Pin Index
- b: Part number
- c: Date code (5 digits)

• RoHS Compliance



All integrated circuits form Asahi Kasei Microdevices Corporation (AKM) assembled in "lead-free" packages* are fully compliant with RoHS.

 $(\mbox{\sc *})$ RoHS compliant products from AKM are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.



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