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AK7841

Monaural Audio Class-D Amp with Power Booster for PiezoSpeaker

GENERAL DESCRIPTION

The AK7841 is a Monaural Class-D amplifier for driving Piezo-Electric Speakers. Its built-in power boost DCDC converter generates adequate high voltage for driving Piezo Speaker from a Li-Ion battery. Output filter-less solution eliminates post LC-filters, which are normally required at Class-D outputs, and contributes to total space savings. Class-D operation ensures higher power efficiency. The AK7841 is the most appropriate for Cellular Phones with a piezo speaker.

FEATURES

☐ **Class-D Amplifier :**
- Piezo-Electric Speaker Driver
- Analog Monaural signal input for both single and Differential-ended
- Monaural BTL output
- Output voltage = 12Vpp @VDD1=8.75V
- Filter-less solution
- Pop noise free architecture during power up or down.
- Output short protection

☐ **Boost DCDC Converter :**
- Input voltage = 2.7V ~ 4.5V → Output voltage = 8.75V
- Over-current protection
- Over-voltage protection

☐**Control function :**
- Pre-gain amplifier −3dB ~ +18dB, 3dB step. Controlled by pin setting.
- Power-own control
- Over-temperature protection

☐**Operational voltage :** VBAT=2.7V ~ 4.5V、DVDDI=1.65V ~ 4.5V

☐**Operational temperature :** −30°C ~ 85°C

☐**Package :** 24pin WL-CSP (2.5mm × 2.5mm, 0.5mm pitch)

BLOCK DIAGRAM

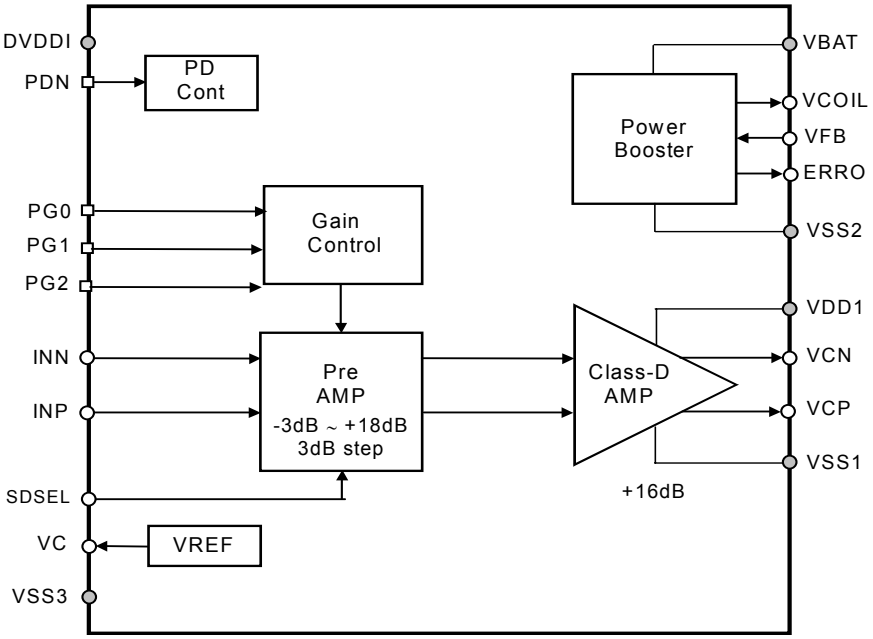
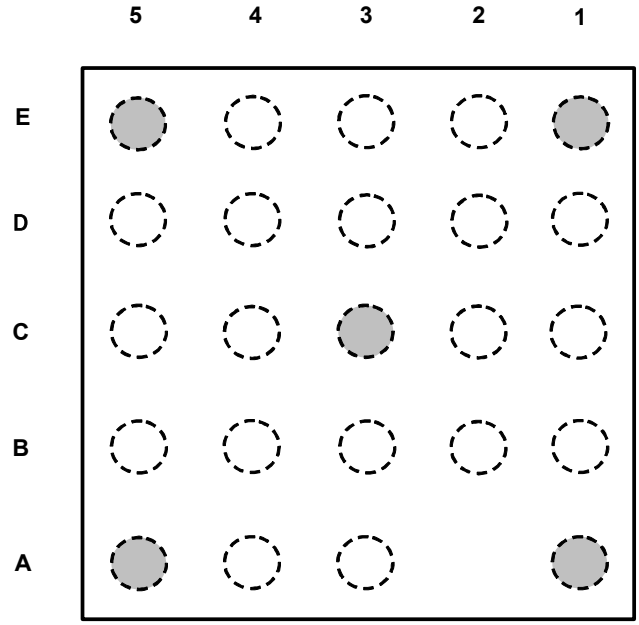


Figure. 1 Block Diagram

PIN ASSIGNMENT



< Top View >

	5	4	3	2	1
E	NC	VFB	VDD1	VCP	NC
D	VCOIL	VSS2	SDSEL	VCN	VSS1
C	ERRO	VBAT	NC	VSS3	VC
B	PG2	PG0	PDN	INN	INP
A	NC	PG1	DVDDI	<Index>	NC

Figure.2 Pin assignment

Pin / FUNCTION

No.	Pin Name	I/O	Function
A1	NC	-	No Connection pin. * Must be connected to VSS level.
A2	-		<Index>
A3	DVDDI	-	Digital interface power：DVDDI=1.65V ~ 4.5V
A4	PG1	I	Pre Gain setting pin1
A5	NC	-	No Connection pin. * Must be tied to VSS level during normal usage.
B1	INP	I	Positive analog input while differential-ended. OPEN while single-ended input.
B2	INN	I	Negative analog input while differential-ended. Analog input while single-ended.
B3	PDN	I	Power down contorol：schmitt trigger input “High”：poewer up、”Low”：power down
B4	PG0	I	Pre Gain setting pin0
B5	PG2	I	Pre Gain setting pin2
C1	VC	O	Voltage reference output * Connect 0.01μF capacitor in between VC and ground.
C2	VSS3	-	Internal analog circuit ground pin：VSS3=0V
C3	NC	-	No Connection pin. * Must be connected to VSS level.
C4	VBAT	-	Battery voltage input：VBAT=2.7V ~ 4.5V
C5	ERRO	O	Phase compensation for Boost DCDC. * Connect 0.1μF capacitor in between ERRO and ground.
D1	VSS1	-	Class D amp ground pin ：VSS1=0V
D2	VCN	O	Class D amp negative output (-)
D3	SDSEL	I	single-end／differential input setting pin “High” : single-end “Low”: differential input
D4	VSS2	-	Power Booster ground pin： VSS2=0V
D5	VCOIL	O	Inductor pin for Boost DCDC.
E1	NC	-	No Connection pin. * Must be connected to VSS level.
E2	VCP	O	Class D amp positive output (+)
E3	VDD1	-	Class D amp power supply ：VDD1=8.75V(typ.)
E4	VFB	I	Power Booster feedback
E5	NC	-	No Connection pin. * Must be connected to VSS level.

Note 1. Digital input pins (PDN, PG0, PG1, PG2, TEST1, TEST2) and NC pins must not be open.

■ Un-used Pins

Un-used pin must be configured as follows.

	Pin Name	Configuration
Analog	INP	OPEN

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=0V; Note 2)

Parameter		Symbol	Min.	Max.	Units
Power Supplies	Battery	VBAT	–0.3	6.5	V
	Class-D Amp	VDD1	–0.3	10	V
	Digital I/F	DVDDI	–0.3	6.5	V
	|VSS2-VSS1| (Note 3)	ΔGND1	-	0.3	V
	|VSS2-VSS3| (Note 3)	ΔGND2	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage(Note 4) (Note 6)		VINA	–0.3	VBAT+0.3	V
Digital Input Voltage (Note 5) (Note 6)		VIND	–0.3	DVDDI+0.3	V
Ambient Temperature		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 2. All voltages are with respect to ground.
Note 3. VSS1, VSS2, VSS3 pins must be connected to the same analog ground plane.
Note 4. IPN and INN pin.
Note 5. PDN, PG0, PG1, PG2, SDSEL pin.
Note 6. Maximum value must not exceed 6.5V even if VBAT or DVDDI are more than 6.2V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=0V;Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Battery (Note 7)	VBAT	2.7	3.6	4.5	V
	Class-D Amp (Note 8)	VDD1	-	8.75	-	V
	Digital I/F (Note 7)	DVDDI	1.65	2.8	4.5	V

Note 7. Have to be "VBAT≧ DVDDI"
Note 8. Supply with boosted voltage (typ. 8.75V) by the Power Booster.

* AKEMD assumes no responsibility for usage beyond the conditions in this datasheet.

DC CHARACTERISTICS

(Ta=25°C; VBAT=2.7V ~ 4.5V, DVDDI=1.65V ~ 4.5V, VSS1=VSS2=VSS3=0V)

Parameter		Symbol	Min.	Typ.	Max.	Units
High-Level Input Voltage 1 (Note 9)		VIH1	70%DVDDI	-	-	V
Low-Level Input Voltage 1 (Note 9)		VIL1	-	-	30%DVDDI	V
High-Level Input Voltage 2 (Note 10)		VIH2	80%DVDDI	-	-	V
Low-Level Input Voltage 2 (Note 10)		VIL2	-	-	20%DVDDI	V
Hysterisys Voltage (Note 10)	DVDDI=2.8V	VHS1	-	0.5	-	V
	DVDDI=1.65V	VHS2	-	0.3	-	V
Input Leakage Current		Iin	-	-	±10	μA

Note 9. Applied to PG0, PG1, PG2, and SDSEL pin.
Note 10. Applied to PDN pin (Summit trigger input. These specifications are guaranteed by design and characterization and are not tested in production.)

ANALOG CHARACTERISTICS

(Typ.) value is measured at Ta=25℃ and VBAT=3.6V,. The worst value was measured at the worst point between VBAT=2.7～4.5V and Ta=-30～+85℃, and written on (Min.) or (Max.) column.
Unless otherwise specified, Ta=25℃, VBAT=3.6V, DVDDI=2.8V, VSS1=VSS2=VSS3=0V;input signal frequency =1kHz; measurement band width=20Hz ~ 20kHz; pre gain=0dB; Class-D amp load capacitance is 1.0uF.

Parameter	Conditions	Min.	Typ.	Max.	Units
Idd	No input signal With output load.	-	17.3	26.0	mA
Shutdown Current	PDN pin = “Low”	-	1.0	10	μA
Input Impedance	INN pin	25	50	75	kΩ
	INP pin	25	50	75	kΩ
Pre Gain Control Range		-3.0		+18.0	dB
Pre Gain Step Size	PG2=”L”, PG1 = “L” , PG0 = “L”	-4.0	-3.0	-2.0	dB
	PG2=”L”, PG1 = “L” , PG0 = “H”	-1.0	0.0	+1.0	dB
	PG2=”L”, PG1 = “H” , PG0 = “L”	+2.0	+3.0	+4.0	dB
	PG2=”L”, PG1 = “H” , PG0 = “H”	+5.0	+6.0	+7.0	dB
	PG2=”H”, PG1 = “L” , PG0 = “L”	+8.0	+9.0	+10.0	dB
	PG2=”H”, PG1 = “L” , PG0 = “H”	+11.0	+12.0	+13.0	dB
	PG2=”H”, PG1 = “H” , PG0 = “L”	+14.0	+15.0	+16.0	dB
	PG2=”H”, PG1 = “H” , PG0 = “H”	+17.0	+18.0	+19.0	dB
Output Voltage	VCN/VCP pins Input signal level=0.70Vrms THD=10%	3.82.	4.24	4.66	Vrms
Output Offset Voltage	VCN/VCP pins No input signal	-	-	250	mV
THD+N	VCN/VCP pins Input signal level=0.50Vrms	-	-	–40	dB
SNR	VCN/VCP pins Input signal level=0.70Vrms, using A-weighting filter	70	80	-	dB
PSRR (Note 12)(Note 1Note 15)	VCN/VCP pins V_{ripple}=200mVpp @1kHz Sine-wave, VBAT=3.6V, all temperature	-	65	-	dB
CMRR (Note 12)(Note 1Note 15)	INP=1.2V±0.5V @Sine-wave, VBAT=3.6V, all temperature	-	65	-	dB
VREF Output Voltage (Note 12) (Note 13)	VC pin	-	2.4	-	V
Switching Frequency	Class-D Amp	225	250	275	kHz
	Power Booster	900	1000	1100	kHz
Start-up Time (Note 14)	VBAT=2.7V	-	28	31	ms

Note 11. Measure between VCN and VCP pin through Low-Pass-Filter (fc=20kHz).
Note 12. These specifications are guaranteed by design and characterization and are not tested in production.
Note 13. Analog ground in the AK7841 is 1.2V(typ.).
Note 14. Time period that is required to be stable output after PDN is “High”.
Note 15. These specifications are guaranteed by design and characterization and are not tested in production.

OPERATION OVERVIEW

■ Power Control

The AK7841 enters shutdown mode by setting "PDN" pin to Logic "Low" level.
And resumes normal operation mode (Stability Operation) by setting "PDN" pin to Logic "High" level.

Power-Up Control

VBAT and DVDDI must be turned on as (1) or (2) below.

(1) VBAT=DVDDI="ON" simultaneously.
(2) VBAT="ON" first, then DVDDI="ON".

Set PDN pin to "High" when driving AK7841. Then, 1μs wait after VBAT=DVDDI="High" is necessary before setting PDN="High". Do not do them simultaneously.

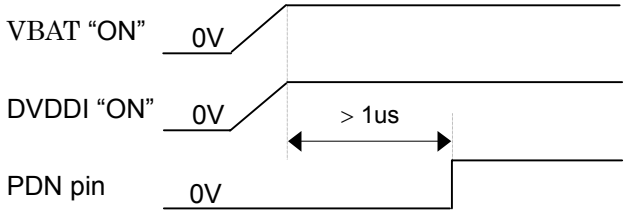


Figure. 3 Power-Up Sequence (1)

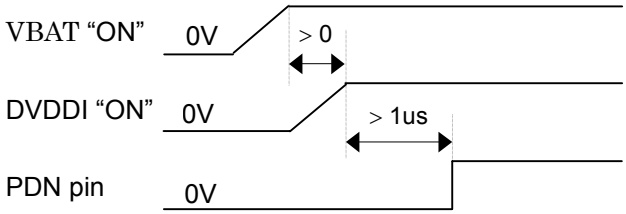


Figure. 4 Power –Up Sequence (2)

Attention: The performance of the device will not be guaranteed after the below sequence.

(3) DVDDI="ON" first, then VBAT="ON".

Power-Down Control

VBAT and DVDDI must be turned off as (4) or (5) below.
(4) VBAT=DVDDI="OFF" at the same time.
(5) DVDDI="OFF" first, then VBAT="OFF".
Set PDN pin to "Low" when shutting down. Then, 1µs wait is necessary before pulling down VBAT and DVDDI. Do not do them simultaneously.

※ When PDN pin is "High" and VBAT/DVDDI supply is suddenly cut off due to unexpected event, pop noise may be detected while sound signal is being output. Even under such cases LSI will not be harmed.

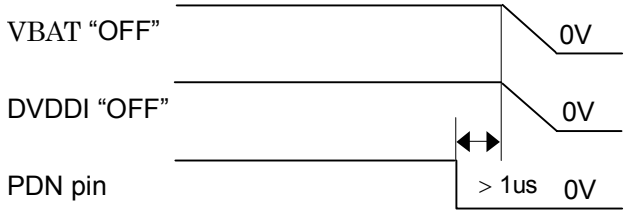


Figure. 5 Power-Down Sequence (4)

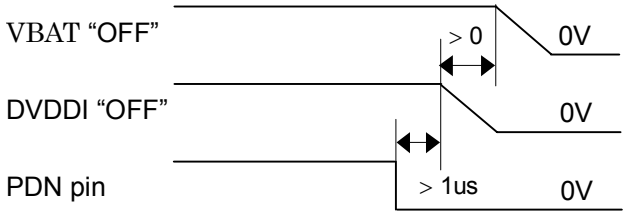


Figure. 6 Power –Down Sequence (5)

Attention: The performance of the device will not be guaranteed after the below sequence.
(6) VBAT="OFF" first, then DVDDI="OFF"

■ Analog inputs

The AK7841 correspond to both single and differential-ended input. Use ac coupling capacitors as described below. Avoid the change from 0.1uF of the recommended value as much as possible because these change of capacitance may influence not only HPF (High Pass Filter) at input but also the operation of the pop noise prevention circuit.

When single-ended input

Connect SDSEL pin to ground. Input t analog signal to INN pin through a 0.1uF capacitor. Then, INP pin should be open. (Figure. 16)

When differential-ended input

Connect SDSEL pin to DVDDI. Input t analog signal to between INN and INP pins through ac-coupling 0.1uF capacitors (Figure. 17). If two conditions are fulfilled as below, ac-coupling capacitors are not needed (Figure. 18).

1. **The voltage of INP and INN are VSS while shutting down.**
2. **The common level of INP and INN pin is between 0.8V and 1.6V, and input signals are within common level±0.5V for each pin (2Vpp).**

■ Pre AMP

Users can change Pre Gain value by setting PG0, PG1, PG2 pins as following Table.1.
For fixed gain application, these pins should be fixed to either VSS3 or DVDDI.

PG2	PG1	PG0	Pre Gain Setting Value
"Low"	"Low"	"Low"	-3.0 dB
"Low"	"Low"	"High"	0.0 dB
"Low"	"High"	"Low"	+3.0 dB
"Low"	"High"	"High"	+6.0 dB
"High"	"Low"	"Low"	+9.0 dB
"High"	"Low"	"High"	+12.0 dB
"High"	"High"	"Low"	+15.0 dB
"High"	"High"	"High"	+18.0 dB

Table.1 Pre Gain setting

■ Class-D amplifier.

The AK7841, a monaural Class-D audio amplifier, has higher efficiency compared to Class-AB amplifier. AK7841 would eliminate much external equipment especially output filter, which is normally equipped to cut high frequency spectrum in class-D output, by using a unique circuit composition.

■ Pop Noise Suppressor

The AK7841 features click-and-pop suppression circuit.

■ Power Booster

Built-in BOOST DCDC CONVERTER generates adequate high voltage for Piezo-Speaker (Typ.8.75V) from a Li-Ion battery voltage range (2.7～4.5V). Supply boosted voltage (VFB=8.75V) to VDD1 for class-D amp operation.

■ Protection

The AK7841 supports following protection circuits for protecting against any damages.

Output Short-Circuit Protection

In case detecting VCL(R)P and VCL(R)N short, the AK7841 clamps peak current of Class-D output circuit without shutting down the outputs.

Over-Temperature Protection

The AK7841 operation will stop at +150°C.
Note that the AK7841 DOES NOT support resume function from Over-Temperature Protection. Once it is activated, the AK7841 does not back in normal operation unless "PDN" is toggled ("L" → "H").

Over-Current Protection

Current-limiting protection clamps the output current without shutting down the outputs.

Over-Voltage Protection

AK7841 has a Voltage-limiting protection in DCDC converter to avoid destroying itself.

Performance characteristics

※ The following various characteristics are typical characteristic data in the typical condition. It is not the one necessarily to secure the characteristic of the description.

Sinwave Single - ended , Total Gain=15.6dB, Output Load Impedance Z_L=1uF,
Measurement Band Width =20～20kz, unless otherwise specified.

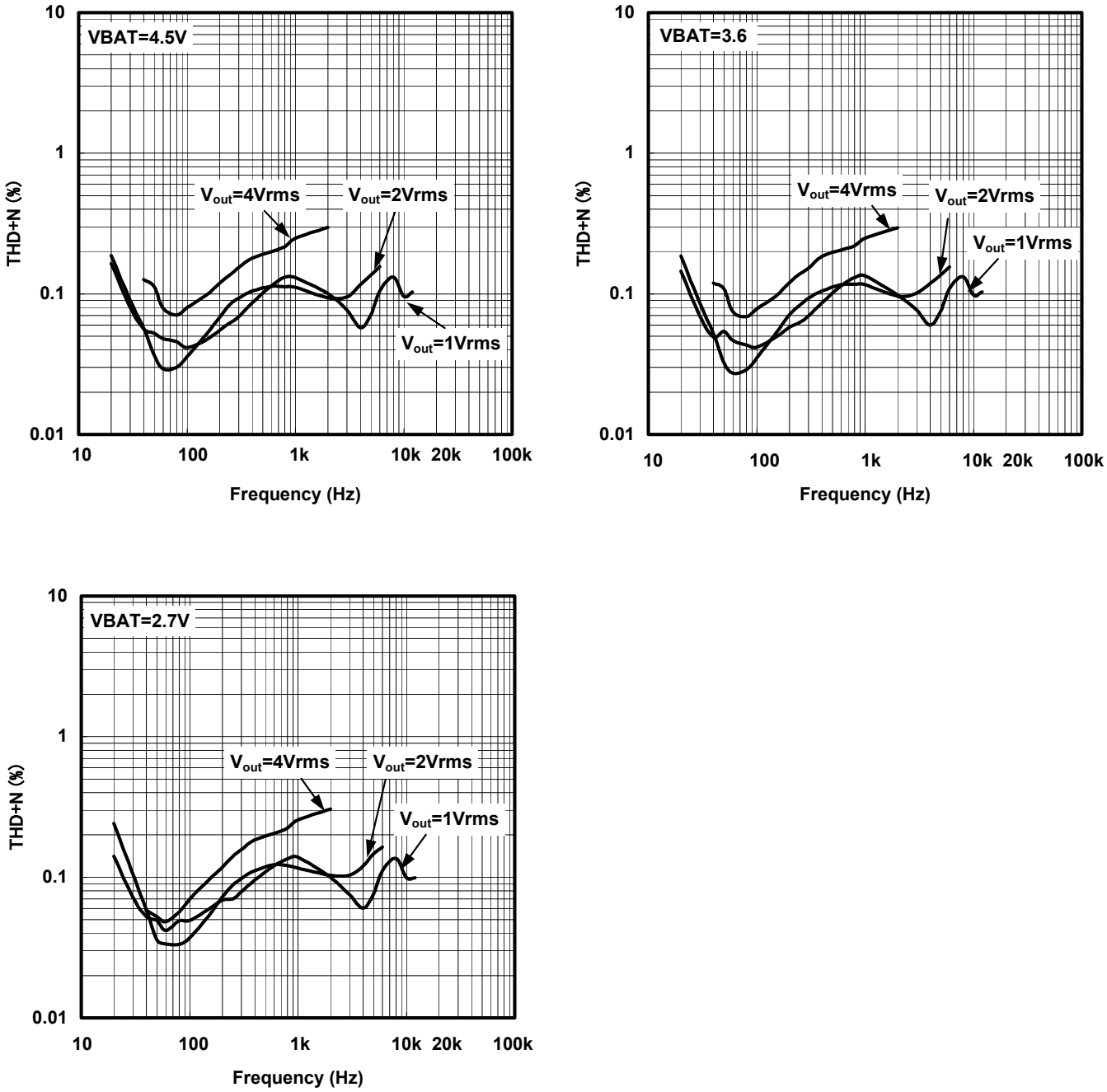
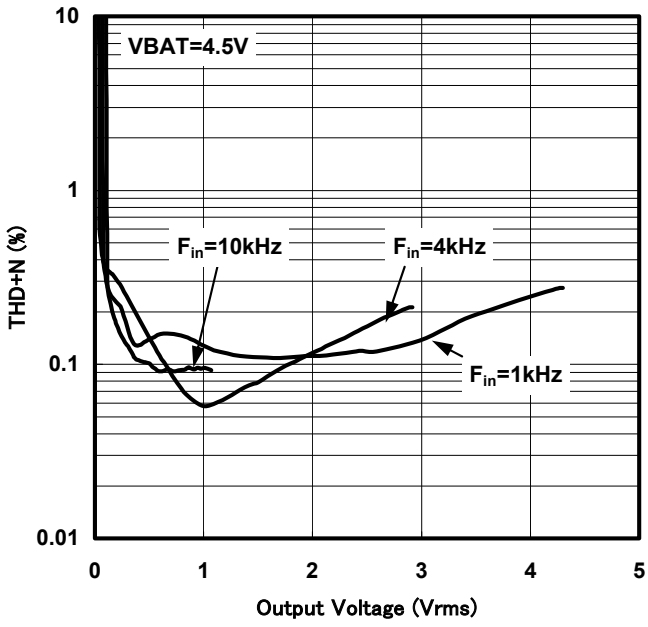
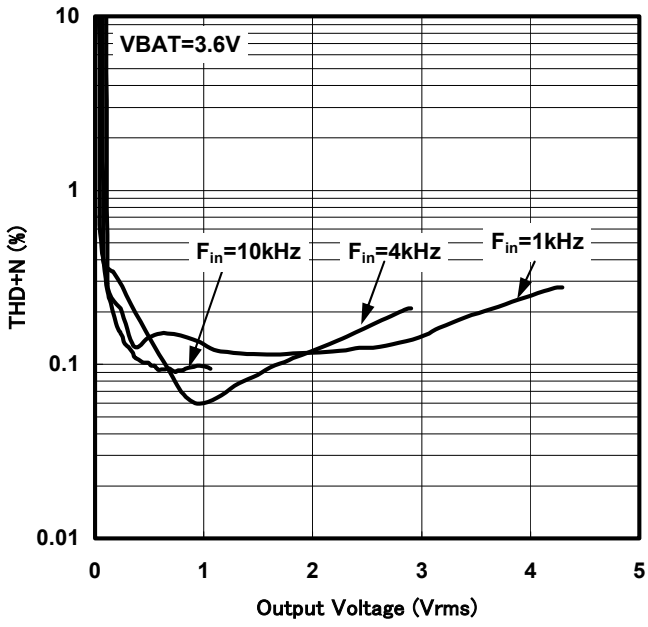


Figure. 7 Total Harmonic Distortion Plus Noise vs Frequency





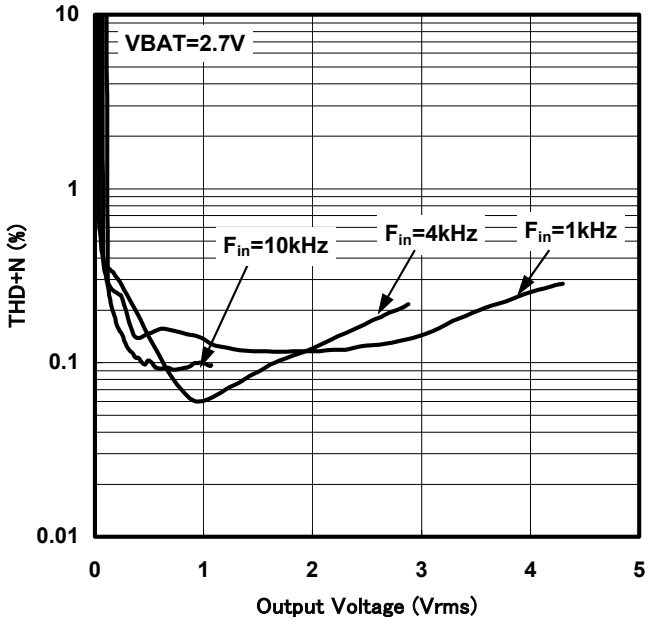


Figure. 8 Total Harmonic Distortion Plus Noise vs Output Voltage

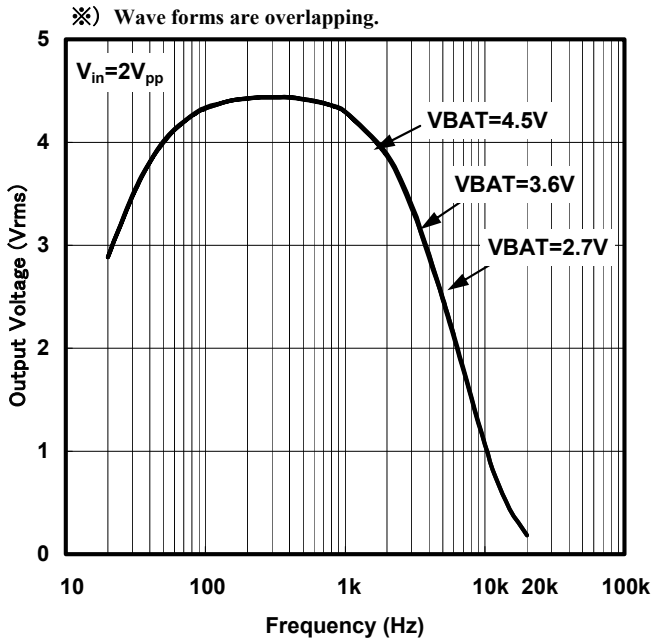


Figure. 9 Output Amplitude vs. Frequency

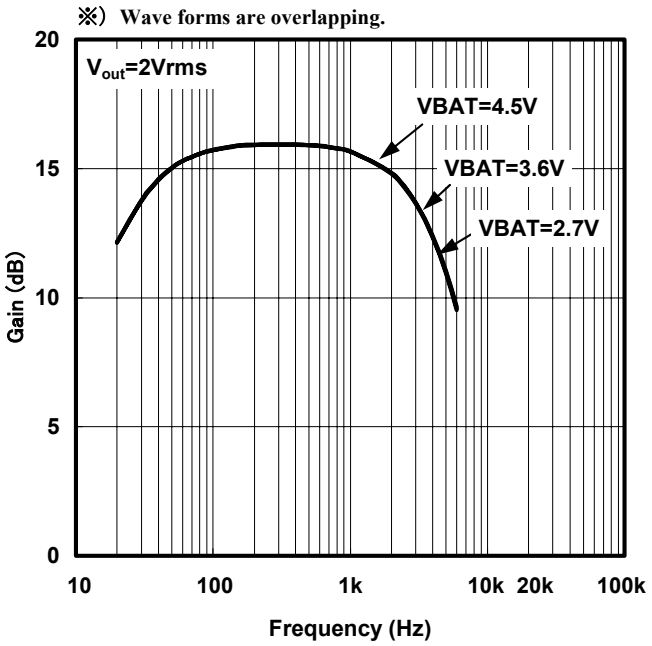


Figure. 10 Frequency Response

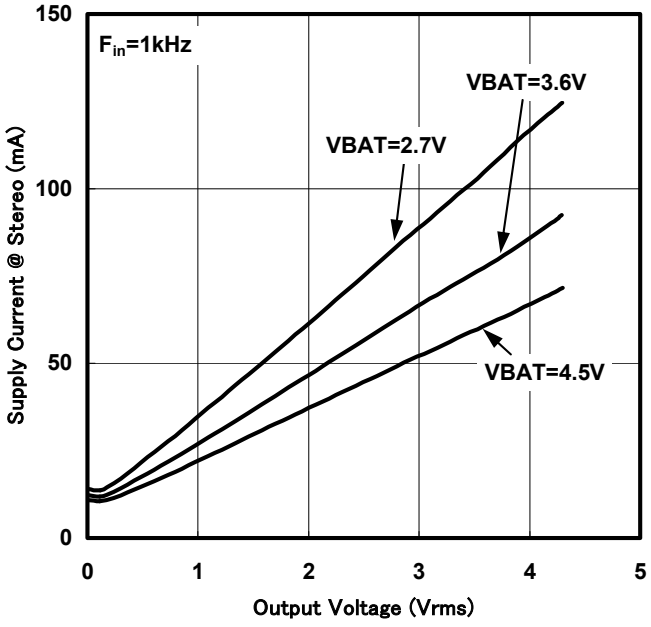


Figure. 11 Supply Current vs Output Voltage

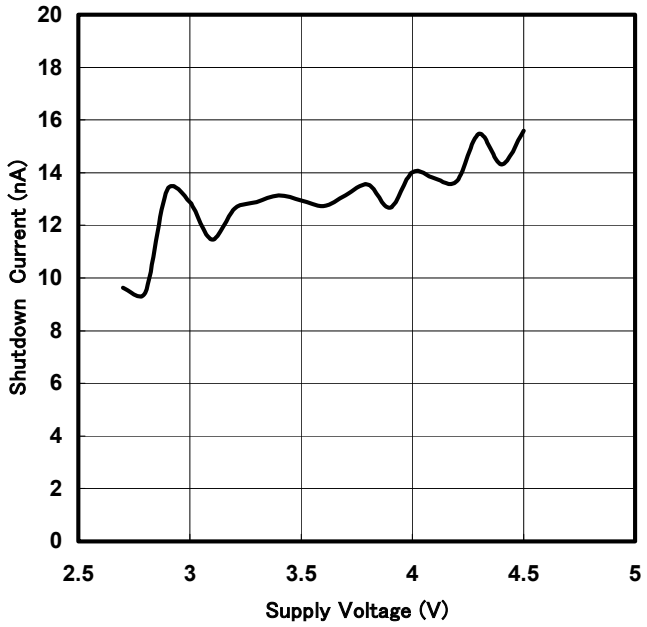


Figure. 12 Shutdown Current vs Supply Voltage

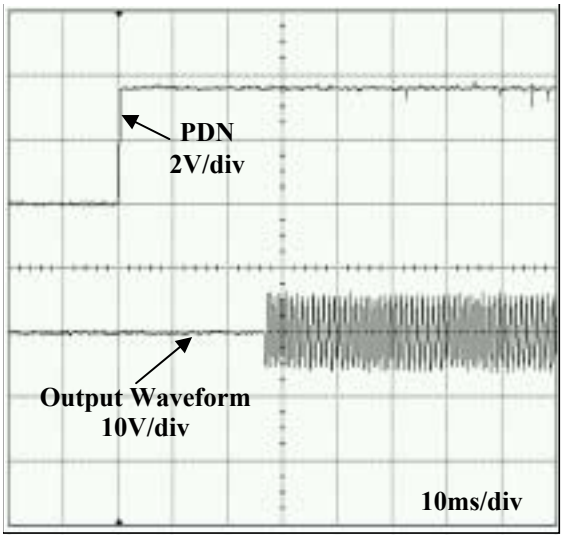


Figure. 13 Startup Waveform

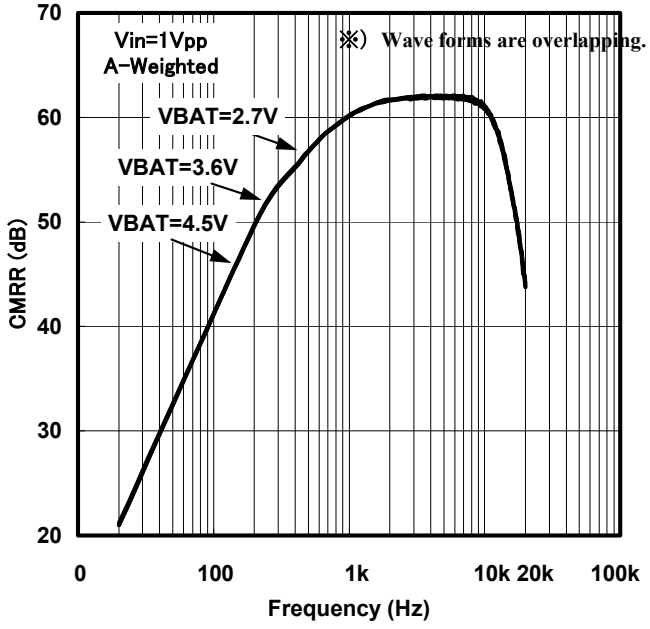


Figure. 14 Common-Mode Rejection Ratio vs Frequency

LEVEL DIAGRAM

Default gain of AK7841 is +15.6dB. Figure. 15.shows the level diagram of AK7841. Pre Gain value is adjustable by pin control as specified in Table.1.

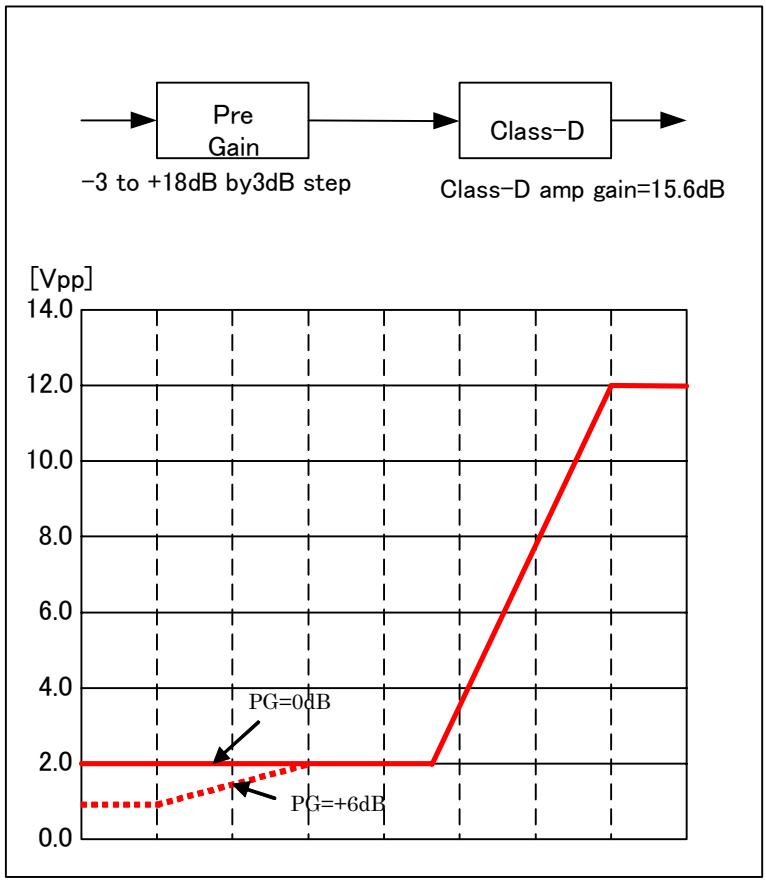


Figure. 15 Level Diagram

TYPICAL APPLICATION CIRCUIT

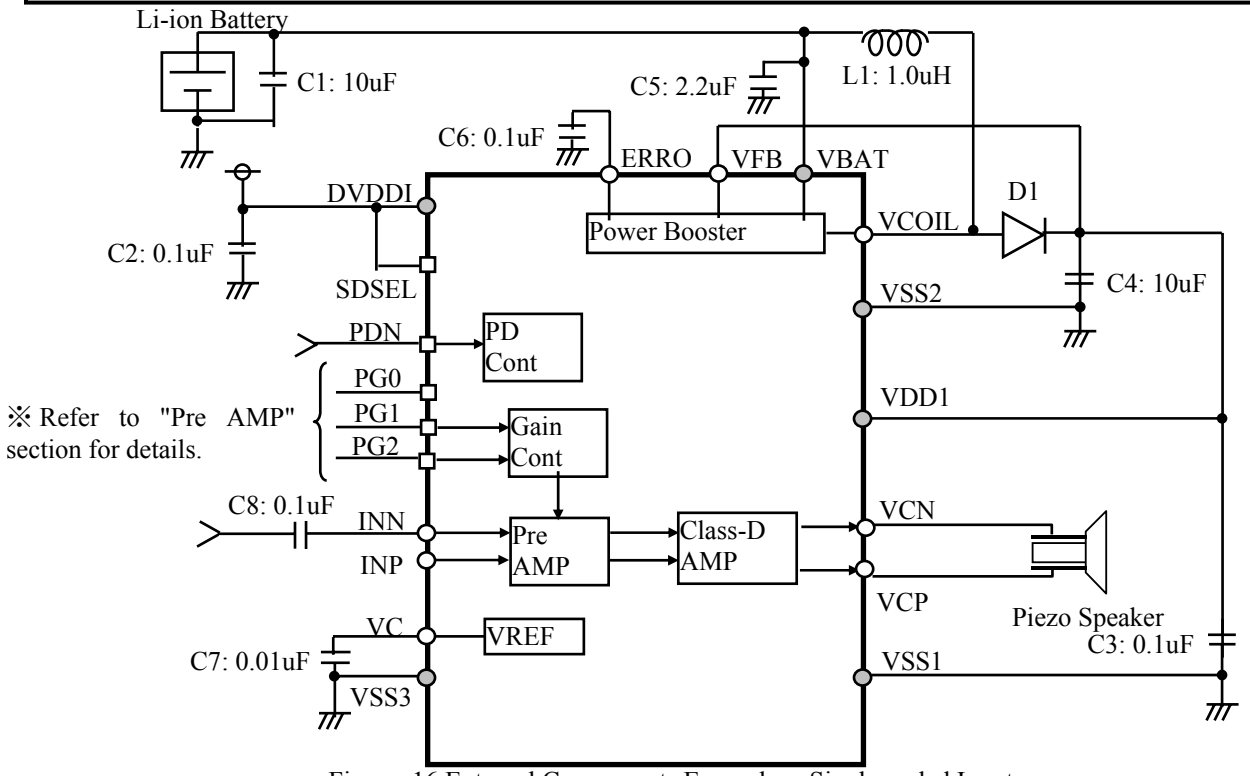


Figure. 16 External Components Examples : Single-ended Input

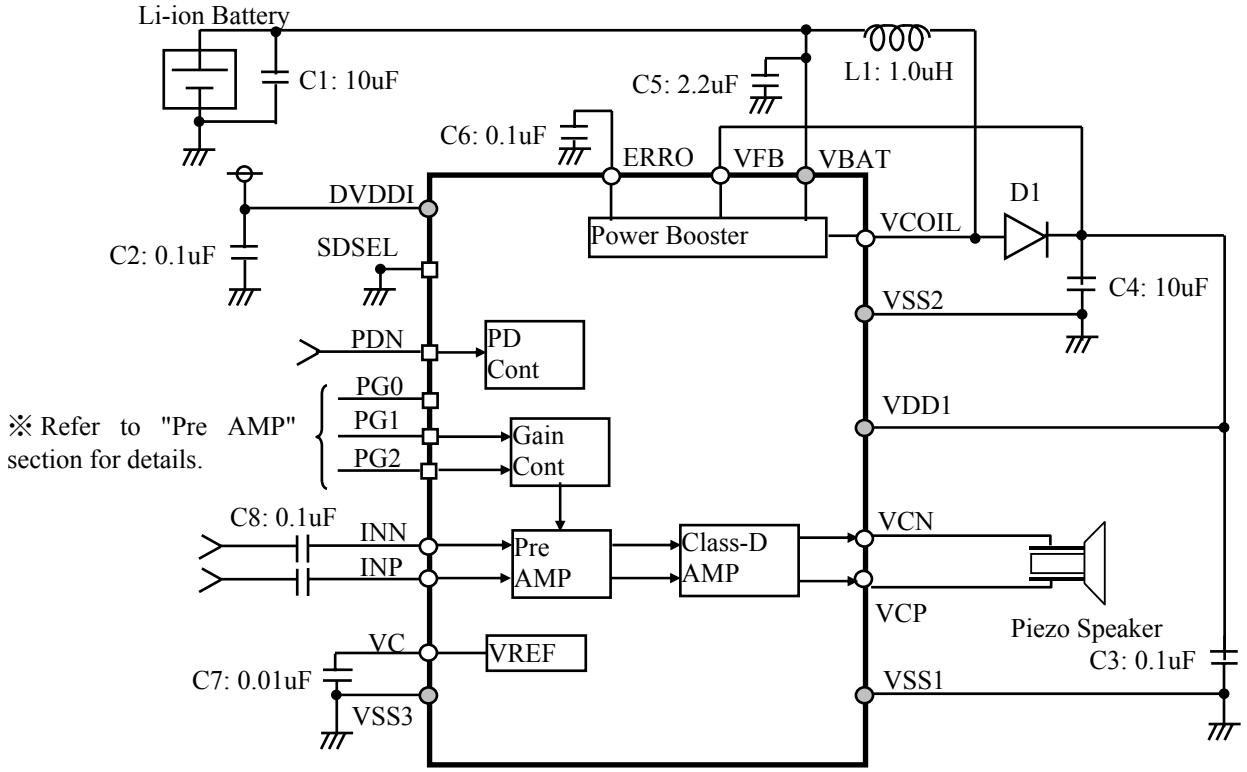


Figure. 17 External Components Examples :
Differential Input with ac coupling capacitors at input

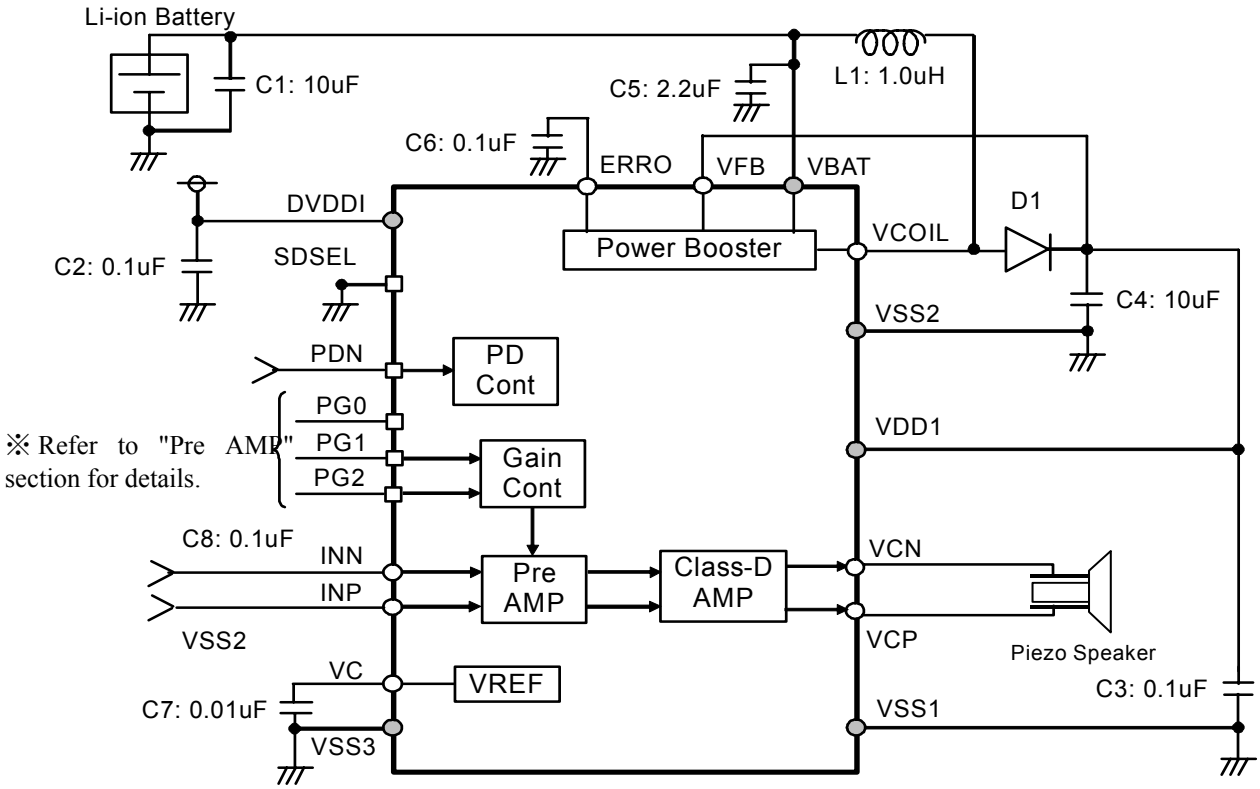


Figure. 18 External Components Examples : Differential Input, direct Connection ※

※If two conditions are fulfilled as below, ac-coupling capacitors are not needed.

1. **The voltage of INP and INN are VSS while shutting down.**
2. **The common level of INP and INN pin is between 0.8V and 1.6V, and input signals are within common level±0.5V for each pin (2Vpp).**

1. Grounding and Power Supply Decoupling

The AK7841 requires careful attention to power supply and grounding arrangements. Supply VBAT with Battery Power. VDD1 must be supplied with boosted flat voltage. Connect VSS1, VSS2 and VSS3 to analog ground plane. System analog and digital ground should be isolated from each other and be connected nearby the power supply pin on the printed circuit board. Decoupling capacitors should be as close to the power supply pins as possible, with the small value ceramic capacitor nearby power supply.

2. Voltage Reference

VC pin is the analog common voltage (ground for signals). Insert a 0.01μF ceramic capacitor between VC and VSS3 to eliminate the effects of high frequency noise. This capacitor should be as close to the VC pin as possible. Do not take out load current from the VC pin. All signals, especially clocks, should be kept away from the VC pin in order to avoid unwanted coupling.

3. Class-D Outputs

The Class-D outputs are in BTL signal format. Locate the outputs close to the speaker to minimize interconnect resistance and capacitance to suppress noise. Match the length and pattern of the plus and minus output interconnect. Keep AK7841 or Class-D outputs away as far away as possible from the devices such as antennas that are sensitive to high frequency noise.

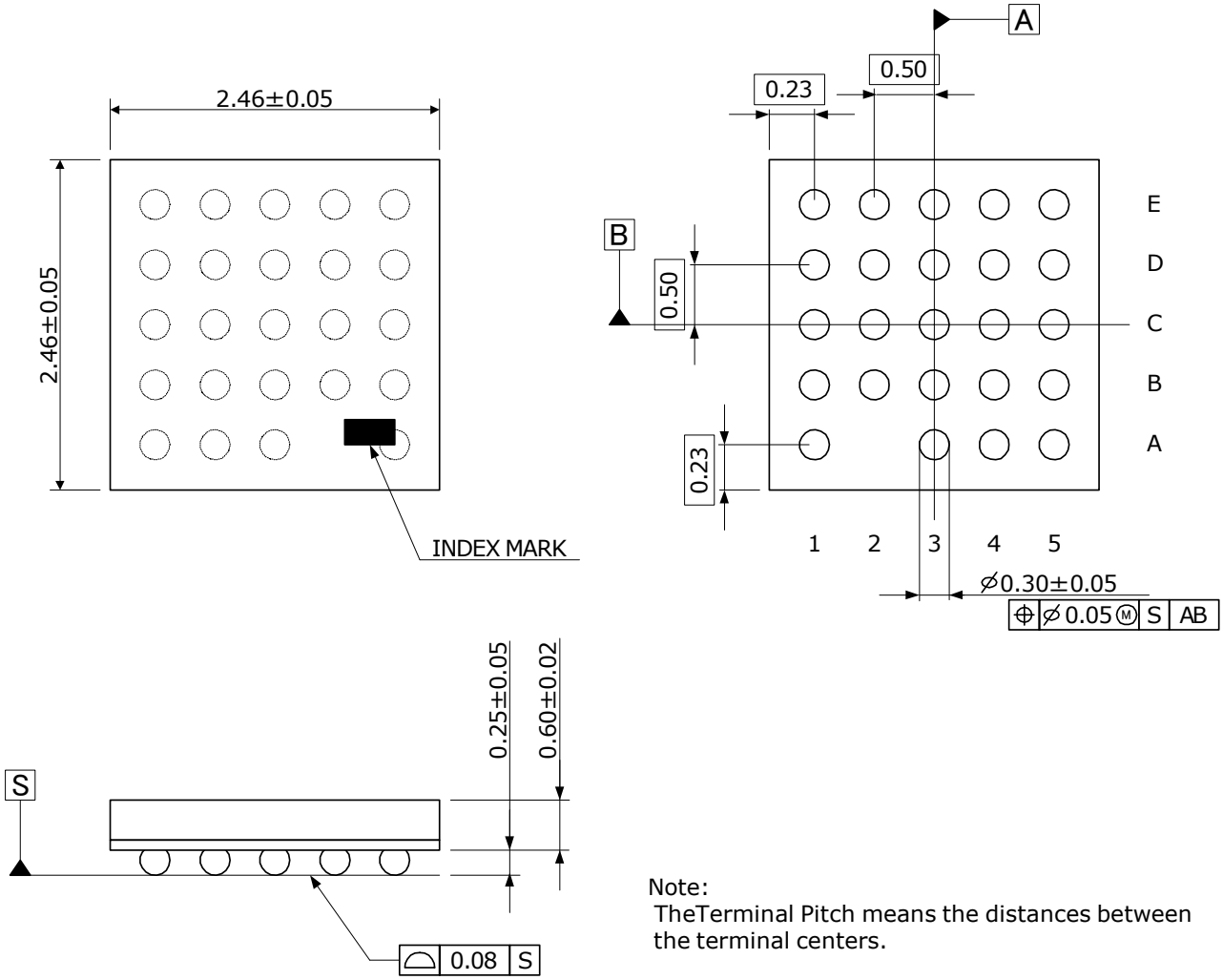
4. Effect on RF bands

Power Booster or Class-D Outputs may affect high frequency signal while applying to some applications.
Apply previous section (**3. Class-D Outputs)** in PCB layout.

5. Drivable Piezo Speakers

AK7841 is designed to drive typical piezo speakers but in some cases electric characteristics of the speakers differ by manufacturers. Feel free to ask us whether your speakers can be driven or not before using them.

PACKAGE



Note:
TheTerminal Pitch means the distances between the terminal centers.

Figure. 19 Package Dimensions (AK7841)

MARKING

(a) Market number : "7841"

(b) Date code(four digits)

Y : Last one digits of Christian year (ex. "2007" → "7")

WW : Manufactured week

L : Wafer lot number, which manufactured in same week ("A", "B", "C", ・・・)

(c) Index indication : "A2" pin location

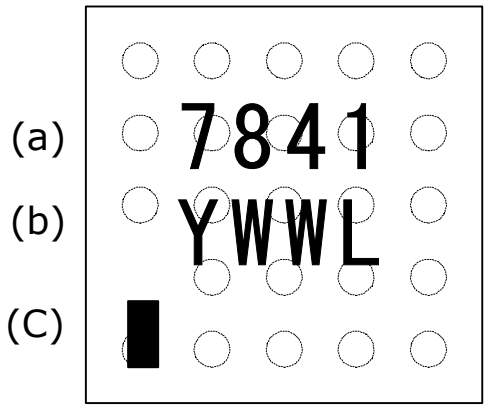


Figure. 20 Package Marking (AK7841)

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