AK7746

Audio DSP with 5-channel 24-bit ADC and Input Mux

1. General Description

The AK7746 is a highly integrated audio processor, including 5 A/D channels, an input mux that can select 2 stereo pairs from 8 stereo inputs, and an on-chip DSP. High quality analog performance is provided by the ADC's achieving 98dB (48kHz) dynamic range. The A/D supports sampling frequencies from 8kHz to 96kHz. The AK7746 includes 72kbits of SRAM for audio delay that is suitable for simulated surround functions and speaker compensation. The programmable DSP allows up to 4608 execution lines per audio sample cycle at 8kHz, 768 lines at 48kHz, or 384 lines at 96kHz with multiple functions per line. The AK7746 can be used to implement complete sound field control, such as echo, 3D, parametric equalization, etc. It is packaged in a 64-lead LQFP.

2. Features

DSP:

- **Word length:** **24-bit (Data RAM)**
- **Instruction cycle time:** **27ns (768fs, fs=48kHz)**
- **Multiplier:** **24 x 16 → 40-bit**
- **Divider:** **24 / 24 → 16-bit or 24-bit**
- **ALU:** **34-bit arithmetic operation (Overflow margin: 4bit)**
- **24-bit arithmetic and logic operation**
- **Shift+Register:** **1, 2, 3, 4, 6, 8 and 15 bits shifted left**
  1, 2, 3, 4, 8 and 15 bits shifted right
  (Other numbers in parentheses are restricted.
  Provided with indirect shift function)
- **Program RAM:** **768 x 32-bit**
- **Coefficient RAM:** **1024 x 16-bit**
- **Data RAM:** **256 x 24-bit**
- **Offset RAM:** **48 x 13-bit**
  (6144 x 12-bit / 3072 x 24-bit / 4096 x 12-bit + 1024 x 24-bit)
- **Internal Memory:** **72kbit SRAM**
- **Sampling frequency:** **8kHz to 96kHz**
- **Serial interface port for micro-controller**
- **Master clock:** **768fs@48kHz (generated by PLL from 256fs or 384fs)**
- **Master/Slave operation**
- **Serial signal input port (8(10) ch):16/20/24-bit : Output port (8ch + 4ch): 24-bit**

ADC: 4 channels (2 channels 2 sets)

- **24-bit 64 x Over-sampling delta sigma**
- **Sampling frequency:** **8kHz to 96kHz**
- **DR:** **98dBA (fs=48 kHz Full-differential Input)**
- **S/N :** **98dBA (fs=48 kHz Full-differential Input)**
- **S/(N+D) :** **91dB (fs= 48 kHz Full-differential Input)**
- **Digital HPF (fc = 1Hz)**
- **Single-ended or Full-differential Input**

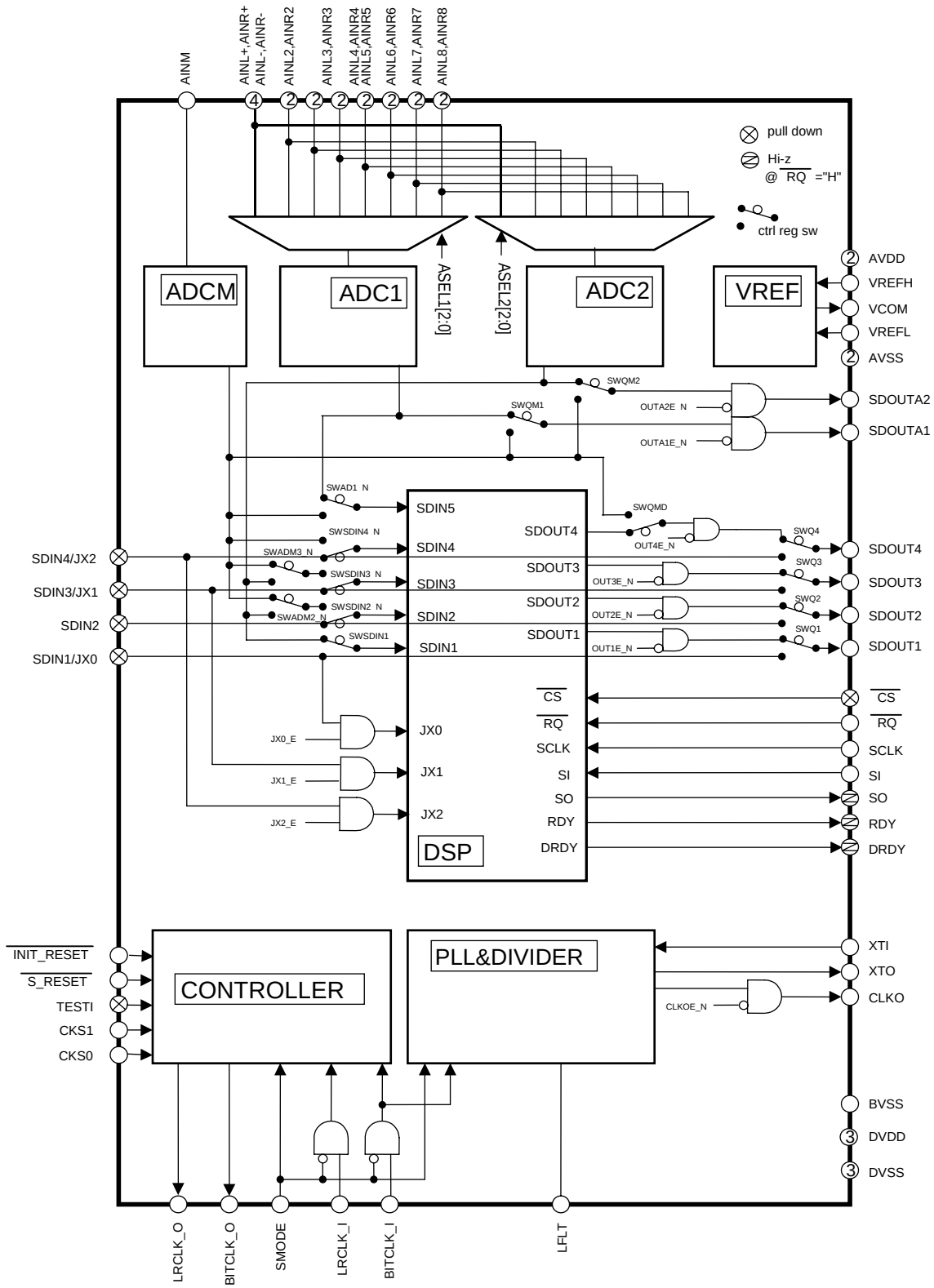
ADC: Monaural 1 channel

- **24-bit 64x Over-sampling delta sigma**
- **Sampling frequency:** **8kHz to 96kHz**
- **DR:** **97dBA (fs=48 kHz)**
- **S/N :** **97dBA (fs=48 kHz)**
- **S/(N+D) :** **91dB (fs= 48 kHz)**

Other

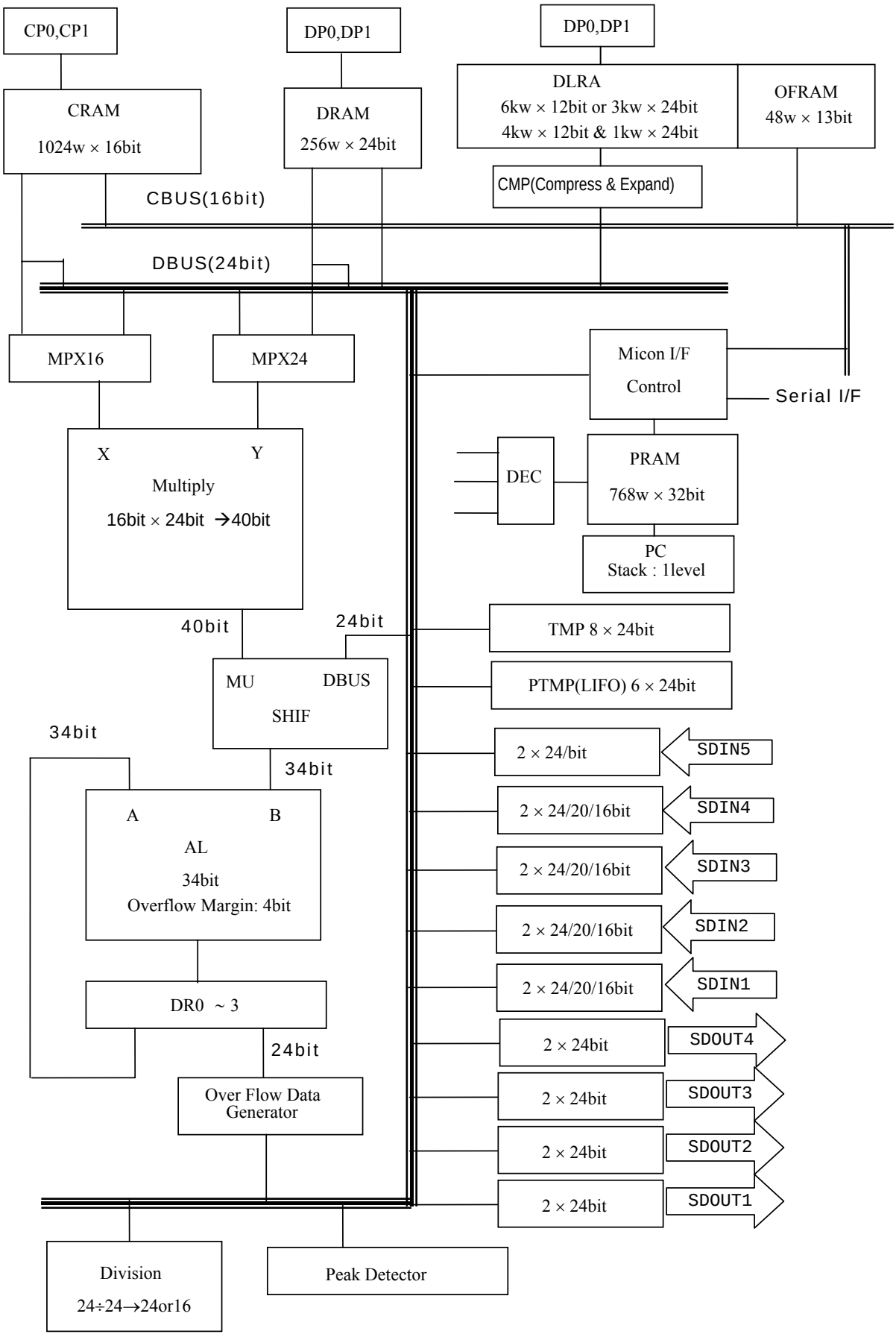
- **External Jump pin:** **3(maximum)**
- **CRC error check function**
- **LRCLK and BITCLK input and output for slave mode**
- **Power supply:** **+3.3V±0.3V**
- **Operating temperature range:** **-40°C~85°C**
- **Package:** **64pin LQFP (0.5mm pitch)**

3. Block diagram



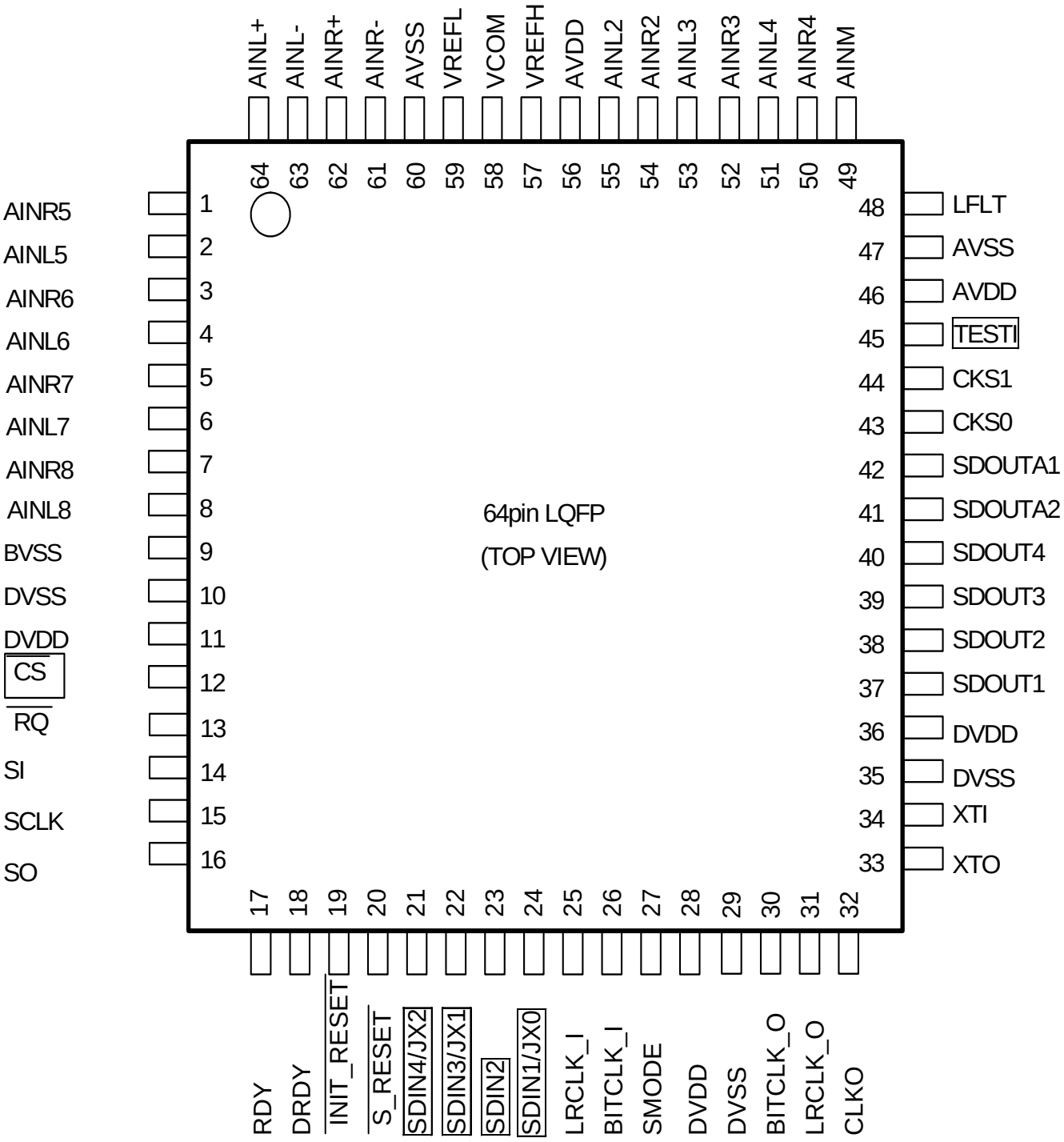
This block diagram is a simplified illustration of the AK7746; it is not a circuit diagram.
Ctrl reg SW describes default setting.

◆ AK7746 DSP Block diagram



4. Description of Input/Output Pins

(1) Pin layout



Note) *** is internal pull-down pin.

(2) Pin function

Pin No	Pin name	I/O	Function	Classification
1	AINR5	I	**ADC1 or ADC2 Rch single ended analog input 5**	Analog input
2	AINL5	I	**ADC1 or ADC2 Lch single ended analog input 5**	
3	AINR6	I	**ADC1 or ADC2 Rch single ended analog input 6**	
4	AINL6	I	**ADC1 or ADC2 Lch single ended analog input 6**	
5	AINR7	I	**ADC1 or ADC2 Rch single ended analog input 7**	
6	AINL7	I	**ADC1 or ADC2 Lch single ended analog input 7**	
7	AINR8	I	**ADC1 or ADC2 Rch single ended analog input 8**	
8	AINL8	I	**ADC1 or ADC2 Lch single ended analog input 8**	
9	BVSS	-	**Analog ground (Silicon base ground level)** Connect with AVSS pin	Analog Power supply
10	DVSS	-	**Digital Ground 0.0V**	Digital Power supply
11	DVDD	-	**Digital power supply 3.3V(typ)**	
12	$\overline{CS}$	I	**Chip select pin for Microcomputer interface. (Internal pull-down)** Normaly leave OPEN or connect with DVSS. $\overline{CS}$ ="H" : SI can not input, SO,RDY,DRDY = Hi-Z.	Microcomputer Interface
13	$\overline{RQ}$	I	**Write request pin for Microcomputer interface.** $\overline{RQ}$ ="L" : Microcomputer interface enable. For run-time data read out: $\overline{RQ}$ ="H". When Microcomputer interface is not used or during initial reset, leave $\overline{RQ}$ ="H".	
14	SI	I	**Serial data input and serial data output control pin for Microcomputer interface.** When SI is not used, leave SI="L".	
15	SCLK	I	**Serial data clock pin for Microcomputer interface.** When SCLK is not used, leave SCLK="H".	
16	SO	O	**Serial data output pin for Microcomputer interface.** $\overline{CS}$ ="H" : SO = Hi-Z.	
17	RDY	O	**Data write ready output pin for Microcomputer interface.** $\overline{CS}$ ="H" : RDY = Hi-Z.	
18	DRDY	O	**Output data ready pin for Microcomputer interface.** $\overline{CS}$ ="H" : DRDY = Hi-Z.	
19	$\overline{INIT\_RESET}$	I	**Reset pin (for initialization)** Used for initialization of the AK7746. When changing CKS1 or CKS0 and changing XTI input frequency, this pin setting is necessary.	Reset
20	$\overline{S\_RESET}$	I	**System Reset pin**	
21	SDIN4/JX2	I	**DSP serial data input pin / External condition jump pin (Internal pull-down)** * Compatible with MSB justified 24 bits / LSB justified 24,20 and 16 bits * It can change its function as a conditional jump pin JX2 by control register setting (JX2_E).	Digital section Serial input data / Conditional input
22	SDIN3/JX1	I	**DSP serial data input pin / External condition jump pin (Internal pull-down)** * Compatible with MSB justified 24 bits / LSB justified 24,20 and 16 bits * It can change its function as a conditional jump pin JX1 by control register setting (JX1_E).	Digital section Serial input data / Conditional input

Pin No	Pin name	I/O	Function	Classification
23	SDIN2	I	**DSP serial data input pin (Internal pull-down)** * Compatible with MSB justified 24 bits / LSB justified 24,20 and 16 bits	Digital section Serial input data
24	SDIN1/JX0	I	**DSP serial data input / External condition jump (Internal pull-down)** * Compatible with MSB justified 24 bits / LSB justified 24,20 and 16 bits * It can change its function as a conditional jump pin JX0 by control register setting (JX0_E).	Digital section Serial input data / Conditional input
25	LRCLK_I	I	**LR channel select clock input** Slave mode (SMODE="L") : Input the fs clock. Master mode (SMODE="H"): Connect to DVSS.	System Clock
26	BITCLK_I	I	**Serial bit clock input** Slave mode: Input 64 fs or 48 fs clocks. When it uses only for master mode then connect to DVSS. (SMODE="H")	
27	SMODE	I	**Slave / Master mode selector** SMODE="L": Slave mode. SMODE="H": Master mode.	Control
28	DVDD	-	**Digital Power supply pin 3.3V (typ)**	Digital Power supply
29	DVSS	-	**Digital Ground pin 0.0V**	
30	BITCLK_O	O	**Serial bit clock output** Master mode (SMODE="H") : Outputs 64fs clock. Slave mode (SMODE="L") : Outputs BITCLK_I clock.	System clock
31	LRCLK_O	O	**LR channel select clock output** Master mode (SMODE="H") : Outputs the fs clock. Slave mode (SMODE="L") : Outputs LRCLK_I clock.	
32	CLKO	O	**Clock output** Output frequency can be selectable by control register.	System clock
33	XTO	O	**Crystal oscillator output** When crystal oscillator is used, it should be connected to this pin and XTI. When the external clock is used, keep this pin open.	System clock
34	XTI	I	**Master clock input** Connect a crystal oscillator between this pin and the XTO pin, Or input the external CMOS clock signal to XTI pin.	
35	DVSS	-	**Digital Ground pin 0.0V**	Digital Power supply
36	DVDD	-	**Digital Power supply pin 3.3V (typ)**	

Pin No	Pin name	I/O	Function	Classification
37	SDOUT1	O	**DSP Serial data output** * Outputs MSB justified 24-bit data. * Allows the selectable output from SDIN1 by control register setting (SWQ1).	Digital section Serial output data
38	SDOUT2	O	**DSP Serial data output** * Outputs MSB justified 24-bit data. * Allows the selectable output from SDIN2 by control register setting (SWQ2).	
39	SDOUT3	O	**DSP Serial data output** * Outputs MSB justified 24-bit data. * Allows the selectable output from SDIN3 by control register setting (SWQ3).	
40	SDOUT4	O	**DSP Serial data output** * Outputs MSB justified 24-bit data. * Allows the selectable output from SDIN4 by control register setting (SWQ4).	
41	SDOUTA2	O	**ADC2 Serial data output** * Outputs MSB justified 24-bit data. * Allows the selectable output from ADCM by control register setting (SWQM2).	
42	SDOUTA1	O	**ADC1 Serial data output** * Outputs MSB justified 24-bit data. * Allows the selectable output from ADCM by control register setting (SWQM1).	
43	CKS0	I	**Master clock (XTI or BITCLK_I) select**	Control
44	CKS1	I	**Master clock (XTI or BITCLK_I) select**	
45	TESTI	I	**Test pin (Internal pull-down)** * Normally , connect to DVSS pin.	TEST

Pin No	Pin name	I/O	Function	Classification
46	AVDD	-	**Analog Power supply pin 3.3V (typ)**	Analog Power Supply
47	AVSS	-	**Analog Ground 0.0V**	
48	LFLT	O	**Filter connection pin for PLL** When using the PLL function, connect a 22kΩ resistor and a 1.5nF capacitor in series to the analog ground (AVSS)	Analog output
49	AINM	I	**ADCM Monaural single ended input**	Analog input
50	AINR4	I	**ADC1 or ADC2 Rch single ended input 4**	
51	AINL4	I	**ADC1 or ADC2 Lch single ended input 4**	
52	AINR3	I	**ADC1 or ADC2 Rch single ended input 3**	
53	AINL3	I	**ADC1 or ADC2 Lch single ended input 3**	
54	AINR2	I	**ADC1 or ADC2 Rch single ended input pin 2**	
55	AINL2	I	**ADC1 or ADC2 Lch single ended input pin 2**	
56	AVDD	-	**Analog Power Supply 3.3V (typ)**	Analog Power supply
57	VREFH	I	**Analog reference voltage input** Normally, connect to AVDD, and connect 0.1μF and 10μF capacitors between this pin and AVSS.	Analog input
58	VCOM	O	**Common voltage** Normally, connect 10μF and 0.1μFcapacitor between this pin and AVSS. Don't connect to other circuitry.	Analog output
59	VREFL	I	**Analog reference voltage input pin for low-level.** Normally, connect to AVSS.	Analog input
60	AVSS	-	**Analog Ground 0.0V**	Analog Power Supply
61	AINR-	I	**ADC1 or ADC2 Rch analog inverted input**	Analog input
62	AINR+	I	**ADC1 or ADC2 Rch analog non-inverted input**	
63	AINL-	I	**ADC1 or ADC2 Lch analog inverted input**	
64	AINL+	I	**ADC1 or ADC2 Lch analog non-inverted**	

Note) Do NOT leave open digital input pins unless they are internally pulled down and BITCLK_I, LRCLK_I in master mode.
(If you do not use pull-down pin, leave open or connects to DVSS. However, TESTI pin should connect to DVSS.)
* If analog input pins (1~8, 49~55, 61~64 pin) are not used, leave them open.

5. Absolute Maximum Rating

(AVSS, BVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Parameter	Symbol	min	max	Unit
Power supply voltage				
Analog(AVDD)	VA	-0.3	4.6	V
Digital(DVDD)	VD	-0.3	4.6	V
|AVSS(BVSS)-DVSS| Note 1)	ΔGND		0.3	V
Input current (except for power supply pin)	IIN	-	±10	mA
Analog input voltage AINL+,AINL-,AINR+,AINR-,	VINA	-0.3	VA+0.3	V
Digital input voltage	VIND	-0.3	VA+0.3	V
Operating ambient temperature	Ta	-40	85	°C
Storage temperature	Tstg	-65	150	°C

Note 1) AVSS(BVSS) should be same level as DVSS.
WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operations are not guaranteed at maximum rating conditions.

6. Recommended Operating Conditions

(AVSS, BVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Parameter	Symbol	min	typ	max	Unit
Power supply voltage					
AVDD	VA	3.0	3.3	3.6	V
DVDD	VD	3.0	3.3	VA	V
Reference voltage (VREF)					
VREFH Note 1)	VRH		VA		V
VREFL Note 2)	VRL		0.0		V

Note 1) VREFH normally connects with AVDD.
Note 2) VREFL normally connects with AVSS

Note: The analog input voltage and output voltage are proportional to the VREFH-VREFL voltages.

7. Electric Characteristics

(1) Analog characteristics

(Unless otherwise specified, Ta = 25°C; AVDD, DVDD = 3.3V; VREFH = AVDD, VREFL = AVSS;
BITCLK = 64 fs; Signal frequency 1 kHz;
Measurement bandwidth = 20 Hz to 20 kHz @48 kHz, 20 Hz to 40 kHz @96kHz;
ADC with all differential inputs, CLKO output = 18.432MHz; XTI = 18.432MHz, SMODE = "H")

	Parameter		min	typ	max	Unit
	Resolution				24	Bits
	Dynamic characteristics					
Stereo ADC Section **ADC1 ADC2**	S/(N+D) fs = 48kHz (-1dBFS)	(Note1)	81	91		dB
	fs = 96kHz (-1dBFS)			88		dB
	Dynamic range fs = 48kHz (A filter)	(Note 1,2)	88	98		dBFS
	fs = 96kHz			94		dBFS
	S/N fs = 48kHz (A filter)		88	98		dBFS
	fs = 98kHz			94		dBFS
	Inter-channel isolation (f=1kHz)	(Note 3)	90	115		dB
	DC accuracy					
	Inter-channel gain mismatching			0.1	0.3	dB
	Analog input					
	Input voltage (differential inputs)	(Note 4)	±1.85	±2.00	±2.15	Vp-p
	Input voltage (single ended)	(Note 5)	1.85	2.00	2.15	Vp-p
	Input impedance (fs=48kHz)	(Note 6)	22	33		kΩ
Monaural ADC Section **ADCM**	**Resolution**				24	Bits
	Dynamic characteristics					
	S/(N+D) fs = 48kHz (-1dBFS)		76	91		dB
	fs = 96kHz (-1dBFS)			88		dB
	Dynamic range fs = 48kHz (A filter)	(Note2)	80	97		dBFS
	fs = 96kHz			93		dBFS
	S/N fs = 48kHz (A filter)		80	97		dBFS
	fs = 98kHz			93		dBFS
	Analog input					
	Input voltage	(Note 7)	1.85	2.00	2.15	Vp-p
	Input impedance	(Note 8)	22	33		kΩ

Note 1) This value is not guaranteed with single-ended input operation
Note 2) Indicates S/(N+D) when -60 dBFS signal is applied
Note 3) Specified for L-ch and R-ch of each input selector with a -1dBFS signal
Note 4) This applies to AINL+, AINL-, AINR+ and AINR-.
Full-scale range (ΔAIN = (AIN+) - (AIN-)) is represented by (±FS = ± (VREFH-VREFL) × (2.0/3.3)).
Note 5) This applies to AINL2~L8 and AINR2~R8.
The full-scale of single-snded input is (FS=(VREFH-VREFL) × (2.0/3.3)).
Note 6) This applies to AINL+, AINL-, AINR+, AINR-, AINL2~L8 and AINR2~R8.
Note 7) This applies to AINM.
Full-scale range is represented by (FS = ±(VREFH-VREFL) × (2.0/3.3)).
Note 8)) This applies to AINM.

(2) DC Characteristics

(VDD=AVDD=DVDD=3.0~3.6V, Ta=25°C)

Parameter	Symbol	min	typ	max	Unit
High level input voltage	VIH	80% of VDD			V
Low level input voltage	VIL			20% of VDD	V
High level output voltage Iout=-100μA	VOH	VDD-0.5			V
Low level output voltage Iout=100μA	VOL			0.5	V
Input leak current Note 1)	Iin			±10	μA
Input leak current (pull-down) Note 2)	Iid		22		μA
Input leak current (XTI pin)	Iix		50		μA

Note 1) The pull-down pins and XTI pin are not included.

Note 2) The pull-down pins are: $\overline{CS}$, SDIN4/JX2, SDIN3/JX1, SDIN2, SDIN1/JX0, TESTI

Note:

Regarding the input/output levels in the text, the low level will be represented as "L" or 0, and the high level as "H" or 1. In principle, "0" and "1" will be used to represent the bus (serial/parallel) such as registers.

(3) Current Consumption

(AVDD=DVDD=3.0V~3.6V, Ta=25°C; master clock (XTI)=18.432MHz=384fs[fs=48kHz];
PLL is in active mode.)

Parameter	min	typ	max	Unit
Power supply current Note 1)				
1)Normal Speed				
a) AVDD		40		mA
b) DVDD		45		mA
c) total(a+b)		85		mA
2)Double Speed Note 2)				
a) AVDD		42	60	mA
b) DVDD		53	90	mA
c) total(a+b)		95	150	mA
3) $\overline{INIT\_RESET}$ ="L"(reference) Note 3)		2		mA

Note 1) Varies slightly different according to the system frequency and contents of the DSP program.

Note 2) Max value is “Double Speed” mode.

Note 3) This is a reference value when using the crystal oscillator. Because most of the power current at the initial reset state is in the oscillator section, the value may vary slightly according to the type of crystal oscillators and external circuits. This is a reference value only.

(4) Digital Filter Characteristics

Values described below are design values cited as references.

1) ADC Section (ADC1, ADC2):

(Ta=25°C; AVDD, DVDD =3.0V~3.6V; fs=48 kHz; HPF=off (Note1))

Parameter	Symbol	min	typ	max	Unit
Digital filter					
Pass band (±0.005dB) Note 2) (-0.02dB) (-6.0dB)	PB	0 - -	 21.768 24.00	21.5 - -	kHz kHz kHz
Stop band	SB	26.5			kHz
Pass band ripple (Note 2)	PR			±0.005	dB
Stop band attenuation (Note3,4)	SA	80			dB
Group delay distortion	ΔGD			0	us
Group delay (Ts=1/fs)	GD		29.3		Ts
Digital filter + SFC					
Amplitude characteristics (0~20.0kHz)			±0.01		dB

Note 1) HPF response is not included
Note 2) The passband is from DC to 21.5 kHz when fs = 48 kHz.
Note 3) The stopband is from 26.5 kHz to 3.0455MHz when fs = 48 kHz.
Note 4) When fs = 48 kHz, the analog modulator samples the analog input at 3.072MHz. The input signal is not attenuated by the digital filter in the multiple bands (n x 3.072MHz ± 21.99kHz; n=0, 1, 2, 3...) of the sampling frequency.

2) Monaural ADC Section (ADCM):

(Ta=25°C; AVDD, DVDD =3.0V~3.6V; fs=48 kHz; HPF=off (Note1))

Parameter	Symbol	min	typ	max	Unit
Digital filter					
Pass band (±0.005dB) Note 2) (-0.02dB) (-6.0dB)	PB	0 - -	 21.768 24.00	21.5 - -	kHz kHz kHz
Stop band	SB	26.5			kHz
Pass band ripple (Note 2)	PR			±0.005	dB
Stop band attenuation (Note3,4)	SA	80			dB
Group delay distortion	ΔGD			0	us
Group delay (Ts=1/fs)	GD		29.3		Ts
Digital filter + SFC					
Amplitude characteristics (0~20.0kHz)			±0.1		dB

Note 1) HPF response is not included
Note 2) The passband is from DC to 21.5 kHz when fs = 48 kHz.
Note 3) The stopband is from 26.5 kHz to 3.0455MHz when fs = 48 kHz.
Note 4) When fs = 48 kHz, the analog modulator samples the analog input at 3.072MHz. The input signal is not attenuated by the digital filter in the multiple bands (n x 3.072MHz ± 21.99kHz; n=0, 1, 2, 3...) of the sampling frequency.

(5) Switching Characteristics

5-1) System clock

(AVDD=DVDD=3.0V~3.6V,Ta=-40~85°C)

Parameter	Symbol	min	typ	max	Unit
Master clock (XTI)					
a) With a crystal oscillator: Note 1)					
CKS[1:0]=0h	fMCLK	-	16.9344 18.432	-	MHz
CKS[1:0]=1h	fMCLK	-	11.2896 12.288	-	MHz
b) With an external clock: Note 1)					
Duty factor (≤18.5MHz) (>18.5MHz)		40 45	50 50	60 55	% %
CKS[1:0]=0h	fMCLK	16.0		18.6	MHz
CKS[1:0]=1h	fMCLK	11.0		12.4	MHz
CKS[1:0]=2h @SMODE="L" (BITCLK_I input)	fXTI	———		———	MHz
CKS[1:0]=2h @SMODE="H" (PLL enable frequency)	fXTI	2.75		3.1	MHz
Clock rise time Clock fall time	tCR tCF			6 6	ns ns
LRCLK Sampling Frequency	fs	8	48	96	kHz
Slave mode :clock rise time Slave mode :clock fall time	tLR tLF			8 8	ns ns
BITCLK_I, BITCLK Frequency Note 3) (@CKS[1:0]≠ 2h)	fBCLK	48		64	fs
Slave mode: High level width Slave mode: Low level width	tBCLKH tBCLKL	70 70			ns ns
Slave mode :clock rise time Slave mode :clock fall time	tBR tBF			6 6	ns ns
BITCLK_I, BITCLK Frequency Note 4) (@CKS[1:0]=2h, SMODE="L") (PLL enable frequency)	fBCLK	— 2.75	64	— 3.1	fs MHz
Duty		40	50	60	%
Slave mode: High level width Slave mode: Low level width	tBCLKH tBCLKL	140 140			ns ns
Slave mode :clock rise time Slave mode :clock fall time	tBR tBF			6 6	ns ns

Note 1) CKS[1]=CKS1, CKS[0]=CKS0

Note 2) LRCLK and sampling rate (fs) must be matched.

Note 3) 48fs is enabled in slave mode.

Note 4) When using BITCLK_I as master clock. Accurate 64 divide clock is required during 1fs.
(Available fs are 44.1kHz and 48kHz).

5-2) Reset

(AVDD=DVDD=3.0V~3.6V,Ta=-40~85°C)

Parameter	Symbol	min	typ	max	Unit
$\overline{\text{INIT\_RESET}}$ Note 1)	tRST	600			ns
$\overline{\text{S\_RESET}}$	tRST	600			ns

Note 1) When "H", the AK7746 needs a stable master clock input to the device.

5-3) Audio Interface

(AVDD=DVDD=3.0~3.6V,Ta=-40°C ~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave mode					
BITCLK_I frequency	fBCLK	48	64	64	fs
Delay time from BITCLK_I"↑" to LRCLK_I Note1)	tBLRD	40			ns
Delay time from LRCLK_I to BITCLK_I "↑" Note1)	tLRBD	40			ns
Delay time from LRCLK_O to serial data output	tLRD			40	ns
Delay time from BITCLK_O to serial data output	tBSOD			40	ns
Serial data input latch setup time	tBSIDS	40			ns
Serial data input latch hold time	tBSIDH	40			ns
Master mode					
BITCLK_O frequency	fBCLK		64		fs
BITCLK_O duty factor			50		%
Delay time from LRCLK_O to serial data output	tLRD			40	ns
Delay time from BITCLK_O to serial data output	tBSOD			40	ns
Serial data input latch setup time	tBSIDS	40			ns
Serial data input latch hold time	tBSIDH	40			ns

Note 1) This feature is to avoid LRCLK_I edge and BITCLK_I "↑"edge.

5-4) Microcomputer Interface

(AVDD=DVDD=3.0V~3.6V, Ta=-40~85°C, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcomputer Interface Signal					
$\overline{RQ}$ Fall time	tWRF			30	ns
$\overline{RQ}$ Rise time	tWRR			30	ns
SCLK fall time	tSF			30	ns
SCLKrise time	tSR			30	ns
SCLK frequency	1/fSCLK			1.4	MHz
SCLK low level width	tSCLKL	350			ns
SCLK high level width	tSCLKH	350			ns
Microcomputer to AK7746					
Time from $\overline{RESET}$ "↓" to $\overline{RQ}$ "↓"	tREW	500			ns
Time from $\overline{RQ}$ "↑" to $\overline{RESET}$ "↑" Note 1)	tWRE	500			ns
$\overline{RQ}$ high level width	tWRQH	500			ns
Time from $\overline{RQ}$ "↓" to SCLK"↓"	tWSC	500			ns
Time from SCLK"↑" to $\overline{RQ}$ "↑"	tSCW	800			ns
SI latch setup time	tSIS	300			ns
SI latch hold time	tSIH	300			ns
AK7746 to microcomputer					
Time from SCLK"↑" to DRDY"↓"	tSDR			600	ns
Time from SI"↑"to DRDY"↓"	tSIDR			600	ns
SI high level width	tSIH	600			ns
Delay time from SCLK"↓" to SO output	tSOS			300	ns
Hold time from SCLK"↑" to SO output	tSOH	150			ns
AK7746 to microcomputer (RAM DATA read-out)					
SI latch setup time (SI="H")	tRSISH	300			ns
SI latch setup time (SI="L")	tRSISL	300			ns
SI latch hold time	tRSIH	300			ns
Time from SCLK"↓" to SO output	tSOD			300	ns
AK7746 to microcomputer (CRC result out) (Note 2)					
Delay time from $\overline{RQ}$ "↑" to SO output	tRSOC			400	ns
Delay time from $\overline{RQ}$ "↓" to SO output (Note 3)	tFSOC	300			ns
$\overline{CS}$					
$\overline{CS}$ Fall time	tCSF			30	ns
$\overline{CS}$ Rise time	tCSR			30	ns
Time from $\overline{S\_RESET}$ "↓" to $\overline{CS}$ "↓"	tWRCS	600			ns
Time from $\overline{CS}$ "↑" to $\overline{S\_RESET}$ "↑"	tWCSR	600			ns
$\overline{CS}$ high level width	tWCSH	1000			ns
Time from $\overline{CS}$ "↓" to $\overline{RQ}$ "↓"	tWCSRQ	600			ns
Time from $\overline{RQ}$ "↑" to $\overline{CS}$ "↑"	tWRQCS	600			ns
$\overline{CS}$ "↓" to SO,RDY,DRDY Hi-Z release	tCSHR			600	ns
$\overline{CS}$ "↑" to SO,RDY,DRDY Hi-Z	tCSHS			600	ns

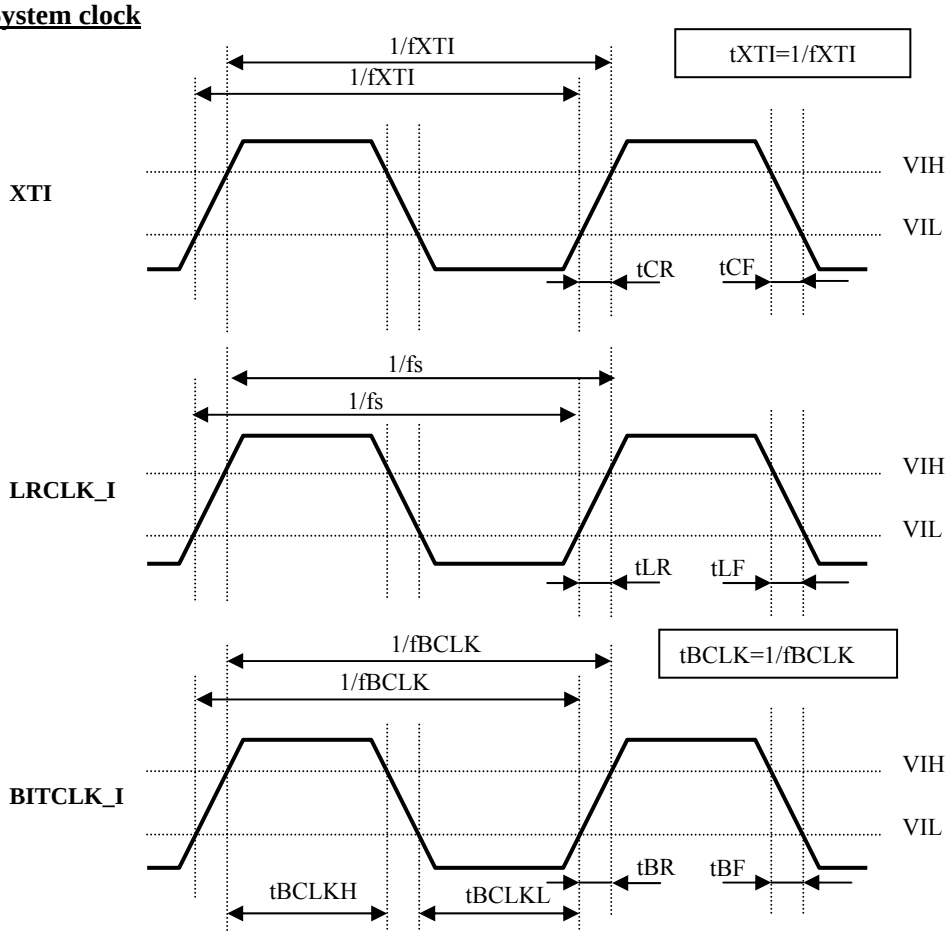
Note 1) Except for external jump code set at reset state.

Note 2) If there is excess serial data D(x) and when divided by G(x) it is equal to R(x), then SO = "H".

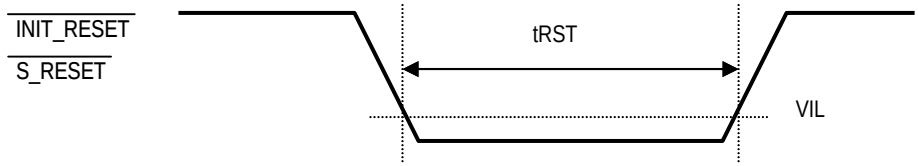
Note 3) Must read for more than 300ns before $\overline{RQ}$ falls .

(6) Timing Waveform

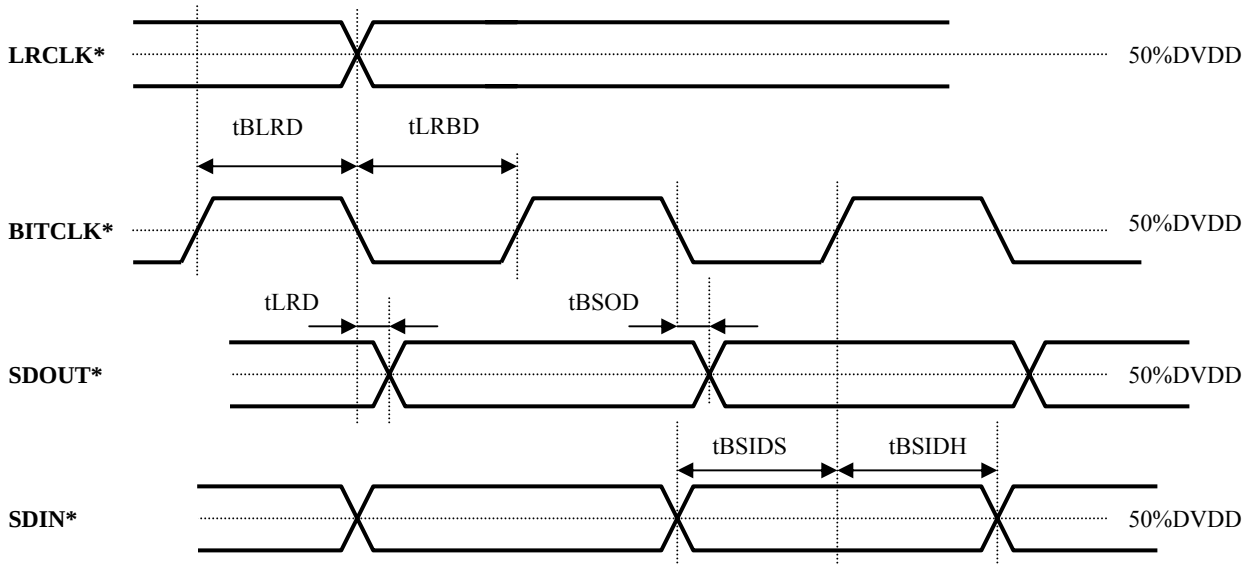
6-1) System clock



6-2) RESET



6-3) Audio interface



LRCLK* : LRCLK_I, LRCLK_O

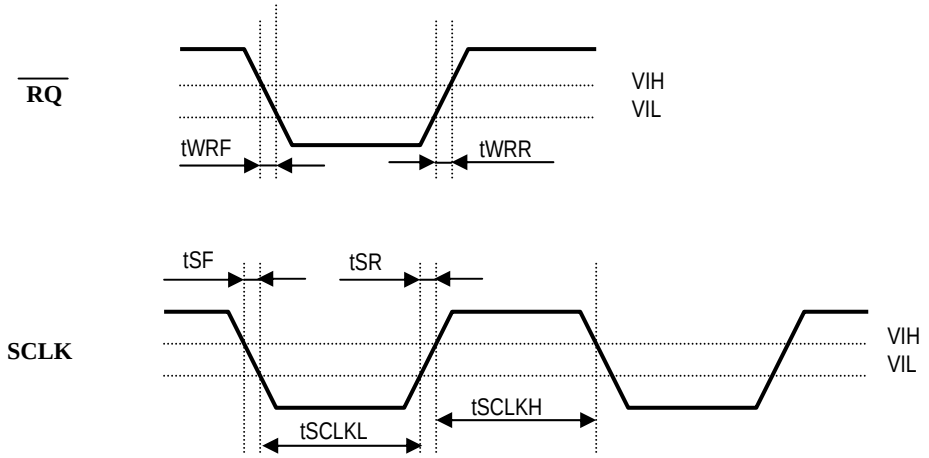
BITCLK* : BITCLK_I, BITCLK_O

SDOUT* : SDOUT1~4,SDOUTA1~2

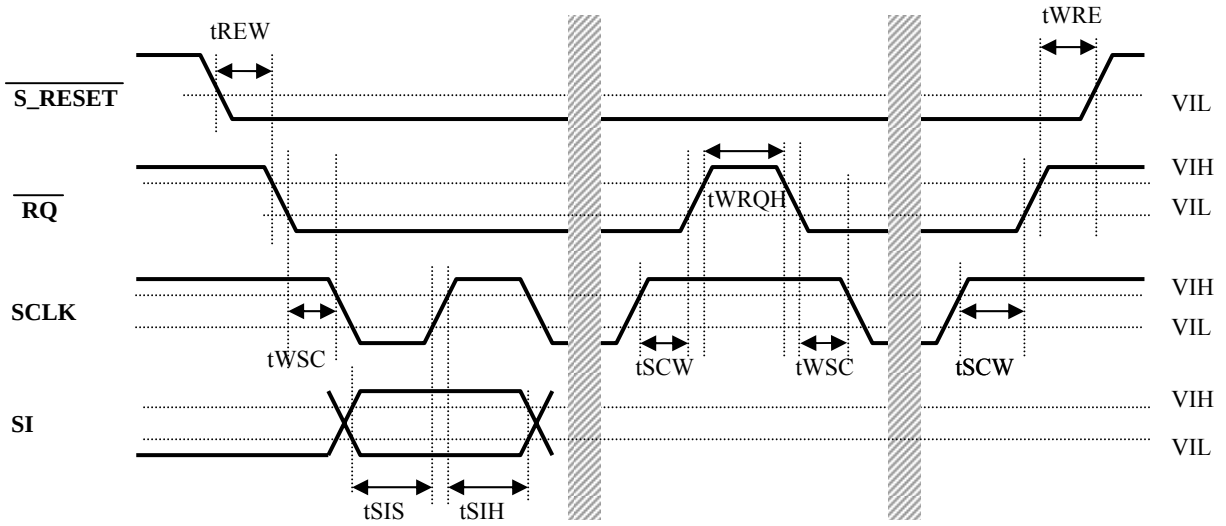
SDIN* : SDIN1~4

6-4) Microcomputer Interface

■ Microcomputer interface



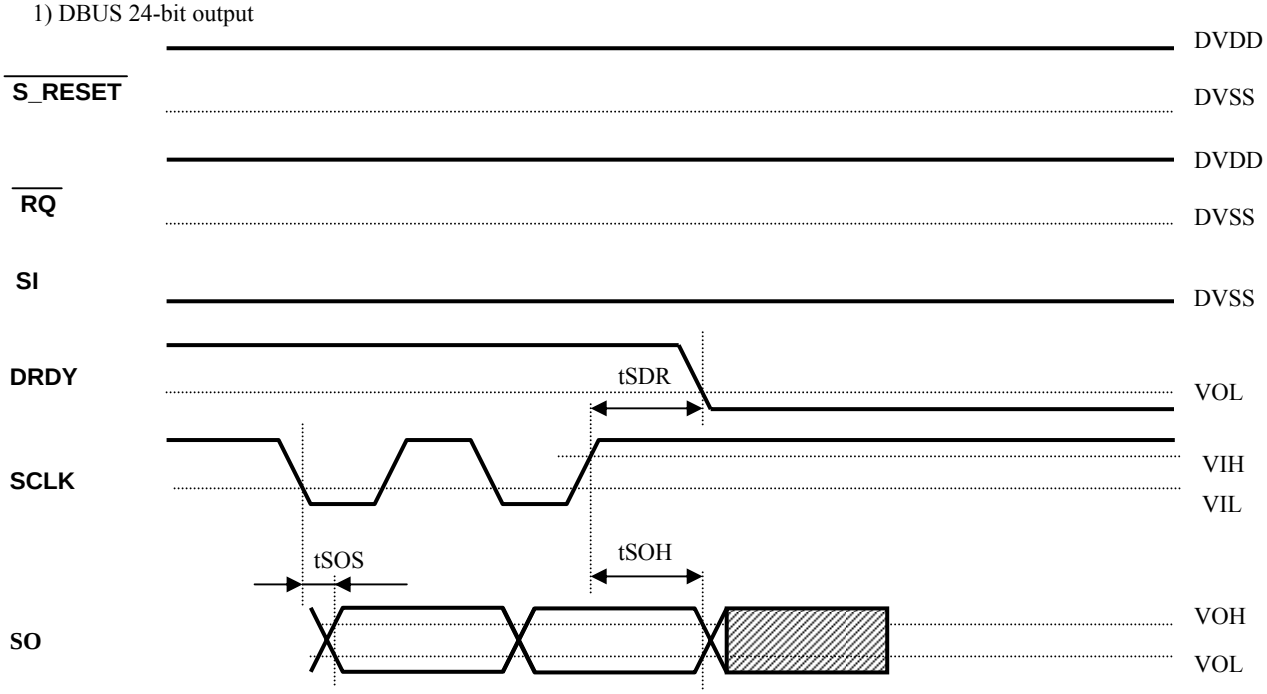
■ Microcomputer → AK7746



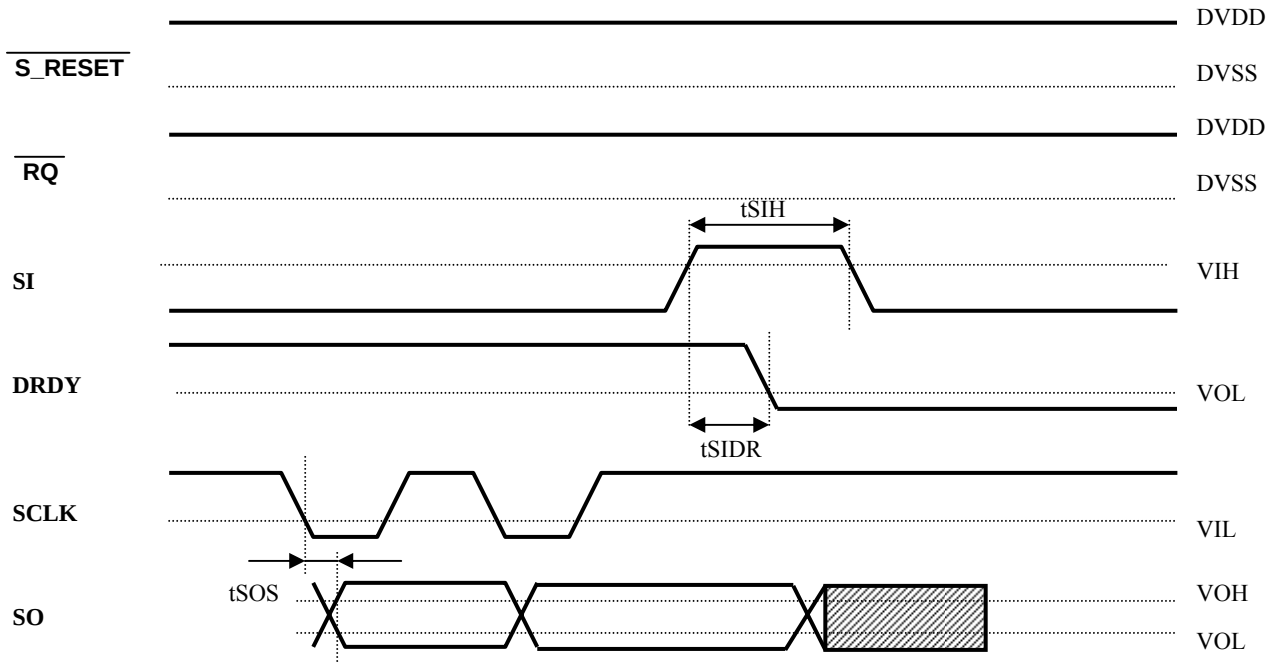
Note: The timing of the RUN state is the same except $\overline{\text{S\_RESET}}$ is "H".

■ AK7746 → Microcomputer (DBUS Output)

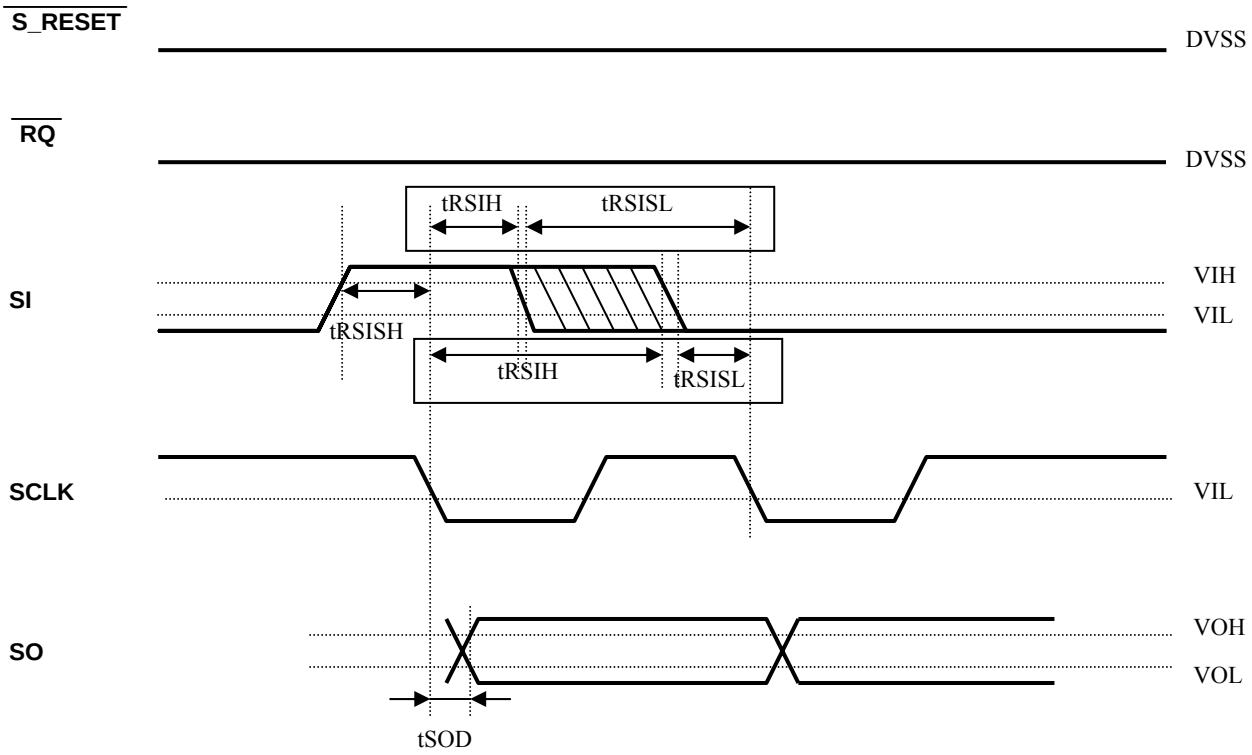
1) DBUS 24-bit output



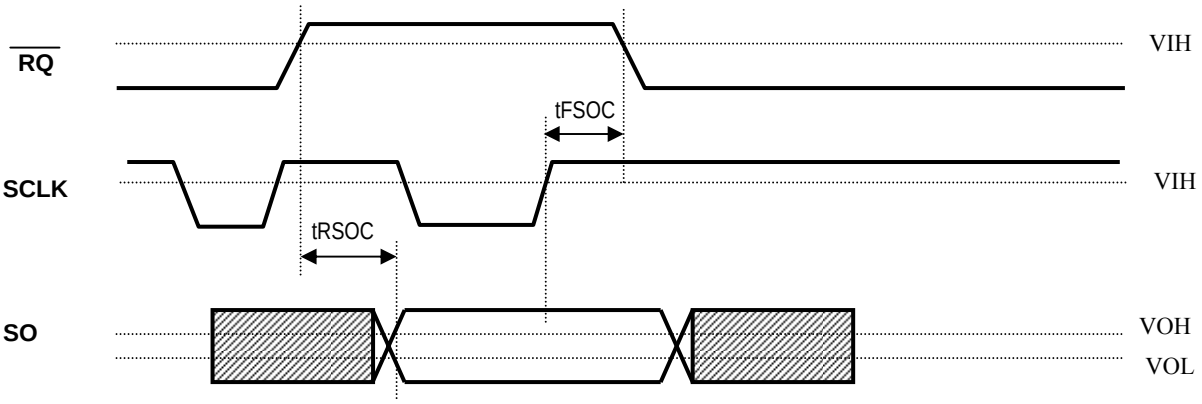
2) DBUS less than 24-bit (Using SI control)



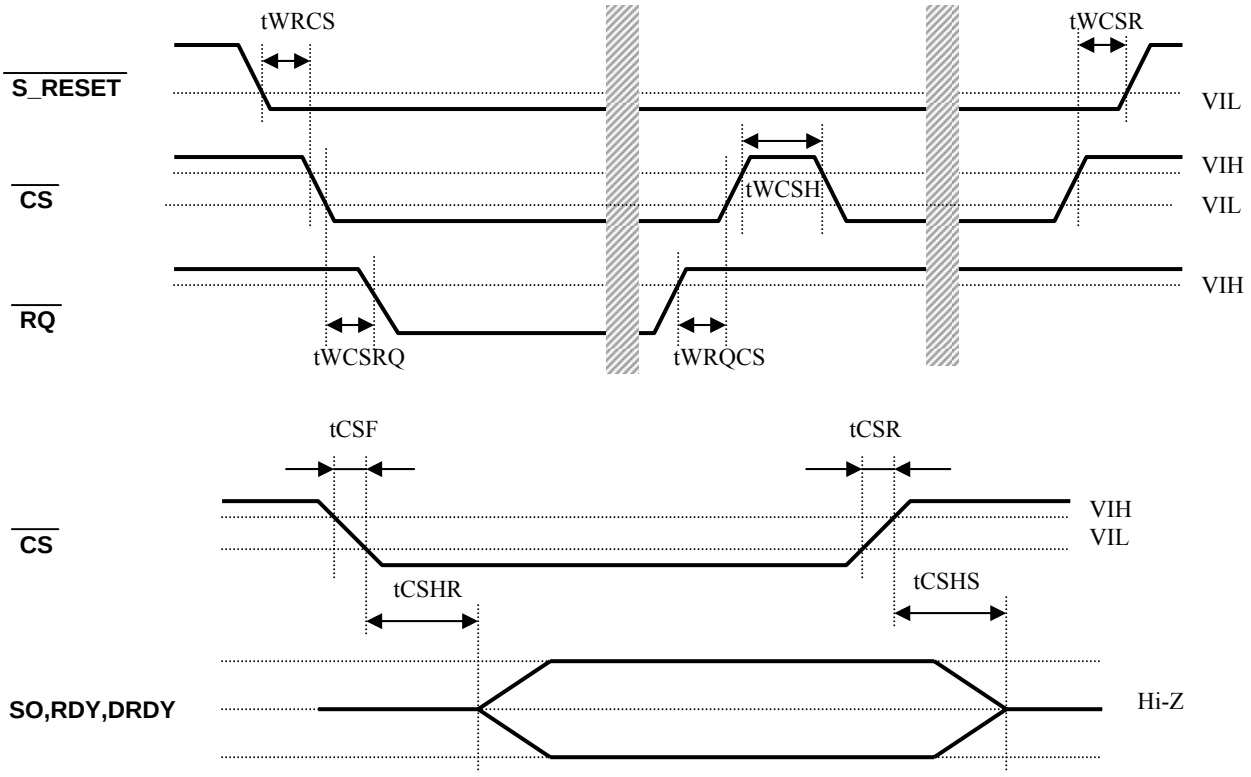
■ AK7746 → Microcomputer (Read out RAM DATA)

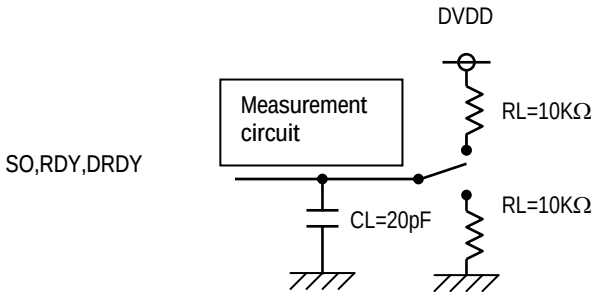


■ AK7746 → Microcomputer (CRC Check: {the surplus of D(x)/G(x)}=R(x))



■ $\overline{CS}$


tWRCS
tWCSR
S_RESET
VIL
CS
VIH
tWCSH
VIL
RQ
VIH
tWCSRQ
tWRQCS
tCSF
tCSR
CS
VIH
VIL
tCSHR
tCSHS
SO,RDY,DRDY
Hi-Z


DVDD
Measurement circuit
RL=10KΩ
SO,RDY,DRDY
CL=20pF
RL=10KΩ

8. Function Description

(1) Various Settings

1-1) SMODE: slave and master mode selector pin

This pin sets LRCLK and BITCLK to either inputs or outputs.

a) Slave mode: SMODE="L"
LRCLK_I (1fs) and BITCLK_I (64fs or 48fs) are inputs.
The LRCLK_O outputs the input signal to LRCLK_I.
The BITCLK_O outputs the input signal to BITCLK_I.
Note) BITCLK_I is able to input 48fs when CKS[1:0]≠2h.

b) Master mode: SMODE="H"
LRCLK_I and BITCLK_I is disabled.
LRCLK_O outputs 1fs, BITCLK_O outputs 64fs.

Note) SMODE pin can be chenged while the $\overline{\text{S\_RESET}}$ is "L". (When stopping XTI or changing the frequency, it must be set during the initial reset ($\overline{\text{INIT\_RESET}}$ ="L" and $\overline{\text{S\_RESET}}$ ="L").
When the input frequency is changed, it should be done during the initial reset ($\overline{\text{INIT\_RESET}}$ ="L" and $\overline{\text{S\_RESET}}$ ="L").

1-2) CKS1 pin,CKS0 pin: Master Clock (XTI or BITCLK_I) select pin

CLK Mode	CKS [1:0]	SMODE	Clock Input pin	Main Input frequency (MHz)	Available Frequency Range (MHz)	Crystal use	Internal PLL	Maximum number of DSP Steps (fs=48kHz)
0	0h	"L","H"	XTI	18.432, 16.9344	16.0~18.6	OK	Use	768
1	1h	"L","H"	XTI	12.288, 11.2896	11.0~12.4	OK	Use	768
2S	2h	"L"	BITCLK_I	3.072, 2.8224	2.75~3.1	NG	Use	768
2M	2h	"H"	XTI	3.072, 2.8224	2.75~3.1	NG	Use	768
3	3h	"L","H"	N/A	N/A	N/A	N/A	N/A	N/A

Note) CKS1=CKS[1], CKS0=CKS[0]

CLK Mode 2S is available only when fs =44.1kHz and 48kHz. CLK Mode 3 is not available (test use only).
The internal master clock (MCLK) of the AK7746 is 36.864MHz maximum.

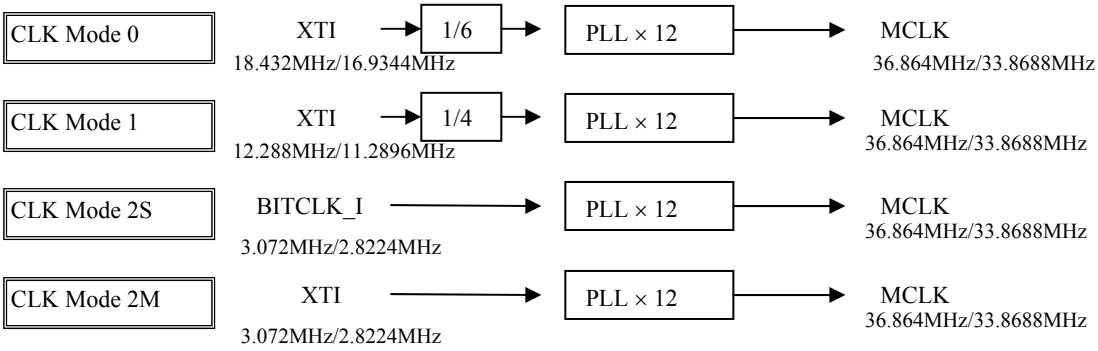


Fig.8-1 Relationship of XTI or BITCLK_I and MCLK (internal master clock)

CLK Mode 2S is used when BITCLK_I is used instead of XTI. Do NOT forget to set SMODE="L" , when using this mode. CLK Mode 2M can be used when SMODE= "H", however, it cannot be used with the crystal oscillator.
When CKS1 or CKS0 settings are changed after power up, (including changing between CLK mode 2S and CLK mode 2M), it must be done during the initial reset state ($\overline{\text{INIT\_RESET}}$ ="L" and $\overline{\text{S\_RESET}}$ ="L"). The CKS1 and the CKS0 pins control the PLL and the internal clock control circuits, therefore an erroneous operation may occur if any pin settings change during the run time of the AK7746. Changing the frequency of the XTI pin should be done at the initial reset state. The sampling rate is set by the control register. (The CLK mode 2S is valid only for 44.1kHz and 48kHz fs mode.)

1-3) Source of the master clock

a) XTI select

Clocks can be supplied to the AK7746's XTI pin as follows:

* When CLK mode 0 or 1 is used, either connect a proper crystal oscillator between XTI and XTO pins or supply a clock of proper frequency to the XTI pin.
* When CLK mode 2M is used, supply a clock of proper frequency to the XTI pin.

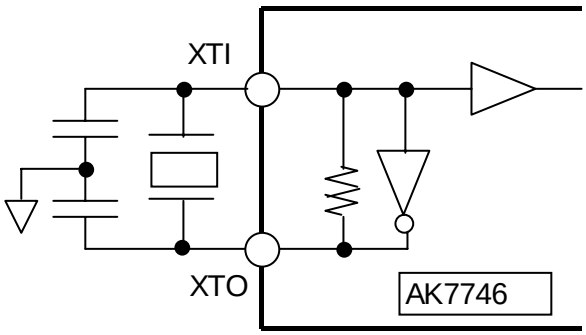


Fig.8-2 Using X'tal : CLK mode 0,1

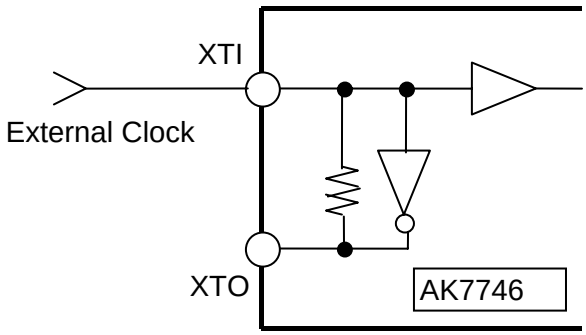


Fig.8-3 Using external clock : CLK mode 0,1,2M

b) BITCLK_I Select

The CLK mode 2S is used when the BITCLK_I is used instead of XTI. When selecting this mode, set SMODE="L". The clock supplied on the BITCLK_I pin is directly frequency- multiplied by the PLL and a master clock is generated. When the system is using this mode only, it is recommended to connect the XTI pin to DVSS.

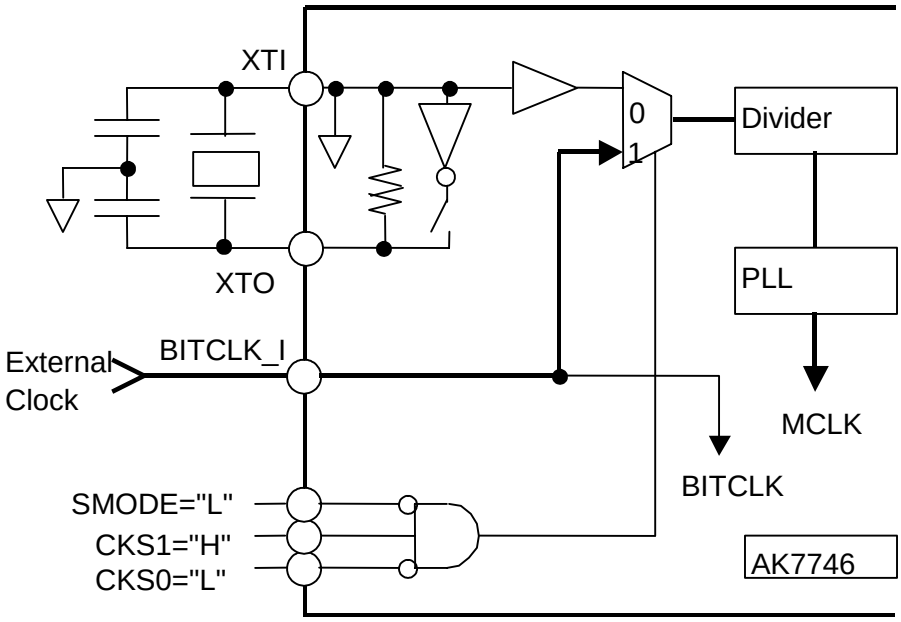


Fig.8-4 Image of the internal connection of the CLK mode 2S.

Input on BITCLK_I pin a divided-by-64 clock of the LRCLK_I (64fs). (BITCLK_I must be in synchronized with LRCLK_I.)

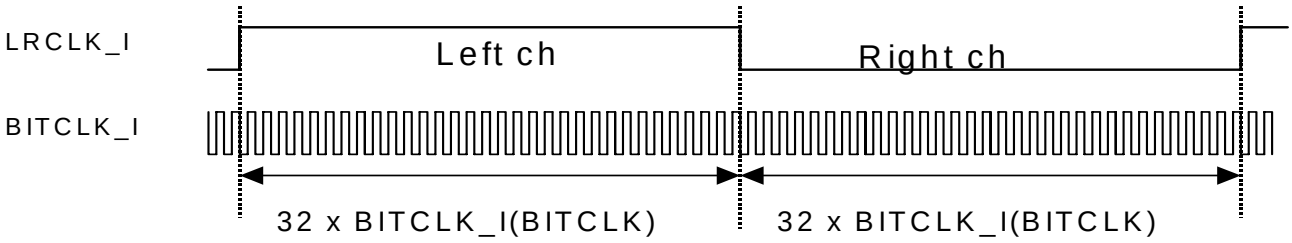


Fig.8-5 Relationship between BITCLK_I and LRCLK_I.

(2) Control registers

The control registers can be set via the microcomputer interface in addition to the control pins. These 8 registers consist of 7-bit data however; SCLK always needs to be a16-bit clock (Command Code 8-bits, Data 8-bits). Each register is set after the last D0 data is written. For the value to be written in the control registers see the description of the interface with microcomputer. The following table describes the control register map.

These control registers are initialized by $\overline{\text{INIT\_RESET}}$ ="L", but these are NOT initialized by $\overline{\text{S\_RESET}}$ ="L".

TEST: for TEST (input 0), (X: it ignores input data, but should input 0).

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
60h	70h	CONT0	DFS[2]	DFS[1]	DFS[0]	DIFS	DIF[1]	DIF[0]	SETCK	X	0000 000X
62h	72h	CONT1	DRAM	RM	BANK[1]	BANK[0]	CMP_N	SS[1]	SS[0]	X	0000 000X
64h	74h	CONT2	JX2_E	JX1_E	JX0_E	SSDIN4	SSDIN3	SWQMD	TEST	X	0000 000X
66h	76h	CONT3	ASEL2[2]	ASEL2[1]	ASEL2[0]	TEST	ASEL1[2]	ASEL1[1]	ASEL1[0]	X	0000 000X
68h	78h	CONT4	SWAD1_N	SWSDIN4_N	SWSDIN3_N	SWSDIN2_N	SWSDIN1	SWADM3_N	SWADM2_N	X	0000 000X
6Ah	7Ah	CONT5	OUT4E_N	OUT3E_N	OUT2E_N	OUT1E_N	CLKOE_N	TEST	TEST	X	0000 000X
6Ch	7Ch	CONT6	TEST	CLKS[1]	CLKS[0]	SWQ4	SWQ3	SWQ2	SWQ1	X	0000 000X
6Eh	7Eh	CONT7	SWQM2	SWQM1	OUTA2E_N	OUTA1E_N	PSADM	PSAD2	PSAD1	X	0000 000X

1. CONT0 can be set only at system reset ($\overline{\text{INIT\_RESET}}$ ="H" & $\overline{\text{S\_RESET}}$ ="L").
2. It is recommended to set CONT1~CONT2, CONT4~CONT7 at system reset.
3. When changing the selector switch of CONT3, a click noise may occur. The selector switchs are set during the writing timing of the CONT3 D0 (SCLK ↑).
4. The control registers can be read during run time.
5. The default setting is initialized by initial reset ($\overline{\text{INIT\_RESET}}$ ="L").

2-1) CONT0 : Sampling rate and interface selection.

This register is enabled only during the system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
60h	70h	CONT0	DFS[2]	DFS[1]	DFS[0]	DIFS	DIF[1]	DIF[0]	SETCK	×	0000 000X

① D7,D6,D5:DFS2,DFS1,DFS0 Sampling rate setting.

fs: sampling frequency

DFS Mode	DFS[2]	DFS[1]	DFS[0]	CKS[1:0] (Input frequency of XTI)			fs(kHz)	DSP Number of Steps	ADC
				0h	1h	2h			
0	0	0	0	384fs	256fs	64fs	48(44.1)	768	o
1	0	0	1	192fs	128fs	32fs	96(88.2)	384	o
2	0	1	0	N/A	N/A	N/A	N/A	N/A	N/A
3	0	1	1	576fs	384fs	96fs	32(29.4)	1152	o
4	1	0	0	1536fs	1024fs	256fs	12(11.025)	3072	o
5	1	0	1	768fs	512fs	128fs	24(22.05)	1536	o
6	1	1	0	1152fs	768fs	192fs	16(14.7)	2304	o
7	1	1	1	2304fs	1536fs	384fs	8	4608	o

Note) When CLK Mode 2S (CLKS[1:0]=2h & SMODE="L"), DFS Mode 0 should be set.

② D4:DIFS Audio interface selection

0: AKM method

1: I^2S compatible (In this case, all input / output pins are I^2S compatible.)

③ D3,D2:DIF[1],DIF[0] SDIN1,SDIN2,SDIN3,SDIN4 Input mode selector

Mode	DIF[1]	DIF[0]	
0	0	0	MSB justified (24bit)
1	0	1	LSB justified (24bit)
2	1	0	LSB justified (20bit)
3	1	1	LSB justified (16bit)

Note) When D4 = 1, the state is I^2S compatible, DIF[1:0] Mode 0 should be set.
This setting has no relation with ADC1, ADC2 and ADCM connection. When SWSDIN1=0, SWSDIN2_N=1, SWSDIN3_N=1 and SWSDIN4_N=1, then it will be MSB justified 24-bit compatible format independent of DIF1 and DIF0 setting.

④ D1: SETCK

Select output clock of the CLKO when the condition of CONT6 CLKS Mode 3.

CONT0	DFS[2:0]							
DFS Mode	0	1	2	3	4	5	6	7
SETCK=0	256fs	N/A	N/A	256fs	1024fs	N/A	512fs	1024fs
SETCK=1	64fs	64fs	32fs	64fs	256fs	256fs	128fs	256fs

⑤ D0: Always 0

When inputs D0, CONT0 setting is fixed.

Note) Underline of the settings with "_" mean default setting.

2-2) CONT1 : RAM control

Recommend changing this register during the system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
62h	72h	CONT1	DRAM	RM	BANK[1]	BANK[0]	CMP_N	SS[1]	SS[0]	×	0000 000X

① D7:DATARAM DATARAM addressing mode selector

0: Ring addressing mode

1: Linear addressing mode

DATARAM has 256-word x 24-bit and has 2 addressing pointer (DP0, DP1).

The Ring addressing mode: starting address increments by 1 every sample period.

The Linear addressing mode: starting address is always the same, DP0 = 00h and DP1 = 80h.

② D6:RM: Decompress bit mode

0: SIGN bit

1: Random data

When Compress & Decompress modes (D3:CMP_N = 0) are selected, this bit determines the decompressed LSB bits.

③ D5,D4:BANK[1:0] DLRAM Setting

Mode	BANK1:D5	BANK0:D4	Memory
0	0	0	24-bit 3kword(RAM A)
1	0	1	12-bit 6kword(RAM A)
2	1	0	12-bit 4kword(RAM A),24bit 1kword(RAM B)
3	1	1	24-bit 1kword(RAM A),12bit 4kword(RAM B)

Note) When mode 0 or 1 is selected, pointer 0 and 1 are available for both RAM area.
When mode 2 or 3 is selected, pointer 0 is available for RAM A and pointer 1 is available for RAM B.
When DLRAM is not used, mode 2 or 3 should be selected.

④ D3:CMP_N 12bitDLRAM Compress & Decompress selector

When mode 1, 2 or 3 is selected, this register can set the compress/decompress function.

0: Compress & Decompress function ON

When data is written to DLRAM the DBUS data is compressed to 12-bits. and when it data is read from DLRAM, it is decompressed to 24-bits.

1: Compress & Decompress function OFF

It always writes to DLRAM MSB 12-bit of DBUS data and it read from MSB 12-bit of DLRAM and add to 000h for LSB bits.

⑤ D2,D1:SS[1:0] DLRAM setting of sampling timing (only for RAM A)

Mode	SS[1]:D2	SS[0]:D1	RAM A mode selected by BANK[1:0]
0	0	0	Update every sampling time
1	0	1	Update every 2 sampling time
2	1	0	Update every 4 sampling time
3	1	1	Update every 8 sampling time

Note) When the mode 1,2 or 3 is selected, it comes out aliasing.

⑥ D0: Input always 0

When inputs D0, CONT1 setting is fixed.

Note) Underlines of the setting of "_" mean default setting.

3) CONT2 : Conditional jump, instruction setting. (See 3. Block diagram)

Recommend changing this register at the system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
64h	74h	CONT2	JX2_E	JX1_E	JX0_E	SSDIN4	SSDIN3	SWQMD	TEST	×	000 000X

① **D7 : JX2_E** (See. 3. Block diagram)
0: Normal operation (SDIN4)
1: JX2 is enable. (SDIN4 can not be read)

② **D6 : JX1_E** (See. 3. Block diagram)
0: Normal operation (SDIN3)
1: JX1 is enable. (SDIN3 can not be read)

③ **D5 : JX0_E** (See. 3. Block diagram)
0: Normal operation (SDIN1)
1: JX0 is enable. (SDIN1 can not be read)

④ **D4 : SSDIN4 DSP instruction select.**
0: ODRB and MSRG are enabled (@SWSDIN4_N=0) / INL4 and MSRG are enabled (@SWSDIN4_N=1)
1: INL4 and INR4 (Digital input of SDIN4) are enabled.

SSDIN4	SWSDIN4_N (CONT4 D6)	SRC field	SRC field
0	0	ODRB	MSRG
0	1	INL4	MSRG
1	×	INL4	INR4

⑤ **D3 : SSDIN3 DSP insturuction select**
0: TDR2 and TDR3 (DR2 and DR3 through output) are enabled
1: INL3 and INR3 (Digital input of SDIN3) are enabled.
When SRC data loads to DBUS, TDR2 and TDR3 data is changed to INL3 and INR3 data.

⑥ **D2 : SWQMD** (See 3. Block diagram)
0: Normal operation
1: The digital output of ADCM connects to SDOUT4.

⑦ **D1 : TEST**
0: Normal operation
1: TEST MODE (Do NOT use this.)

⑧ **D0 : Always input 0**

Note) Underlines of the ①~⑦ mean default setting.

4) CONT3 : ADC2, ADC1 input selector setting

When changing this setting during RUN steate, it may come out click noise.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
66h	76h	CONT3	ASEL2[2]	ASEL2[1]	ASEL2[0]	TEST	ASEL1[2]	ASEL1[1]	ASEL1[0]	×	0000 000X

① D7,D6,D5 : ASEL2[2:0] ADC2 Input selector setting

ASEL2[2]	ASEL2[1]	ASEL2[0]	Selected analog input pins
0	0	0	AINL-,AINL+,AINR-,AINR+
0	0	1	AINL2,AINR2
0	1	0	AINL3,AINR3
0	1	1	AINL4,AINR4
1	0	0	AINL5,AINR5
1	0	1	AINL6,AINR6
1	1	0	AINL7,AINR7
1	1	1	AINL8,AINR8

② D4 : TEST

0: Normal operation

1: TEST MODE (Do NOT use this.)

③ D3,D2,D1 : ASEL1[2:0] ADC1 input

ASEL1[2]	ASEL1[1]	ASEL1[0]	Selected analog input pins
0	0	0	AINL-,AINL+,AINR-,AINR+
0	0	1	AINL2,AINR2
0	1	0	AINL3,AINR3
0	1	1	AINL4,AINR4
1	0	0	AINL5,AINR5
1	0	1	AINL6,AINR6
1	1	0	AINL7,AINR7
1	1	1	AINL8,AINR8

④ D0 : Always input 0

Note) Underlines of the ①~③ mean default setting.

5) CONT4 : Internal path setting (see. 3. Block diagram)

Recommend this register changing at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
68h	78h	CONT4	SWAD1_N	SWSDIN4_N	SWSDIN3_N	SWSDIN2_N	SWSDIN1	SWADM3_N	SWADM2_N	×	0000 000X

① **D7 : SWAD1_N DSP SDIN5 input select**
0: DSP SDIN5 connects with ADC1 serial out
1: DSP SDIN5 connects with ADCM serial out

② **D6 : SWSDIN4_N DSP SDIN4 input select**
0: DSP SDIN4 connects with SDIN4 –pin
1: DSP SDIN4 connects with ADCM serial out.

③ **D5 : SWSDIN3_N DSP SDIN3 input select**
0: DSP SDIN3 connects with SDIN3 pin.
1: DSP SDIN3 connects with D2: SWADM3_N.
SWADM3_N=0 ADCM selected
SWADM3_N=1 ADC2 selected

④ **D4 : SWSDIN2_N DSP SDIN2 input select**
0: DSP SDIN2 connects with SDIN2 pin
1: DSP SDIN2 connects with D1: SWADM2_N.
SWADM2_N=0 ADCM selected
SWADM2_N=1 ADC2 selected

⑤ **D3 : SWSDIN1 DSP SDIN1 input select**
0: DSP SDIN1 connects with ADC2 serial output.
1: DSP SDIN1 connects with SDIN1 pin

⑥ **D2 : SWADM3_N ADCM,ADC2 select**
0: ADCM Selected
1: ADC2 Selected

⑦ **D1 : SWADM2_N ADCM,ADC2 select**
0: ADCM Selected
1: ADC2 Seleted

⑧ **D0 : Always input 0**

Note) Underlines of the ①~⑦ mean default setting.

6) CONT5 : Output control (See. 3 Block diagram)

Recommend this register changing at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
6Ah	7Ah	CONT5	OUT4E_N	OUT3E_N	OUT2E_N	OUT1E_N	CLKOE_N	TEST	TEST	×	0000 000X

① **D7: OUT4E_N DSP SDOUT4 Output select**
0: Normal operation
1: When SWQMD=0 & SWQ4=0, then SDOUT4 = "L".

② **D6 : OUT3E_N DSP SDOUT3 Output select**
0: Normal operation
1: When SWQ3=0 then SDOUT3 ="L".

③ **D5 : OUT2E_N DSP SDOUT2 Output select**
0: Normal operation
1: When SWQ2=0, then SDOUT2="L".

④ **D4 : OUT1E_N DSP SDOUT1 Output select**
0: Normal operation
1: When SWQ1=0 then SDOUT1="L".

⑤ **D3 : CLKOE_N CLKO Output select**
0: Normal operation
1: CLKO="L"
If CLKOE_N=1 is changed to CLKOE_N=0, CLKO should output the clock.

⑥ **D2 : TEST**
0: Normal operation
1: TEST mode (Do NOT use this mode.)

⑦ **D1 : TEST**
0: Normal operation
1: TEST mode (Do NOT use this mode.)

⑧ **D0: Always input 0**

Note) Underlines of the ①~⑦ mean default setting.

7) CONT6 : CLKO setting & Internal path setting (See. 3 Block diagram)

Recommend this register changing at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
6Ch	7Ch	CONT6	TEST	CLKS[1]	CLKS[0]	SWQ4	SWQ3	SWQ2	SWQ1	×	0000 000X

① **D7 : TEST**

0: Normal operation

1: TEST Mode (Do NOT use.)

② **D6,D5 : CLKS[1],CLKS[0] CLKO Output select**

CLKS Mode	CLKS[1]	CLKS[0]	CLKO	MCLK @36.864MHz	MCLK @33.8688MHz
0	0	0	MCLK/2	18.432MHz	16.9344MHz
1	0	1	MCLK/3	12.288MHz	11.2896MHz
2	1	0	MCLK × 2/9	8.192MHz	7.5264MHz
3	1	1	SETCK	CONT0(D1)	CONT0(D1)

Note1) MCLK is the internal master clock. MCLK is changed by inputting XTI frequency. Normally, MCLK is 36.864MHz or 33.8688MHz. See (5) 1) Master clock select table.

Note 2) CLKS Mode 3 output data is determined by CONT0 SETCK(D1).

Note 3) It takes 12ms(max) until the clock comes out following $\overline{\text{INIT\_RESET}}$ release.

Note 4) When this control register changes, noise may occur on CLKO. Once CLKO comes out, it can not stop unless CLKE_N is set to 1 or a reset is initialized (while the clock is supplied)

③ **D4 : SWQ4 SDOUT4 Output select**

0: Normal operation

1: Through outputs of SDIN4.
Note that it includes output delay.

④ **D3 : SWQ3 SDOUT3 Output select**

0: Normal operation

1: Through outputs of SDIN3.
Note that it includes output delay.

⑤ **D2 : SWQ2 SDOUT2 Output select**

0: Normal operation

1: Through outputs of SDIN2.
Note that it includes output delay.

⑥ **D1 : SWQ1 SDOUT1 Output select**

0: Normal operation

1: Through outputs of SDIN1.
Note that it includes output delay.

⑦ **D0 : Always input 0**

Note) Underlines of the ①~⑥ mean default setting.

8) CONT7 : ADC setting (See. 3 Block diagram)

Recommend this register changing at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
6Eh	7Eh	CONT7	SWQM2	SWQM1	OUTA2E_N	OUTA1E_N	PSADM	PSAD2	PSAD1	×	0000 000X

① **D7 : SWQM2 SDOUTA2 Output select**
0: Select ADC2 output
1: Select ADCM output

② **D6 : SWQM1 SDOUTA1 Output select**
0: Select ADC1 output.
1: Select ADCM output

③ **D5 : OUTA2E_N SDOUTA2 Output select**
0: Normal operation
1: SDOUTA2="L"

④ **D4 : OUTA1E_N SDOUTA1 Output select**
0: Normal operation
1: SDOUTA1="L"

⑤ **D3 : PSADM**
0: Normal operation
1: ADCM power save mode.
When ADCM is not used, it can be powered down
(The digital output data of the ADCM is 000000h)
When it resumes normal operation, it should write 0.

⑥ **D2 : PSAD2**
0: Normal operation
1: ADC2 power save mode
When ADC2 is not used, it can be powered down
(The digital output data of the ADC2 is 000000h)
When it resumes normal operation, it should write 0.

⑦ **D1 : PSAD1**
0: Normal operation
1: ADC1 power save mode
When ADC1 is not used, it can be powered down
(The digital output data of the ADC1 is 000000h)
When it resumes normal operation, it should write 0.

⑧ **D0 : Always input 0.**

Note) Underlines of the ①~⑦ mean default setting.

(3) Power supply startup sequence

At the rise of AVDD and DVDD, $\overline{\text{INIT\_RESET}}$ and $\overline{\text{S\_RESET}}$ should be set to "L".

$\overline{\text{INIT\_RESET}}$ = "L" initializes all control registers. Note 1), Note 2). VREF (Analog reference level) of the AK7746 is set up and begins to generate the internal master clock by setting to $\overline{\text{INIT\_RESET}}$ = "H". The interface of the AK7746 cannot accept data before the PLL locks; it must wait at least 15ms from $\overline{\text{INIT\_RESET}}$ = "H". Note 3)

Normally, $\overline{\text{INIT\_RESET}}$ setting is only done at power-on.

Note 1): To confirm initialization power up and master clock (XTI) supplied.

Note 2): Set to $\overline{\text{INIT\_RESET}}$ = "H" after setting the oscillation when a crystal oscillator is used.
This setting time may differ depending on the crystal oscillator and its external circuit.

Note 3): In case of CKS[1:0] = 0h then waiting time is 15ms. CKS[1:0] = 1h or 2h then waiting time is 22ms.

NOTE: Do not stop the system clock (slave mode: XTI, LRCLK_I, BITCLK_I (CLK2S mode : LRCLK_I, BITCLK_I), master mode: XTI) except when $\overline{\text{S\_RESET}}$ = "L". If these clock signals are not supplied, excess current will flow due to dynamic logic that is used internally, and an operation failure may result.

Don't set $\overline{\text{S\_RESET}}$ ="H" during $\overline{\text{INIT\_RESET}}$ ="L", unless its crystal oscillator will stop or be in unstable.

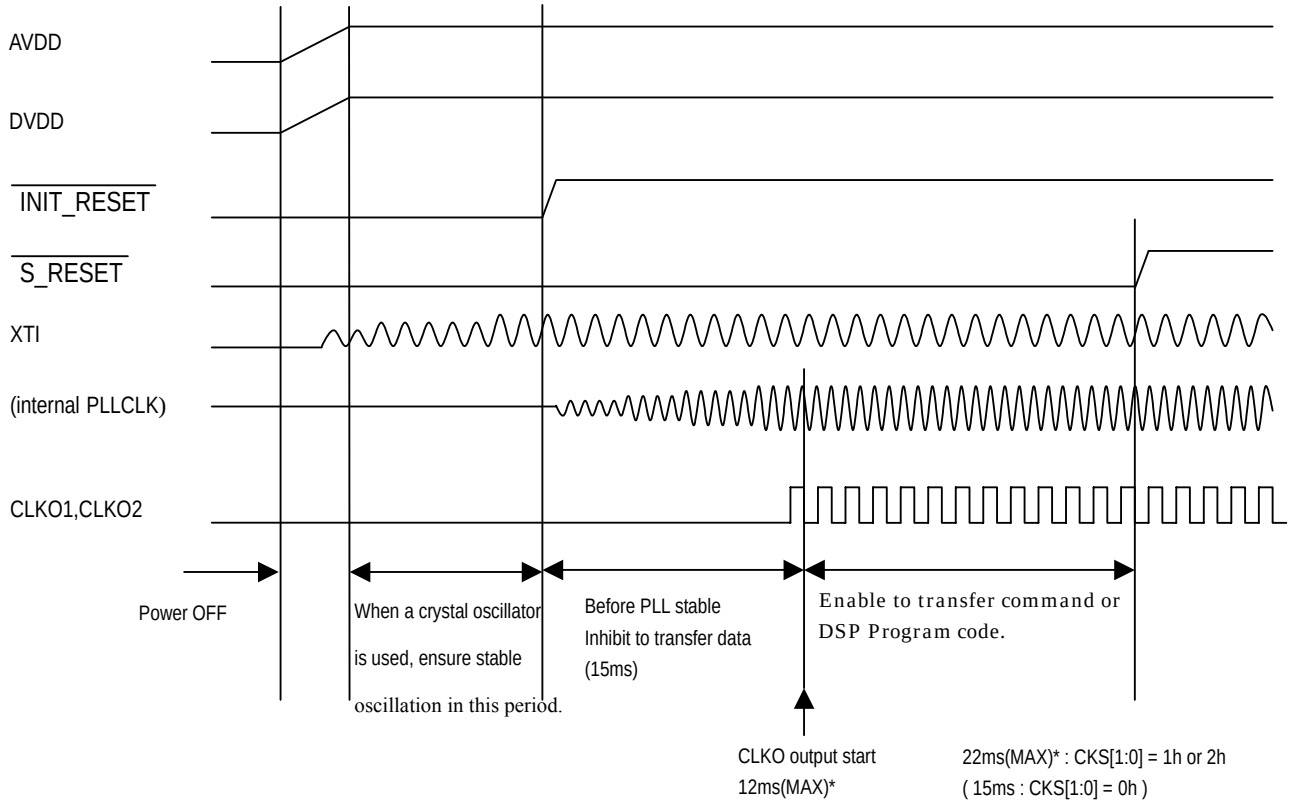


Fig.8-6 Power supply startup sequence

(4) Resetting

The AK7746 has two reset pins: $\overline{\text{INIT\_RESET}}$ and $\overline{\text{S\_RESET}}$.

The $\overline{\text{INIT\_RESET}}$ pin is used to set up VREF and initialize the AK7746, as shown in "Power supply startup sequence section (3)."

The system is reset when $\overline{\text{S\_RESET}}$ ="L". (Description of "reset" is for "system reset".)

During a system reset, a program write operation is normally performed (except for write operation during running).

During the system reset phase, the ADC sections are also reset. (The digital section of ADC output is MSB first 00000h). However, VREF will be active; LRCLK and BITCLK in the master mode will be inactive**.**

The system reset is released by setting $\overline{\text{S\_RESET}}$ to "H", which activates the internal counter.

This counter generates LRCLK and BITCLK in the master mode: however, a problem may occur when a clock signal is generated.

When the system reset is released in slave mode, internal timing will be actuated in synchronization with rising edge "↑" of LRCLK (when the standard input format is used). Timing between the external and internal clocks is adjusted at this time. Therefore make sure to avoid phase difference between LRCLK and internal timing. If the phase difference in LRCLK and internal timing is within about -1/16 to 1/16 of the input sampling cycle (1/fs) during the operation, the operation is performed with internal timing remaining unchanged. If the phase difference exceeds the above range, the phase is adjusted by synchronizing the "↑" of LRCLK (when the standard input format is used). This prevents synchronization failure with the external circuit.

The ADC section can output 516-LRCLK after its internal counter has started. (The internal counter starts at the first rising edge of LRCLK in master mode. In slave mode, it starts 6 LRCLKs(max) after the release of system reset.)

The AK7746 performs normal operation when $\overline{\text{S\_RESET}}$ is set to "H".

♦ RAM Clear

The AK7746 will write automatically all 0 data into all DRAM and DLRAM after release the system reset. (RAM Clear).

It takes 5*LRCLK(max)+2048*MCLK(internal master clock) at slave mode, and it takes 2*LRCLK(max)+2048*MCLK at master mode.

Therefore in the slave mode, it will take about 160μs [(5/48kHz)+(2048/36.864MHz)] at fs=48kHz, or 174μs [(5/44.1kHz)+(2048/33.8688MHz)] at fs=44.1kHz.

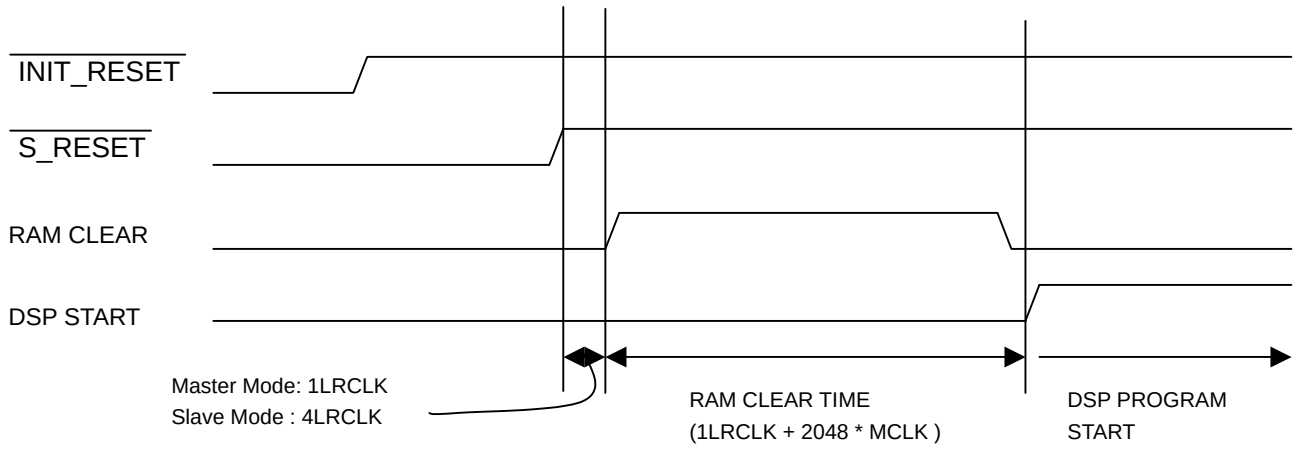


Fig.8-7 RAM CLEAR SEQUENCE

(5) System clock

1) master clock select table.

(A) Sampling frequency 48kHz series (Normal :48kHz, Double:96kHz)

XTI [MHz]	SMODE	INPUT PIN CKS1	INPUT PIN CKS0	CONT0 DFS2	CONT0 DFS1	CONT0 DFS0	FS [KHz]	DSP STEP	MCLK [MHz]	PLL active	AD active	X'tal active
18.432	0 or 1	0	0	0	0	0	48	768	36.864	o	o	o
↑	↑	↑	↑	0	0	1	96	384	↑	o	o	o
↑	↑	↑	↑	0	1	0	N/A	N/A	↑	-	-	-
↑	↑	↑	↑	0	1	1	32	1152	↑	o	o	o
↑	↑	↑	↑	1	0	0	12	3072	↑	o	o	o
↑	↑	↑	↑	1	0	1	24	1536	↑	o	o	o
↑	↑	↑	↑	1	1	0	16	2304	↑	o	o	o
↑	↑	↑	↑	1	1	1	8	4608	↑	o	o	o
12.288	0 or 1	0	1	0	0	0	48	768	36.864	o	o	o
↑	↑	↑	↑	0	0	1	96	384	↑	o	o	o
↑	↑	↑	↑	0	1	0	N/A	N/A	↑	-	-	-
↑	↑	↑	↑	0	1	1	32	1152	↑	o	o	o
↑	↑	↑	↑	1	0	0	12	3072	↑	o	o	o
↑	↑	↑	↑	1	0	1	24	1536	↑	o	o	o
↑	↑	↑	↑	1	1	0	16	2304	↑	o	o	o
↑	↑	↑	↑	1	1	1	8	4608	↑	o	o	o
3.072	1	1	0	0	0	0	48	768	36.864	o	o	×
↑	↑	↑	↑	0	0	1	96	384	↑	o	o	×
↑	↑	↑	↑	0	1	0	N/A	N/A	↑	-	-	-
↑	↑	↑	↑	0	1	1	32	1152	↑	o	o	×
↑	↑	↑	↑	1	0	0	12	3072	↑	o	o	×
↑	↑	↑	↑	1	0	1	24	1536	↑	o	o	×
↑	↑	↑	↑	1	1	0	16	2304	↑	o	o	×
↑	↑	↑	↑	1	1	1	8	4608	↑	o	o	×

BITCLK_I [MHz]	SMODE	INPUT PIN CKS1	INPUT PIN CKS0	CONT0 DFS2	CONT0 DFS1	CONT0 DFS0	FS [KHz]	DSP STEP	MCLK [MHz]	PLL active	AD active	X'tal active
3.072	0	1	0	0	0	0	48	768	36.864	o	o	×
↑	↑	↑	↑	0	0	1	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	0	1	0	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	0	1	1	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	1	0	0	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	1	0	1	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	1	1	0	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	1	1	1	↑	↑	↑	↑	↑	↑

(B) Sampling frequency 44.1kHz series (Normal: 44.1kHz, Double: 88.2kHz)

XTI [MHz]	SMODE	INPUT PIN CKS1	INPUT PIN CKS0	CONT0 DFS2	CONT0 DFS1	CONT0 DFS0	FS [KHz]	DSP STEP	MCLK [MHz]	PLL Active	AD Active	X'tal Active
16.9344	0 or 1	0	0	0	0	0	44.1	768	33.8688	o	o	o
↑	↑	↑	↑	0	0	1	88.2	384	↑	o	o	o
↑	↑	↑	↑	0	1	0	N/A	N/A	↑	-	-	-
↑	↑	↑	↑	0	1	1	29.4	1152	↑	o	o	o
↑	↑	↑	↑	1	0	0	11.025	3072	↑	o	o	o
↑	↑	↑	↑	1	0	1	22.05	1536	↑	o	o	o
↑	↑	↑	↑	1	1	0	14.7	2304	↑	o	o	o
↑	↑	↑	↑	1	1	1	-	-	-	-	-	-
11.2896	0 or 1	0	1	0	0	0	44.1	768	33.8688	o	o	o
↑	↑	↑	↑	0	0	1	88.2	384	↑	o	o	o
↑	↑	↑	↑	0	1	0	N/A	N/A	↑	-	-	-
↑	↑	↑	↑	0	1	1	29.4	1152	↑	o	o	o
↑	↑	↑	↑	1	0	0	11.025	3072	↑	o	o	o
↑	↑	↑	↑	1	0	1	22.05	1536	↑	o	o	o
↑	↑	↑	↑	1	1	0	14.7	2304	↑	o	o	o
↑	↑	↑	↑	1	1	1	-	-	-	-	-	-
2.8224	1	1	0	0	0	0	44.1	768	33.8688	o	o	×
↑	↑	↑	↑	0	0	1	88.2	384	↑	o	o	×
↑	↑	↑	↑	0	1	0	N/A	N/A	↑	-	-	-
↑	↑	↑	↑	0	1	1	29.4	1152	↑	o	o	×
↑	↑	↑	↑	1	0	0	11.025	3072	↑	o	o	×
↑	↑	↑	↑	1	0	1	22.05	1536	↑	o	o	×
↑	↑	↑	↑	1	1	0	14.7	2304	↑	o	o	×
↑	↑	↑	↑	1	1	1	-	-	-	-	-	-

BITCLK_I {MHz}	SMODE	INPUT PIN CKS1	INPUT PIN CKS0	CONT0 DFS2	CONT0 DFS1	CONT0 DFS0	FS [KHz]	DSP STEP	MCLK [MHz]	PLL Active	AD Active	X'tal Active
2.8224	0	1	0	0	0	0	44.1	768	33.8688	o	o	×
↑	↑	↑	↑	0	0	1	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	0	1	0	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	0	1	1	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	1	0	0	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	1	0	1	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	1	1	0	↑	↑	↑	↑	↑	↑
↑	↑	↑	↑	1	1	1	↑	↑	↑	↑	↑	↑

(C) CLKO Output select information. (fs=48kHz)

XTI or BITCLK_I [MHz]	INPUT PIN CKS[1]	INPUT PIN CKS[0]	CONT0 SETCK	CONT6 CLKS1	CONT6 CLKS0	OUTPUT CLKO [MHz]
18.432	0	0	0	0	0	18.432
↑	↑	↑	0	0	1	12.288
↑	↑	↑	0	1	0	8.192
↑	↑	↑	0	1	1	256fs
↑	↑	↑	1	X	X	64fs
12.288	0	1	0	0	0	18.432
↑	↑	↑	0	0	1	12.288
↑	↑	↑	0	1	0	8.192
↑	↑	↑	0	1	1	256fs
↑	↑	↑	1	X	X	64fs
3.072	1	0	0	0	0	18.432
↑	↑	↑	0	0	1	12.288
↑	↑	↑	0	1	0	8.192
↑	↑	↑	0	1	1	256fs
↑	↑	↑	1	X	X	64fs
36.864	1	1	0	0	0	18.432
↑	↑	↑	0	0	1	12.288
↑	↑	↑	0	1	0	8.192
↑	↑	↑	0	1	1	256fs
↑	↑	↑	1	X	X	64fs

(D) CLKO Output information

$\overline{\text{INIT\_RESET}}$	$\overline{\text{S\_RESET}}$	CLKO	
		CLKOE_N=0	CLKOE_N=1
L	L	Stop	
H	L	Active	Stop
H	H	Active	Stop

(E) Output timing image

The following figure indicates the timing when changing of CLKO.
(The phase of the clock is not always same as following figure.)

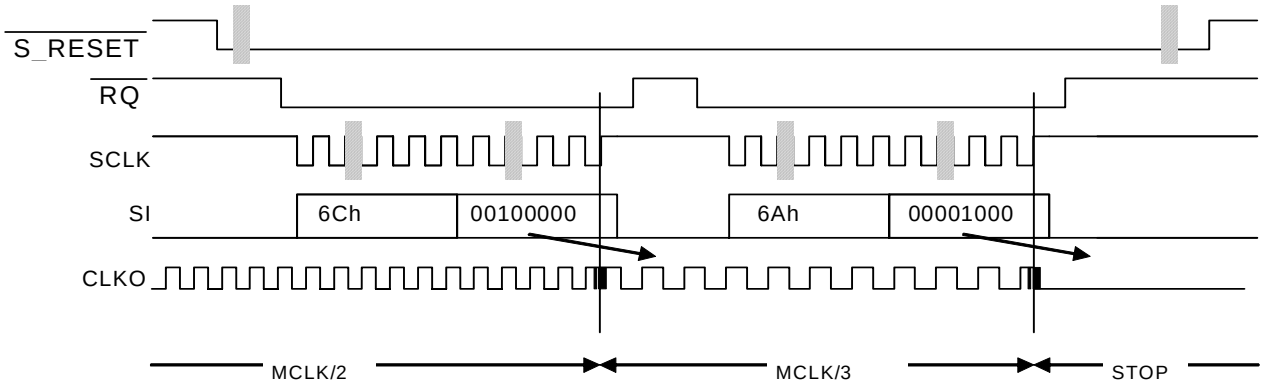


Fig.8-8 Example of changing control register CONT6 setting 00h(Default) into new value.

2) Master Clock (XTI pin or BITCLK_I pin)

The master clock can get from the crystal oscillator connected between the XTI and the XTO pins, or from the external clock to the XTI pin and XTO pin is open. Only the CLK mode 2S (CKS[1:0]=2h and SMODE="L") can use the clock input to the BITCLK_I pin instead of the XTI pin. At that time the XTI pin should be connected to DVSS.

3) Slave Mode

When the mode is CKS[1:0]≠2h, the requied system clocks are XTI , LRCLK_I(1fs) and BITCLK_I (64fs or 48fs). At that time, the master clock (XTI) must be synchronized with LRCLK_I, but it does not need to be in phase.
When the mode is CKS[1:0]=2h, the requied system clocks are LRCLK_I(1fs) and BITCLK_I (64fs only, 48fs can not be use). In this mode the master clock (BITCLK_I) must be in synchronized with LRCLK_I and also need to be in phase.
LRCLK_I, BITCLK_I are directly output on LRCLK_O and BITCLK_O respectively.

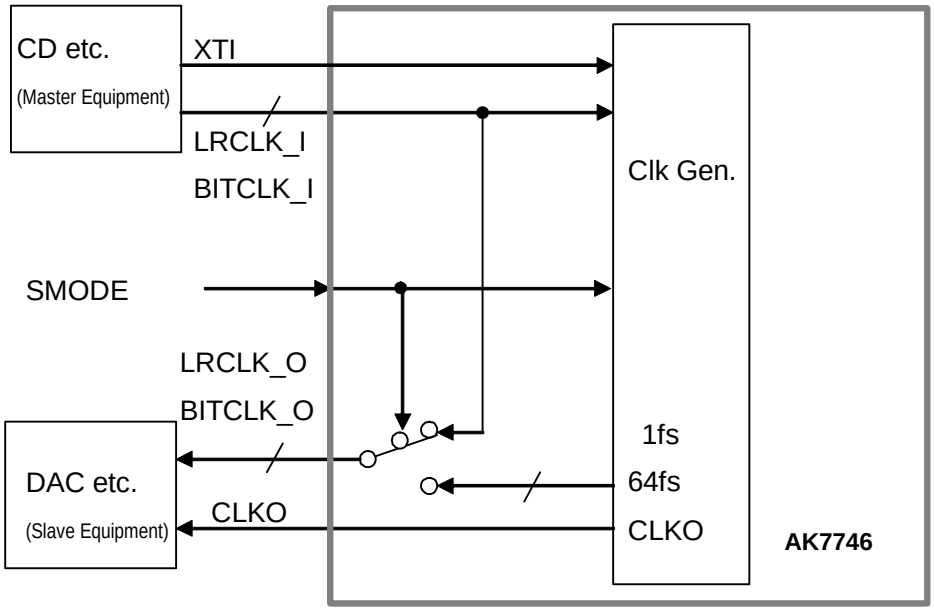


Fig. 8-9 Slave mode example

4) Master Mode

Master mode requires a clock input to XTI pin. When a clock is applied to the XTI input, LRCLK_O and BITCLK_O are automatically generated by an XTI-synchronized internal counter. No output is available on LRCLK_O and BITCLK_O pins during an initial reset ($\overline{\text{INIT\_RESET}}$ ="L") and a system reset ($\overline{\text{INIT\_RESET}}$ ="H" and $\overline{\text{S\_RESET}}$ ="L").

When using only for the master mode on the AK7746, the LRCLK_I and the BITCLK_I should set "L".

(6) Audio data interface (internal connection mode)

The serial audio data pins SDIN1,SDIN2,SDIN3,SDIN4,SDOUT1,SDOUT2,SDOUT3, SDOUT4, SDOUTA1 and SDOUTA2 are interfaced with the external system, using LRCLK_I, LRCLK_O, BITCLK_I and BITCLK_O. These ports are controlled via registers. (See the block diagram on page.2 and the control register setting section at page 28.)

The data format is MSB-first 2's complement. Normally, the input/output format, in addition to the standard format used by AKM, can be changed to I^2S compatible mode by setting the control register "CONT0 DIF (D4) to 1". (In this case, all input/output audio data pin interface are in the I^2S compatible mode.)

The input SDIN1, SDIN2, SDIN3 and SDIN4 formats are MSB justified 24-bit at initialization. Setting the control registers CONT0: DIF1 (D3), DIF0 (D2) will cause these ports to be compatible with LSB justified 24-bit, 20-bit and 16-bit.

However, individual setting of SDIN1, SDIN2, SDIN3 and SDIN4 is not allowed. The output SDOUT1, SDOUT2, SDOUT3 and SDOUT4 are fixed at 24-bit MSB justified only. The ADCM is monoral but outputs same data for Lch and Rch.

In slave mode BITCLK_I corresponds to not only 64fs but also 48fs. 64fs is the recommended mode. Following formats describe 64fs examples.

1) Standard input format (DIFS = 0: default set value)

a) Mode 1 (DIF[1:0] = 0 default set value)

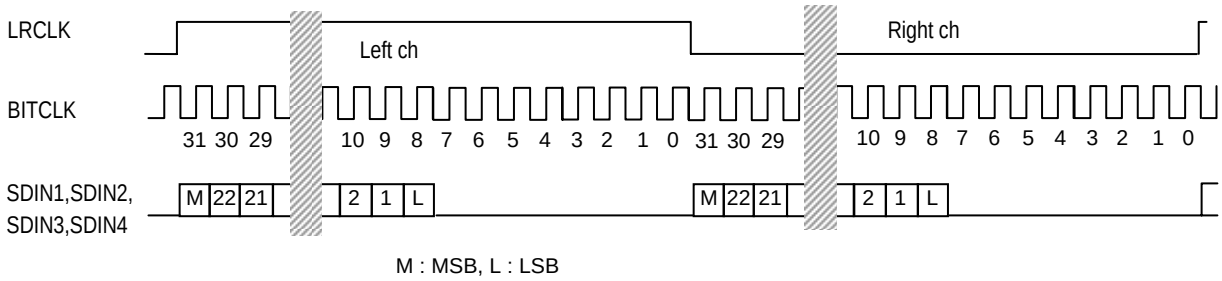


Fig.8-10

* When you want to input the MSB-justified 20-bit data into SDIN, SDINA input four "0" following the LSB.

b) Mode 2, Mode 3, Mode 4

SDIN1,SDIN2,SDIN3,SDIN4	Mode2 : DIF[1:0]=1	LSB justified 24-bit
SDIN1,SDIN2,SDIN3,SDIN4	Mode3 : DIF[1:0]=2	LSB justified 20-bit
SDIN1,SDIN2,SDIN3,SDIN4	Mode4 : DIF[1:0]=3	LSB justified 16-bit

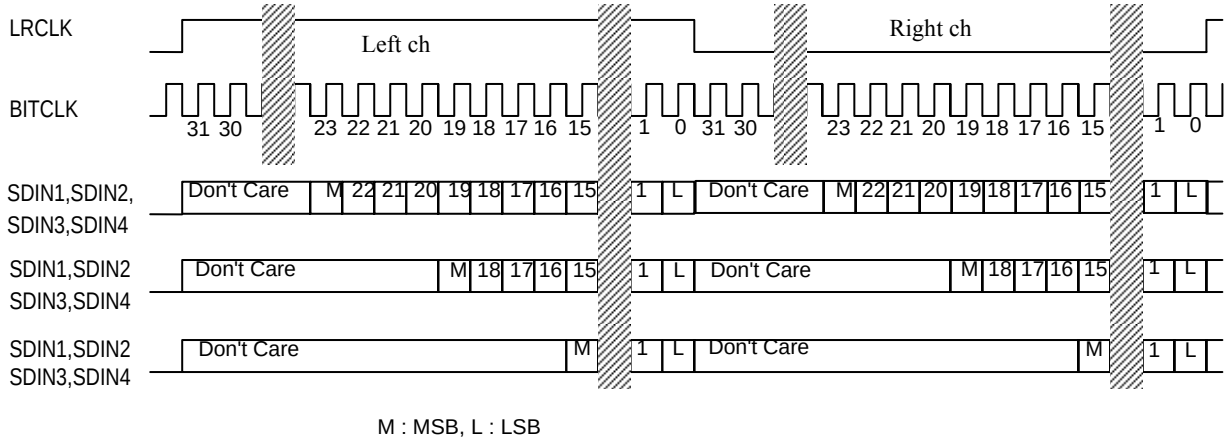
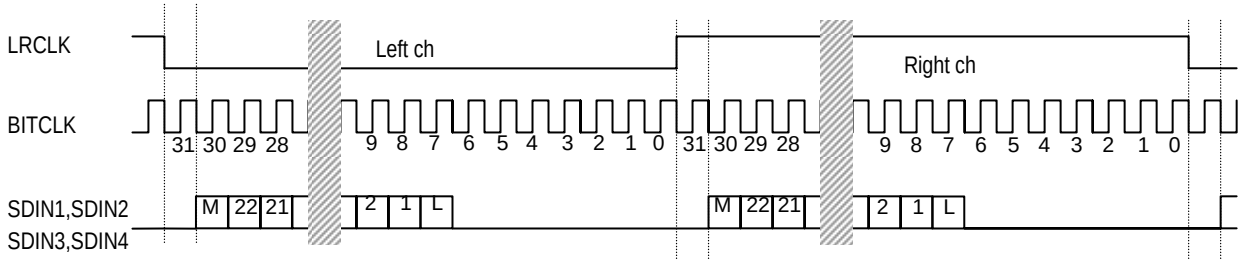


Fig.8-11

2) I²S compatible input format (DIFS=1)

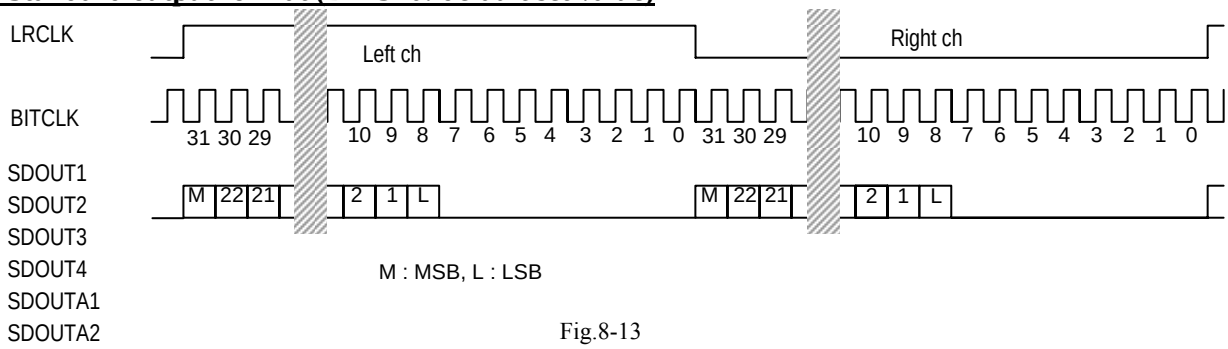


M : MSB, L : LSB

Mode 1: DIF[1:0]= 0 must be set.

Fig.8-12

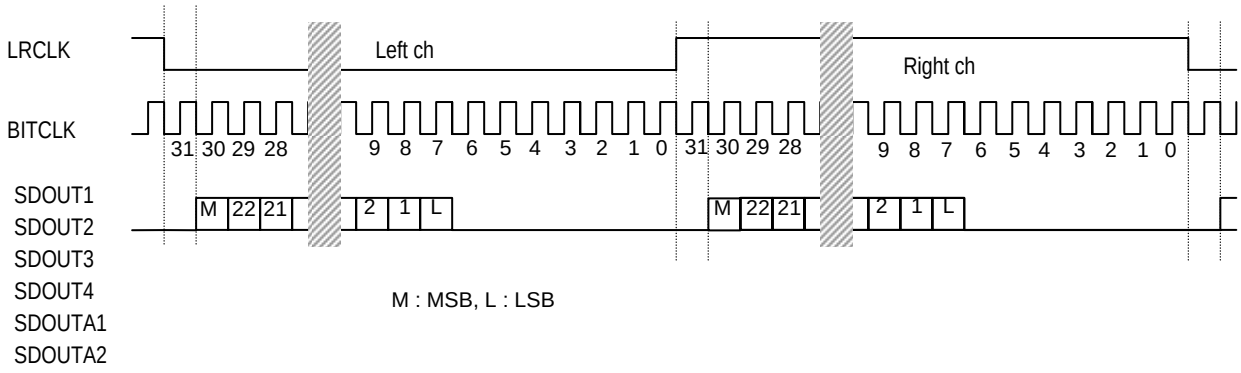
3) Standard output format (DIFS=0: default set value)



M : MSB, L : LSB

Fig.8-13

4) I²S compatible output format (DIFS=1)



M : MSB, L : LSB

Fig.8-14

(7) Interface with microcomputer

The microcomputer interface uses 6 control pins; $\overline{RQ}$ (ReQuest Bar), SCLK (Serial data input Clock), SI (Serial data Input), SO (Serial data Output), RDY (ReaDY) and DRDY (Data ReaDY).

In the AK7746, two types of operations are provided; writing and reading during the reset phase (system reset) and R/W during the run phase. During the reset phase, writing of the control register, program RAM, coefficient RAM, offset RAM, external conditional jump code, and reading of the program RAM, coefficient RAM and offset RAM are enabled. During the run phase, writing of coefficient RAM, offset RAM and external conditional jump code, and reading of data on the DBUS (data bus) from the SO, are enabled. Its data is MSB first serial I/O.

When the AK7746 transfers data to the microcomputer, it starts by $\overline{RQ}$ going "L" (Expects when reading the data on the DBUS). The AK7746 reads data at the rising point of SCLK from the SI pin, and outputs data on the falling edge of SCLK to the SO pin. The AK7746 first data is command code and then address data for the data input / output to start.

When $\overline{RQ}$ changes to "H", one command has finished. For a new command requests, set $\overline{RQ}$ to "L" again. For DBUS data reads, leave $\overline{RQ}$ ="H". (It does not need command code input.) To clear the output buffer (MICR), the SI pin is used. (In this case, it is necessary to protect against a noise as SCLK.)

The Command code table is as follows.

Command code list

Conditions for use	Code name	Command code		Remark:
		WRITE	READ	
RESET phase	CONT0	60h	70h	For the function of each bit, See the description of Control Registers.
	CONT1	62h	72h	
	CONT2	64h	74h	
	CONT3	66h	76h	
	CONT4	68h	78h	
	CONT5	6Ah	7Ah	
	PRAM	C0h	C1h	
	CRAM	A0h	A1h	
	OFRAM	90h	91h	
	External condition jump	C4h	-	
	CRC check (R(x))	B6h	D6h	
RUN phase	(CONT1~CONT7)	(Note 1)	7Xh	
	CONT3	66h	76h	Only CONT3 can use
	CRAM rewrite preparation	A8h	-	It needs to do before CRAM rewrite
	CRAM rewrite	A4h	-	
	OFRAM rewrite preparation	98h	-	It needs to do before OFRAM rewrite
	OFRAM rewrite	94h	-	
	External condition jump	C4h	-	Same code as RESET
	CRC check (R(x))	B6h	D6h	Same code as RESET

NOTE: Do not send other than the above command codes. Otherwise an operation error may occur.
If there is no communication with the microcomputer, set the SCLK to "H" and the SI to "L" for use.

Note 1) It is recommended that CONT1~CONT7 registers are also only written to at a system reset to avoid any unwanted noise. However, the CONT3 analog switch selectors can change during runtime.
[See. 8. (2) Control registers.]

1) Write during reset phase

a) Control register write (during reset phase)

The data comprises a set of 2 bytes used to perform control register write operations (during reset phase). When all data has been entered, the new data is sent at the rising edge of the 16th count of SCLK.

Data transfer procedure

① Command code	60h,62h,64h,66h,68h,6Ah,6Ch
② Control data	(D7 D6 D5 D4 D3 D2 D1 D0)

For the function of each bit, see the description of Control registers (p.25).

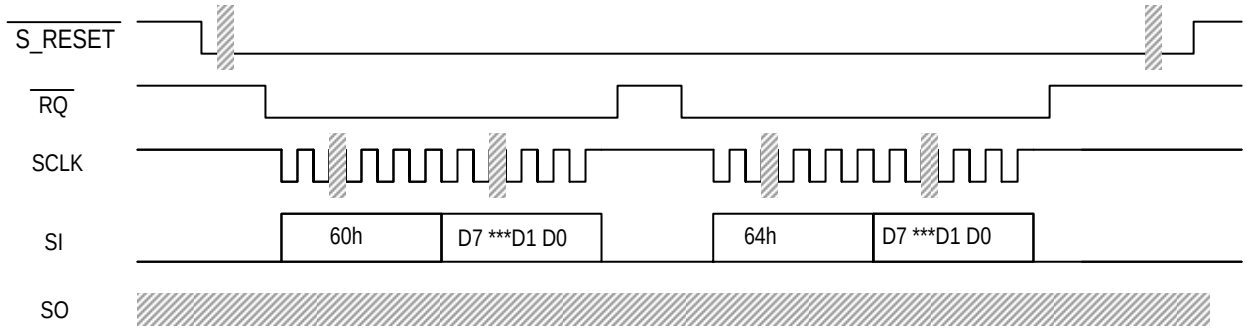


Fig .8-15 Control Registers write operation

b) Program RAM writes (during reset phase)

Program RAM write operations are performed during the reset phase using 7-bytes of data. When all data have been transferred, the RDY terminal is set to "L". Upon completion of writing into the PRAM, RDY returns “H” to allow the next data bit input. When writing to sequential addresses, input the data without a command code or address. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L" again and then input the command code, address and data in that order.

Data transfer procedure

① Command code	C0h (1 1 0 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 A9 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D31 . . . . . D24)
⑤ Data	(D23 . . . . . D16)
⑥ Data	(D15 . . . . . D8)
⑦ Data	(D7 . . . . . D0)

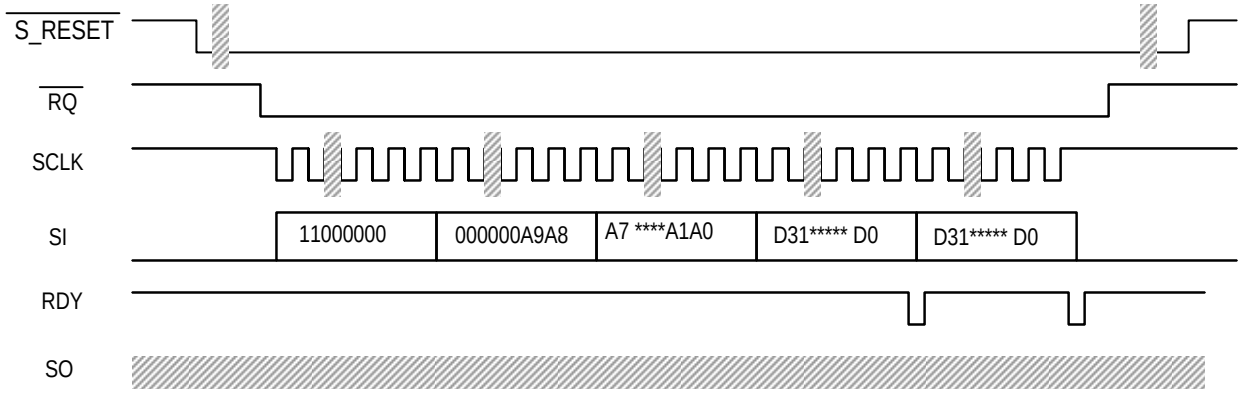


Fig.8-16 Input of continuous address data into PRAM

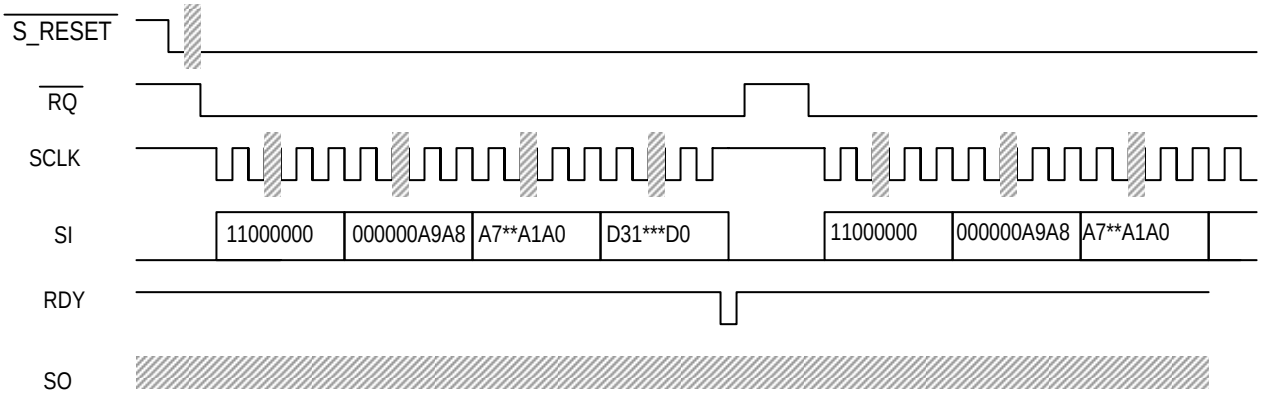


Fig.8-17 Input of discontinuous address data into PRAM

c) Coefficient RAM writes (during reset phase)

5 bytes of data are used to perform coefficient RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the CRAM, it goes to "H" to allow the next data to be input. When writing to sequential addresses, input the data as shown below. To write discontinuous data, transition the $\overline{RQ}$ terminal from "H" to "L" and then input the command code, address and data.

Data transfer procedure

① Command code	A0h (1 0 1 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 A9 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D15 . . . . . D8)
⑤ Data	(D7 . . . . . D0)

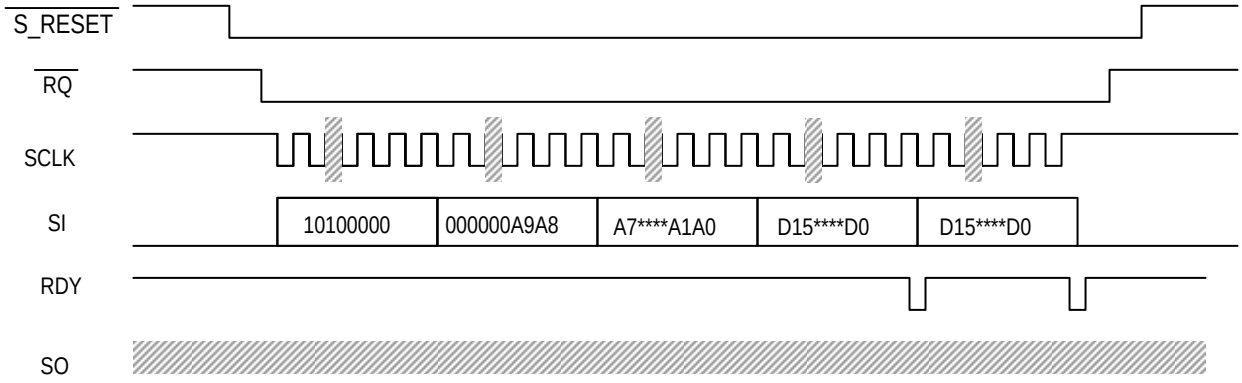


Fig.8-18 Input of continuous address data into CRAM

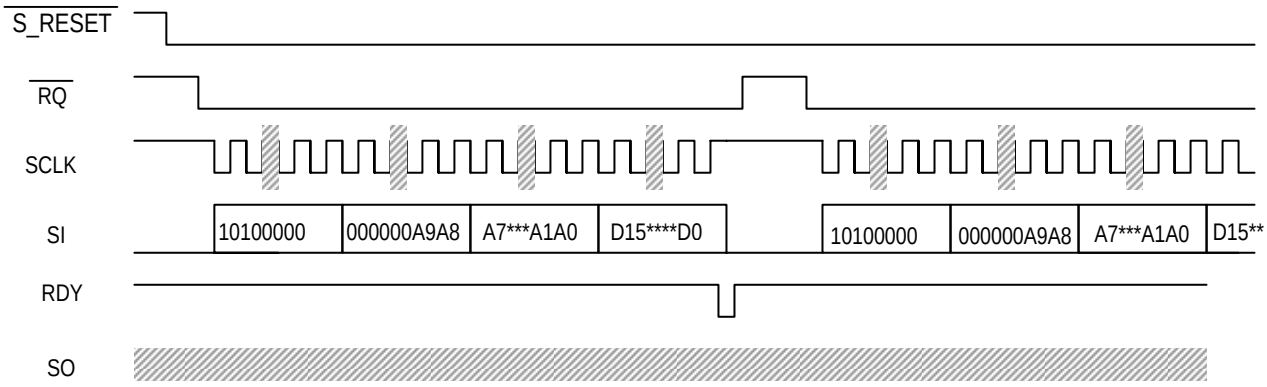


Fig.8-19 Input of discontinuous address data into CRAM

d) Offset RAM writes (during reset phase)

5 bytes of data are used to perform offset RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the OFRAM, it goes to "H" to allow the next data to be input. When writing to sequential addresses, input the data without a command code or address. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L" and then input the command code, address and data in that order.

Data transfer procedure

① Command code	90h (1 0 0 1 0 0 0 0)
② Address	(0 0 A5 A4 .. . . A0)
③ Data	(0 0 0 0 0 0 0 0)
④ Data	(0 0 0 D12 D11 * * . D8)
⑤ Data	(D7 . . . . . D0)

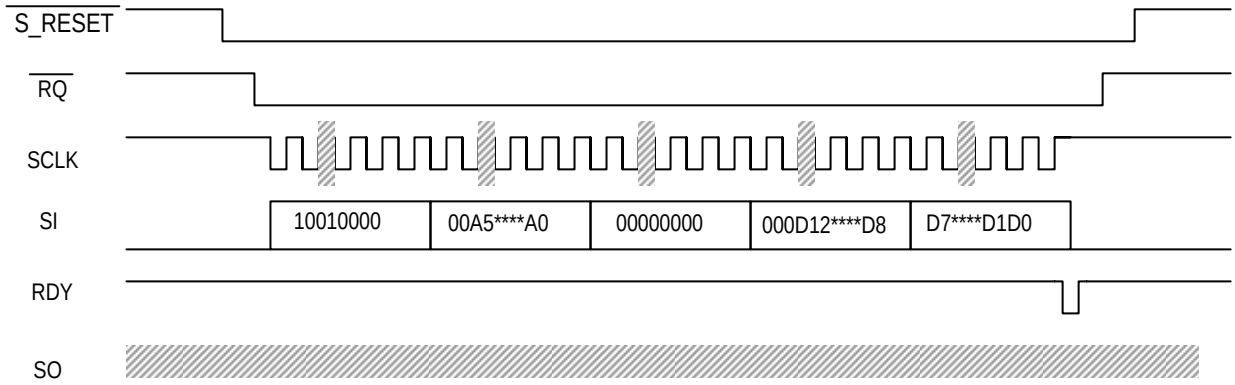


Fig.8-20 Input of data into OFRAM

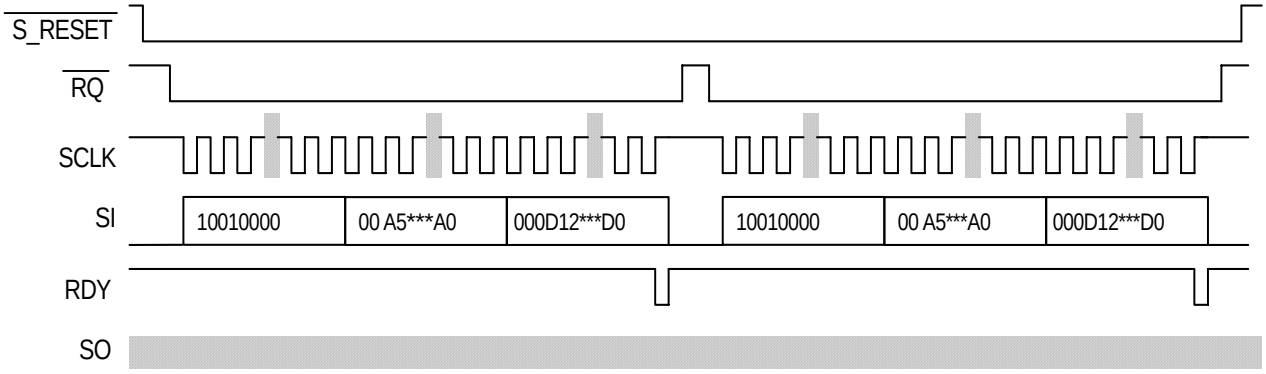
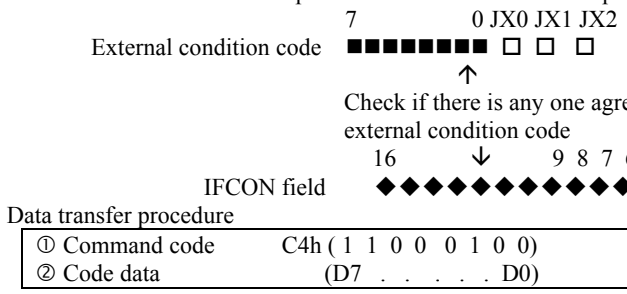


Fig.8-21 Input of discontinuous address data into OFRAM

e) External conditional jump code writes (during reset phase)

Two bytes of data are used to perform external conditional jump operations. The data can be entered during both the reset and operation phases, and the input data are set to the specified register at the leading edge of the LRCLK. When all data bits have been transferred, the RDY terminal goes to "L". Upon write completion, it goes to "H". A jump command will be executed if there is any one agreement between "1" of each bit of external condition code 8 bits (soft set) plus 3 bits (hard set) at the external input terminal JX0, JX1,JX2 and "1" of each bit of the IFCON field. The data during the reset phase can be written only before release of the reset, after all data has been transferred. $\overline{RQ}$ Transition from "L" to "H" in the write operation during the reset phase must be executed after three LRCLK in the slave mode or one LRCLK in master mode, respectively, from the trailing edge of the LRCLK after release of the reset. Then the RDY goes to "H" after capturing the rise of the next LRCLK. A write operation from the microcomputer is disabled until the RDY goes to "H". The IFCON field provides external conditions written on the program. It resets to 00h by $\overline{INIT\_RESET}$ ="L", however, it remains previous condition even $\overline{S\_RESET}$ ="L".

Note: It should be noted that the LRCLK phase is inverted in the I^2S-compatible state.



Data transfer procedure

① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)

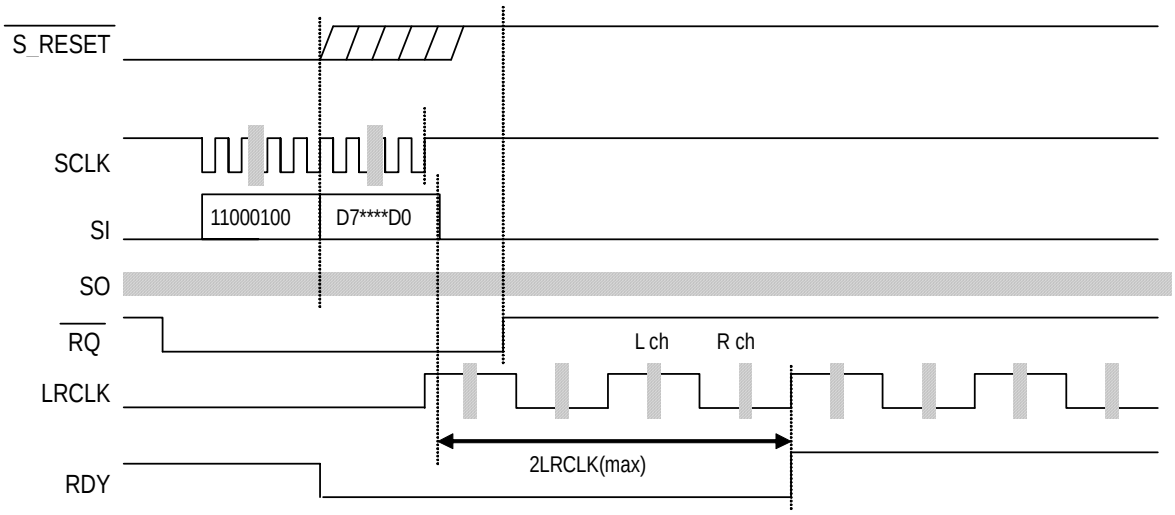


Fig.8-22 Timing for external conditional jump write operation (during reset phase)

2) Read during reset phase

a) Control register data read (during reset phase)

To read data written into the control registers, input the command code and 16 bits of SCLK. After the input command code, the data of D7 to D1 outputs from SO is synchronized with the falling edge of SCLK. D0 is invalid, so please ignore this bit.

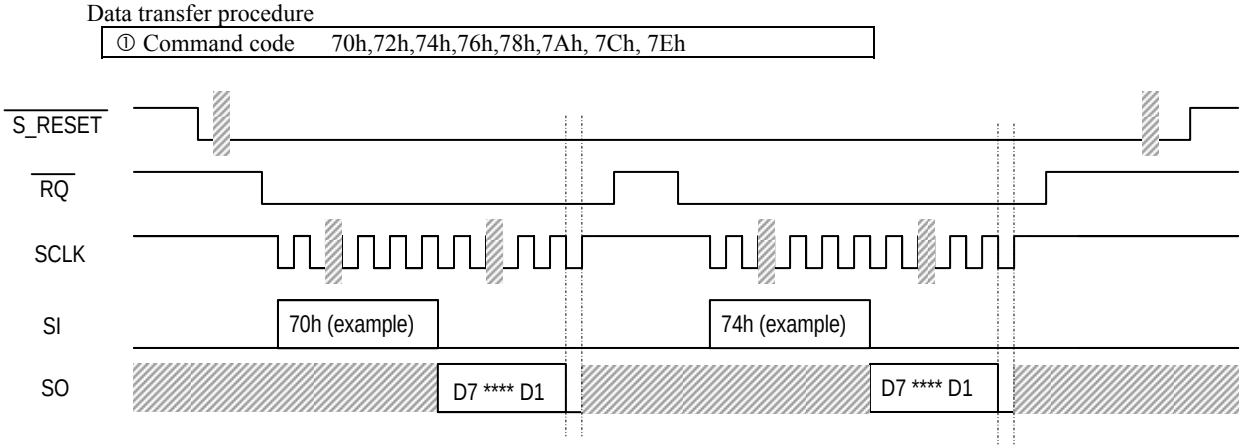


Fig.8-23 Reading of Control Register data

b) Program RAM read (during reset phase)

To read data written into PRAM, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". The data is then clocked out from SO in synchronization with the falling edge of SCLK. (Ignore the RDY operation that will occur in this case.)
If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

①Command code input C1h (1 1 0 0 0 0 0 1)
②Read address input MSB (0 0 0 0 0 0 A9 A8)
③Read address input LSB (A7 . . . . A0)

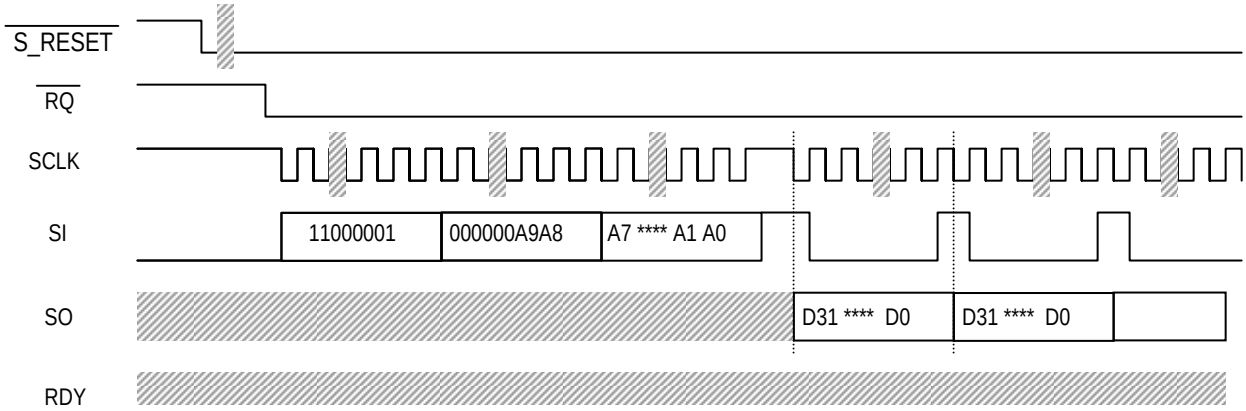


Fig.8-24 Reading of PRAM data

c) CRAM data read (during reset phase)

To read out the written coefficient data, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". The data is clocked out from SO in synchronization with the falling edge of SCLK. If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

① Command code	A1h (1 0 1 0 0 0 0 1)
② Address upper	(0 0 0 0 0 0 A9 A8)
③ Address lower	(A7 . . . . . A0)

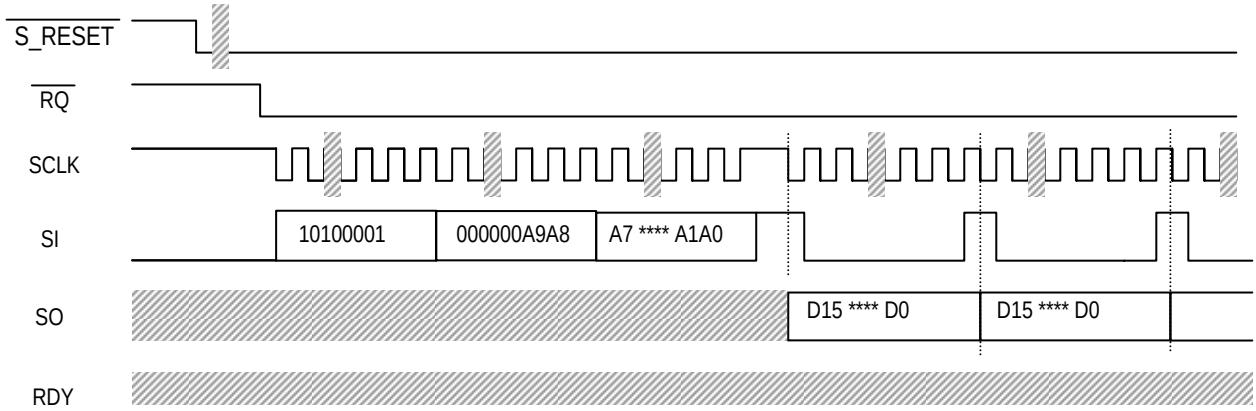


Fig.8-25 Reading of CRAM data

d) OFRAM data read (during reset phase)

The written offset data can be read out during the reset phase. To read it, input the command code and the address you want to read. After that, set SI to "H" and SCLK to "L". This completes preparation for outputting the data. Then set SI to "L", and the data is clocked out in synchronization with the falling edge of SCLK. If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to “H”.

Data transfer procedure

① Command code 91h (1 0 0 1 0 0 0 1)
② Address (0 0 A5 . . . . A0)

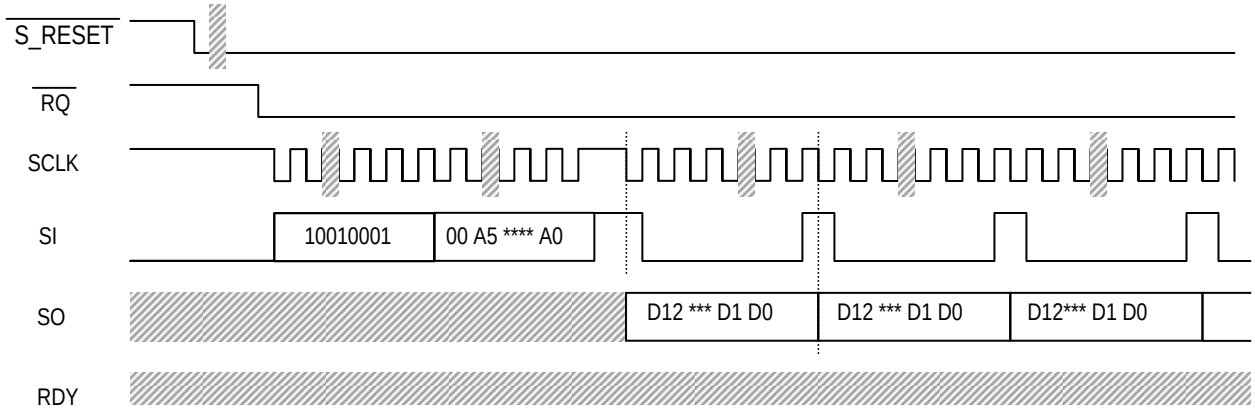


Fig.8-26 Reading of OFRAM data

3) Write during RUN phase

a) CRAM rewrites preparation and writes (during RUN phase)

This function is used to rewrite CRAM (coefficient RAM) during program execution. After inputting the command code, you can input a maximum of 16 data (2 bytes 1set) of a continuous address you want to rewrite, then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the coefficient RAM are rewritten:

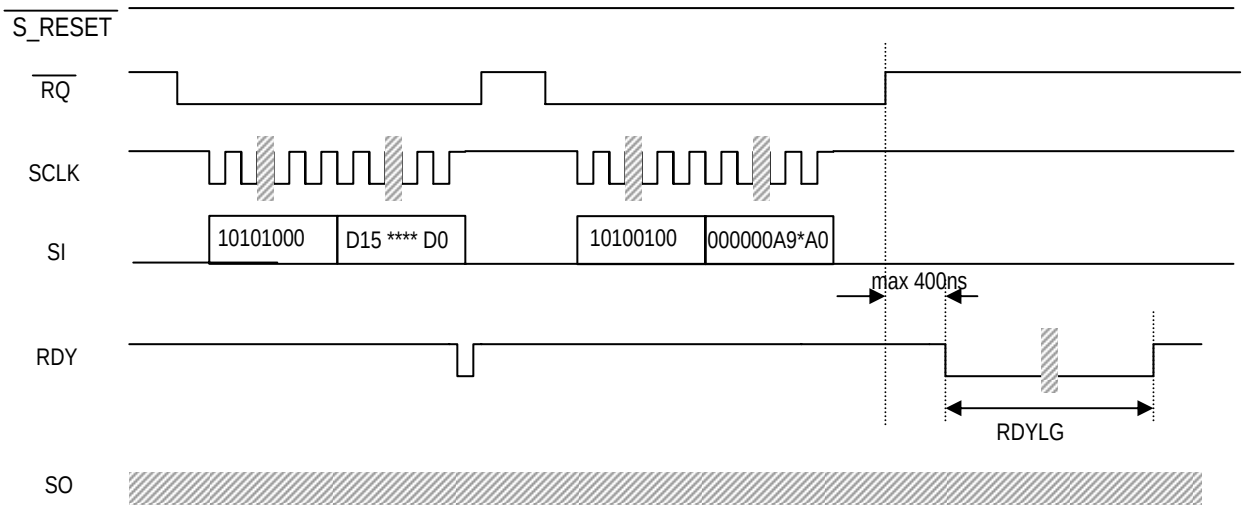
Coefficient RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position ↓ ↓ ↓ ↓ ↓ ↓

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code	A8h	(1 0 1 0 1 0 0 0)
	② Data		(D15 . . . . D8)
	③ Data		(D7 . . . . . D0)
* Rewrite	① Command code	A4h	(1 0 1 0 0 1 0 0)
	② Address upper		(0 0 0 0 0 0 A9 A8)
	③ Address lower		(A7 . . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

Fig. 8-27 CRAM rewriting preparation and writing

b) OFRAM rewrites preparation and writes (during RUN phase)

This function is used to rewrite OFRAM (offset RAM) during program execution. After inputting the command code, you can input a maximum of 16 data (3 bytes 1 set) of a continuous address you want to rewrite.
Then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the offset RAM are rewritten:

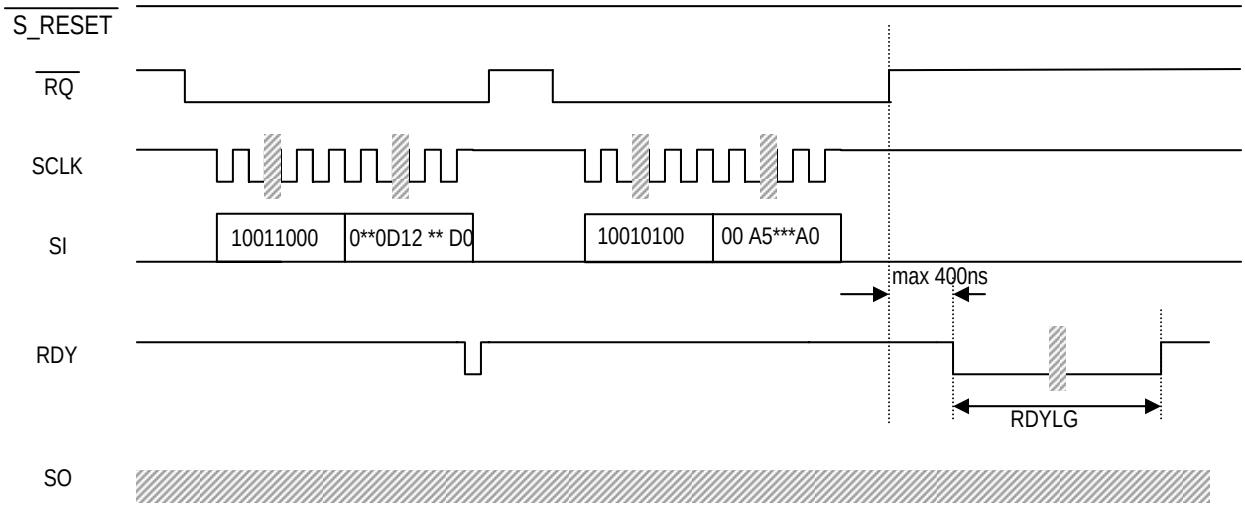
Offset RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position ↓ ↓ ↑ ↓ ↓ ↓

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code 98h	(1 0 0 1 1 0 0 0)
	② Data	(0 0 0 0 0 0 0 0)
	③ Data	(0 0 0 D12 . . . D8)
	④ Data	(D7 . . . . . D0)
* Rewrite	① Command code 94h	(1 0 0 1 0 1 0 0)
	② Address	(0 0 A5A4 . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

Fig.8-28 OFRAM rewriting preparation and writing

c) External conditional jump code rewrite (during RUN phase)

Two data bytes are used to write an external conditional jump code. Data can be input during both the reset and operation phases, and input data is set to the specified register at the rising edge of LRCLK. When all data has been transferred, the RDY pin goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between each bit of the 8-bit external condition code and "1"of each bit of the IFCON field. A write operation from the microcomputer is disabled until RDY goes to "H".

Note: The LRCLK phase is inverted in the I^2S-compatible state.

Data transfer procedure

① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)

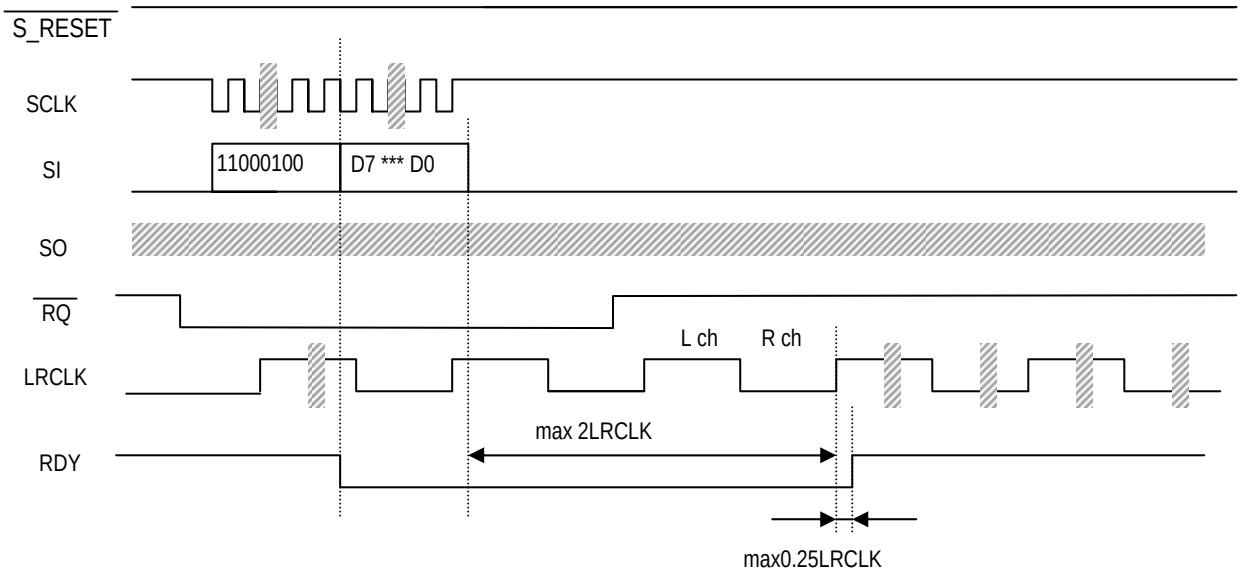


Fig.8-29 External condition jump write timing (during RUN phase)

4) Read-out during RUN phase (SO output)

a) Control register data read (during run phase)

The control register can read during run time. To read data written into the control registers, input the command code and 16 bits of SCLK. After the input command code, the data of D7 to D1 outputs from SO is synchronized with the falling edge of SCLK. D0 is invalid, so please ignore this bit.

Data transfer procedure

① Command code	70h,72h,74h,76h,78h,7Ah, 7Ch, 7Eh

In order to know the each bit function, see 8. Function description (2) Control registers.

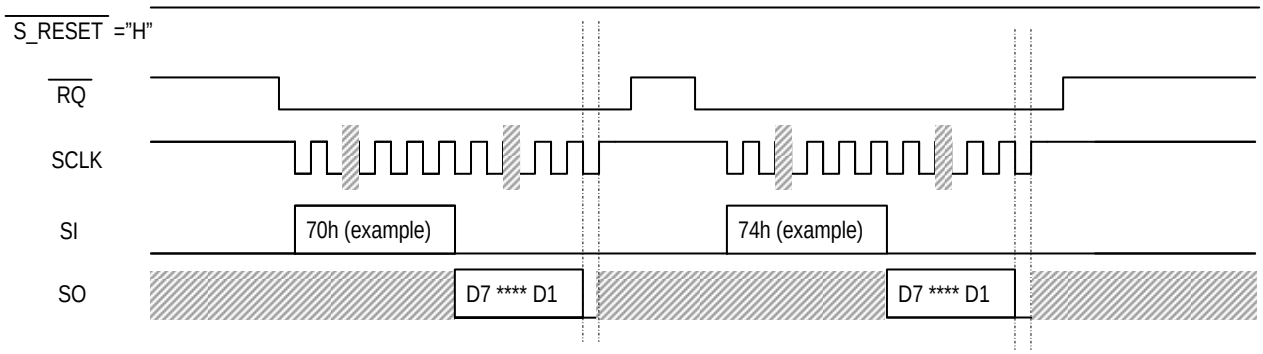


Fig.8-30 Control register read (during RUN phase)

b) SO data read (during run phase)

SO outputs data on DBUS (data bus) of the DSP section. Data is set when @MICR the DST field specifies. Setting of data allows DRDY to go to "H", and data is output synchronized with the falling edge of SCLK. When SI goes to "H", DRDY goes to "L" to wait for the next command. Once DRDY goes to "H", the data of the last @MICR command immediately before DRDY goes to "H" will be held until SI goes to "H" or read out 24-bit data with SCLK, and subsequent commands will be rejected. A maximum of 24 bits are output from SO.

Note) In the case of read out 24-bit data, DRDY falls down when 24th SCLK rising edge and SO output bit is not stable. So, if the microcontroller cannot read out at SCLK rising edge, it should ignore the last 1bit (D0).

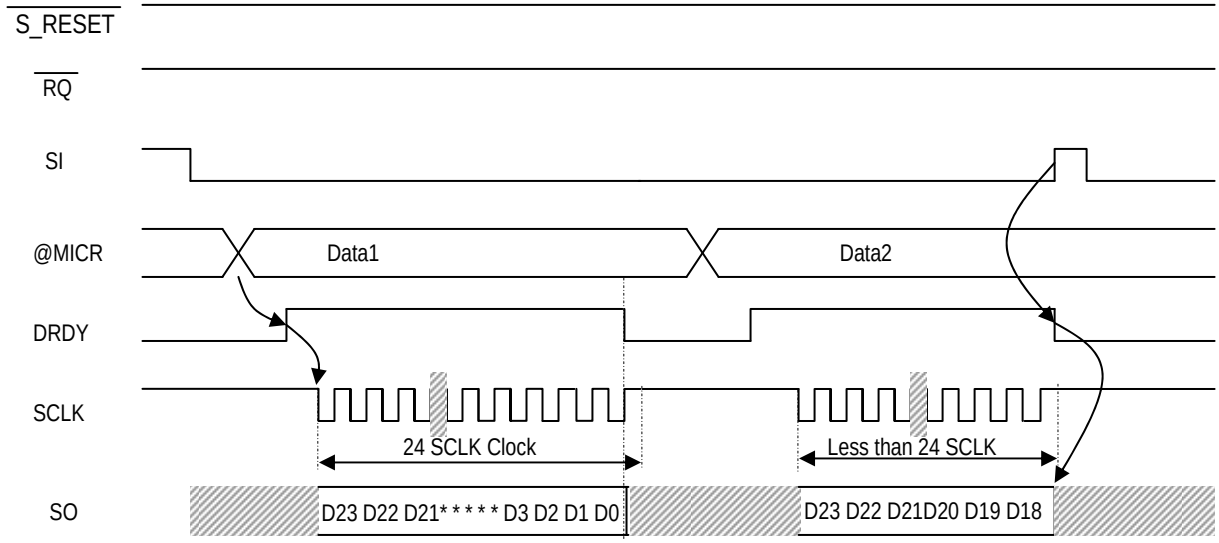


Fig.8-31 SO read (during RUN phase)

5) Simple error check for communication

The AK7746 has a simple CRC error check function.

(Note: Its main purpose is checking against the noise effects during writes from microprocessor to the AK7746. This check CANNOT guarantee 100% error detection on the AK7746.
Explanation:

* Serial data(X): Input SI data from $\overline{RQ}$ fall to rise up.
* Generator polynomial G(x) =$x^{16}+x^{12}+x^5+1$ (X.25 of CCITT standard order of hexadecimal is 11021h).
* The rest of D(x) divides by G(x) is R(x).
  This division is using exclusive-or instead of subtraction during this calculation.
  It makes good 16-bit zero data after translated serial data D(X) and the rest R(X) of this division comes out 16bit data.

In order to do simple error check is as following:

1) Use the command code B6h and write the R(x) (the rest result of serial data D(x) divided by G(x)).
2) Then use the command code D6h and read out R(x) to check whether the R(x) is correct or not. (Unless this read out, CRC check itself works.)
3) If the result of D(x) divided by G(x) is equal to R(x), SO outputs "H" from the next rising edge of $\overline{RQ}$ to falling edge of $\overline{RQ}$. (However, SO read out from micro-controller is prior to this signal. Refrain from a runtime read out while doing CRC check.) If R(x) is not equal to the result, it outputs "L".
4) If you want to check other serial data, then repeat action form 1) to 3).

Note) In the case of detecting CRC error in runtime "CRAM rewrite" (A4h) or "OFRAM rewrite"(94h), the possibility of writing data to the wrong address exists.

* Specific order of data translates.

1) Write the register

The rest R(x) data writing is using 3-byte/unit (24bit)

Data translate order.

①Command code B6h
②Upper 8bit of R(x) (D15 * * * * * * D8)
③Lower 8bit of R(x) (D7 * * * * * * D0)

2) Read out the register

The rest R(x) data reading out is 3-byte/unit (24bit)

Data translate order

①Command code D6h
②Upper 8bit of R(x) (D15 * * * * * * D8)
③Lower 8bit of R(x) (D7 * * * * * * D0)

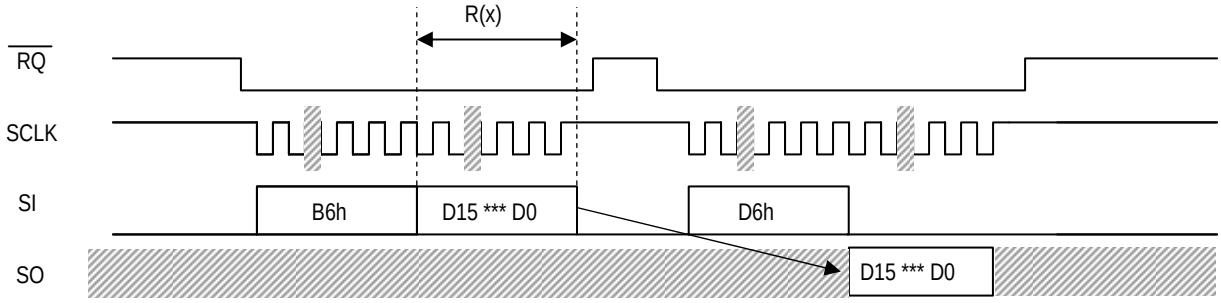


Fig.8-32 Example: Control register writing, reading

3) CRC Check

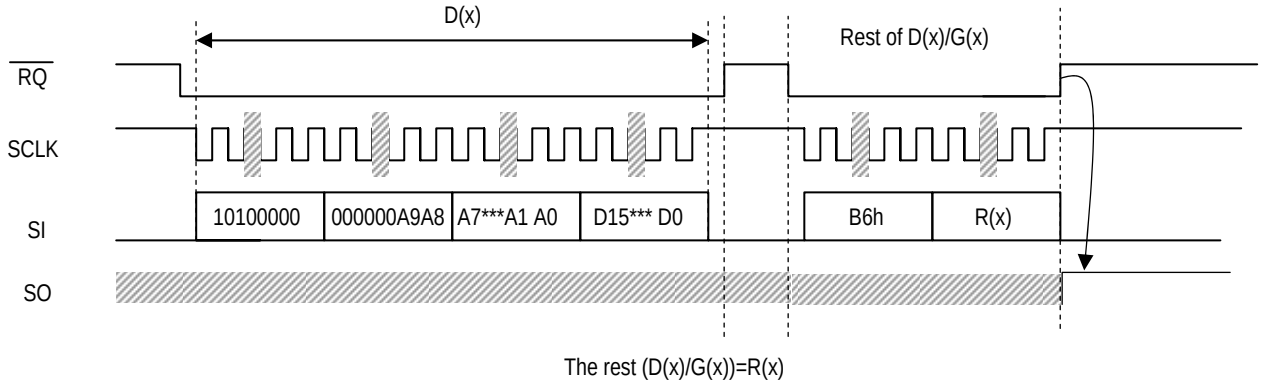


Fig.8-33 The rest of D(x)/G(x)=R(x) CRC Check example.

4) Example of the R(x) made from D(x).

Examples	D(X)	R(X)
1	D6ABCDh	1E51h
2	D2A5A5h	0C30h
3	A855557777AAAA0000FFFFh	2297h

6) ADC high-pass filter

The AK7746 incorporates a digital high-pass filter (HPF) for canceling DC offset in the ADC. The HPF cut-off frequency is about 1 Hz (fs = 48 kHz). This cut-off frequency is proportional to the sampling frequency (fs).

	96kHz	48kHz	44.1kHz	32kHz	8kHz
Cut-off frequency	1.86Hz	0.93Hz	0.86Hz	0.62Hz	0.16Hz

9. System Design

(1) Connection example

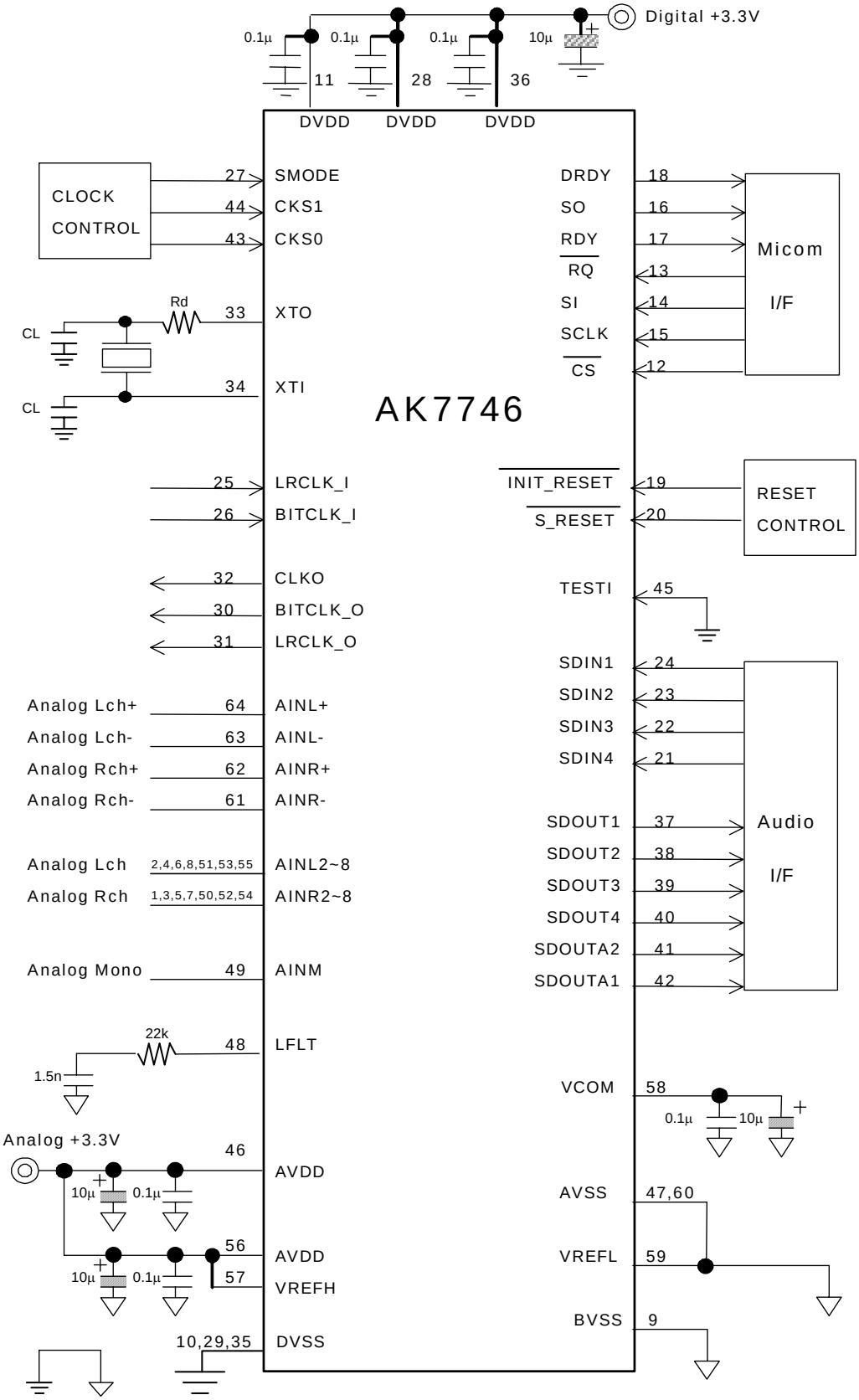


Fig.9-1

(2) Peripheral circuit

1) Ground and power supply

To minimize digital noise coupling, AVDD and DVDD should be individually de-coupled at the AK7746. System analog power is supplied to AVDD.

Generally, power supply and ground wires must be connected separately according to the analog and digital systems. Connect them at a position close to the power source on the PCB board. Decoupling capacitors and ceramic capacitors of small capacity in particular, should be connected at positions as close as possible to the AK7746.

2) Reference voltage

The input voltage difference between the VREFH pin and the AVSS pin determines the full scale of analog input. Normally, connect AVDD to VREFH, and connect 0.1μF ceramic capacitors from them to AVSS. To shut out high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between this pin and AVSS. The ceramic capacitor in particular should be connected as close as possible to the pin. To avoid coupling to the AK7746, digital signals and clock signals should be kept away as far as possible from the VREFH pin.

VCOM is used as the common voltage of the analog signal.To filter out high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between this pin and AVSS. The ceramic capacitor should be connected as close as possible to the pin. Do not draw current from the VCOM pin.

3) Analog input

Analog input signals are applied to the modulator through the differential input pins of each channel. The input voltage is equal to the differential voltage between AIN+ and AIN- (ΔVAIN = (AIN+) - (AIN-)), and the input range is ±FS = ±(VRADH - VRADL) × 2.0/3.3. When VRADH = 3.3V and VRADL = 0V, the input range is within ±2.00V. The output code format is given in terms of 2's complements.

When fs = 48 kHz, the AK7746 samples the analog input at 3.072 MHz. The digital filter eliminates noise from 30 kHz to 3.042 MHz. However, noise is not rejected in the bandwidth close to 3.072 MHz. Most audio signals do not have large noise in the vicinity of 3.072 MHz, so a simple RC filter is sufficient.

The analog source voltage to the AK7746 is +3.3V(Typ.). Voltage of AVDD + 0.3 V or more, voltage of AVSS - 0.3 V or less, and current of 10 mA or more must not be applied to analog input pins (AINL and AINR). Excessive current will damage the internal protection circuit and will cause latch-up, thereby damaging the IC. Accordingly, if the surrounding analog circuit voltage is ±15 V, the analog input pins must be protected from signals with the absolute maximum rating or more.

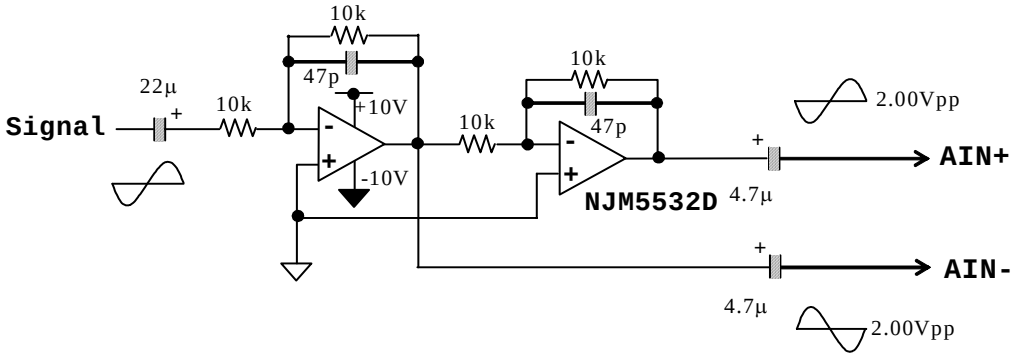


Fig.9-2 Example of the input buffer circuit (Differensial input)

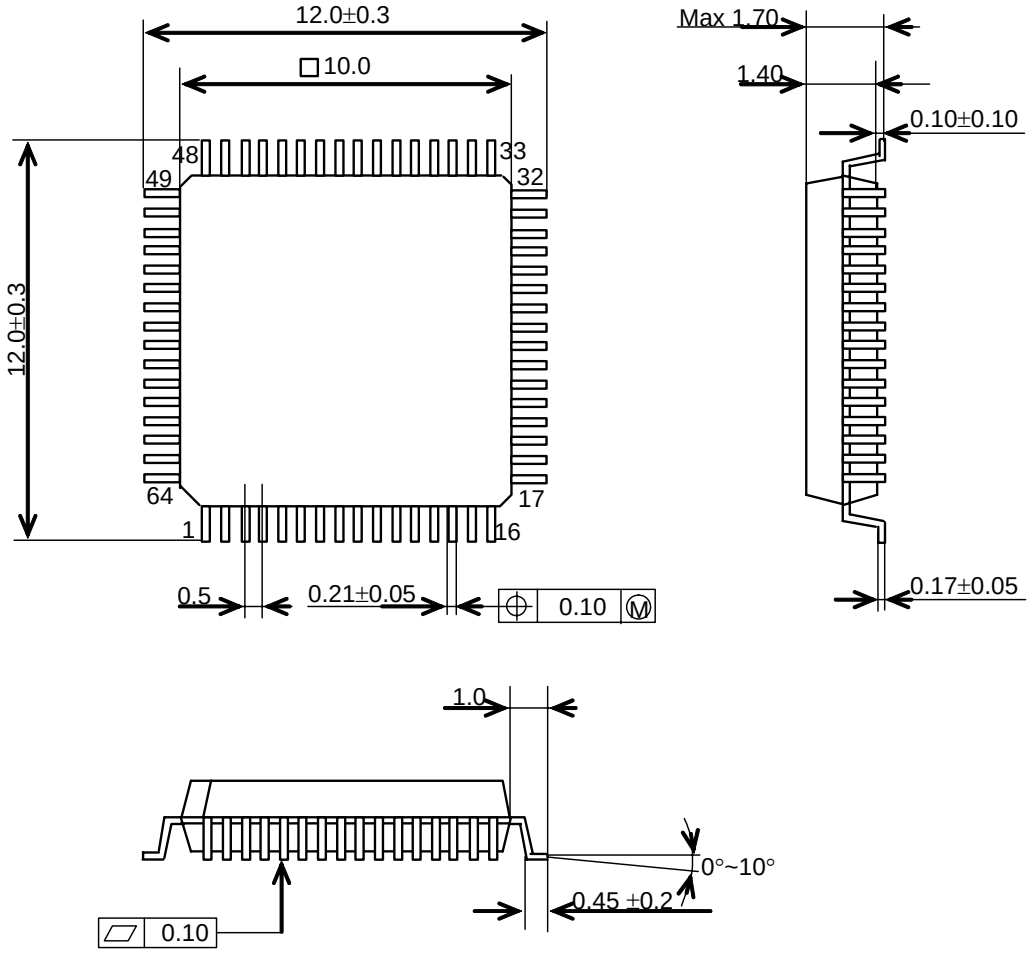
The internal center level (AVDD/2) for the analog input pins of the AK7746 (AINL+, AINL-, AINR+, AINR-, AINL2~L8, AINR2~R8 and AINM) is made after initial reset release.

4) Connection to digital circuit

To minimize the noise resulting from the digital circuit, connect low voltage logic to the digital output. The applicable logic family includes the 74LV, 74LV-A, 74ALVC and 74AVC series.

10. Package

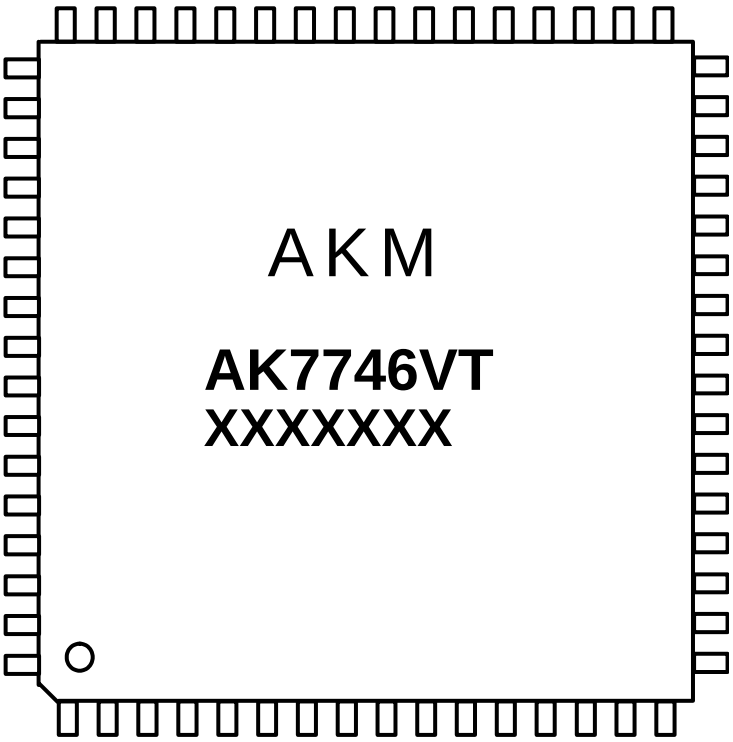
- 64pin LQFP (Unit : mm)



- Material & Lead finish

Package: Epoxy
Lead-frame: Copper
Lead-finish: Soldering plate

11. Marking



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK7746VT
4) Asahi Kasei Logo

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd.(AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  (a): A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b): A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.