ACCUTEK
MICROCIRCUIT CORPORATION

AK63232Z
32,768 x 32 Bit CMOS / BiCMOS Static Random Access Memory

DESCRIPTION

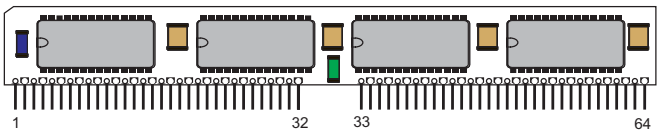
The Accutek AK63232Z SRAM Module consists of fast high performance SRAMs mounted on a low profile, 64 pin ZIP Board. The module utilizes four 28 pin 32K x 8 SRAMs in 300 mil SOJ packages and four decoupling capacitors mounted on the front side of a printed circuit board.

The SRAMs used have common I/O functions and single output enable functions. Also, four separate chip select ($\overline{CE}$) connections are used to independently enable the four bytes. The modules can be supplied in a variety of access time values from 8 nSEC to 45 nSEC in CMOS or BiCMOS technology.

The Accutek module is designed to have a maximum seated height of 0.500 inch. The module conforms to JEDEC-standard sizes and pin-out configurations. This, along with use of two pins for module memory density identification, PD_0 and PD_1, minimizes interchangeability and design considerations when changing from one module size to the other in customer applications.

Top View

64-Pin ZIP



FEATURES

- 32,768 x 32 bit organization
- JEDEC standard 64 pin ZIP format
- Common I/O, single $\overline{OE}$ functions with four separate chip selects ($\overline{CE}$)
- Low height, 0.500 inch maximum seated height
- Upward compatible with 64K x 32 (AK63264), 256K x 32 (AK632256), 512K x 32 (AK632512) and 1 Meg x 32 (AK6321024)
- Presence Detect, PD_0 and PD_1 for identifying module density
- Fast Access Times range from 8 nSEC BiCMOS to 45 nSEC CMOS
- TTL compatible inputs and outputs
- Single 5 volt power supply - AK63232Z
- Single 3.3 volt power supply - AK63232Z/3.3
- Operating temperature range in free air, 0^0Ct o7 0^0C

PIN NOMENCLATURE

A_0 - A_{14}	Address Inputs
$\overline{CE}_1$ - $\overline{CE}_4$	Chip Enable
DQ_1 - DQ_{32}	Data In/Data Out
$\overline{OE}$	Output Enable
PD_0 - PD_1	Presence Detect
Vcc	Power Supply
Vss	Ground
$\overline{WE}$	Write Enable

MODULE OPTIONS

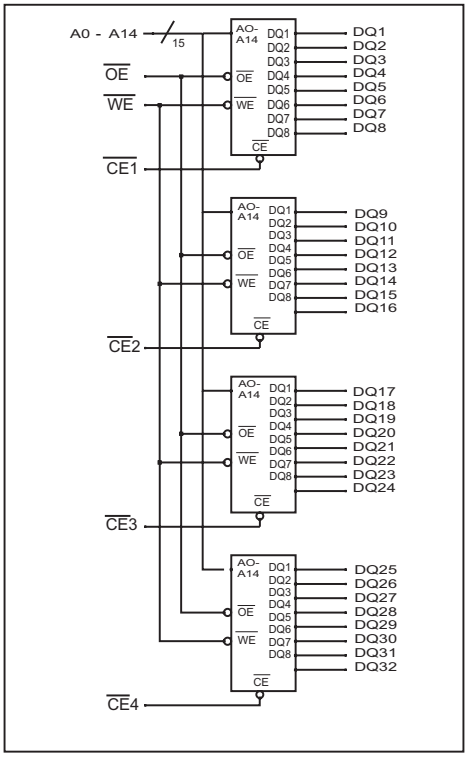
Leaded ZIP: AK63232Z

PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	17	A2	33	CE4	49	A4
2	PD0	18	A9	34	CE3	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	OE	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	WE	44	DQ19	60	DQ23
13	A0	29	NC	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	CE2	47	A3	63	DQ32
16	A8	32	CE1	48	A10	64	Vss

PD0 = Open
PD1 = Open

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8

1 Product

AK = Accutek Memory

2 Type

4 = Dynamic RAM
5 = CMOS Dynamic RAM
6 = Static RAM

3 Organization/Word Width

1 = by 1 16 = by 16
4 = by 4 32 = by 32
8 = by 8 36 = by 36
9 = by 9

4 Size/Bits Depth

64 = 64K 4096 = 4 MEG
256 = 256K 8192 = 8 MEG
1024 = 1 MEG 16384 = 16 MEG

5 Package Type

G = Single In-Line Package (SIP)
S = Single In-Line Module (SIM)
D = Dual In-Line Package (DIP)
W = .050 inch Pitch Edge Connect
Z = Zig-Zag In-Line Package (ZIP)

6 Special Designation

P = Page Mode
N = Nibble Mode
K = Static Column Mode
W = Write Per Bit Mode
V = Video Ram

7 Separator

- = Commercial 0^0C to +70^0C
M = Military Equivalent Screened (-55^0C to +125^0C)
I = Industrial Temperature Tested (-45^0C to +85^0C)
X = Burned In

8 Speed (first two significant digits)

DRAMS			SRAMS		
50	=	50 nS	8	=	8 nS
60	=	60 nS	12	=	12 nS
70	=	70 nS	15	=	15 nS
80	=	80 nS	20	=	20 nS

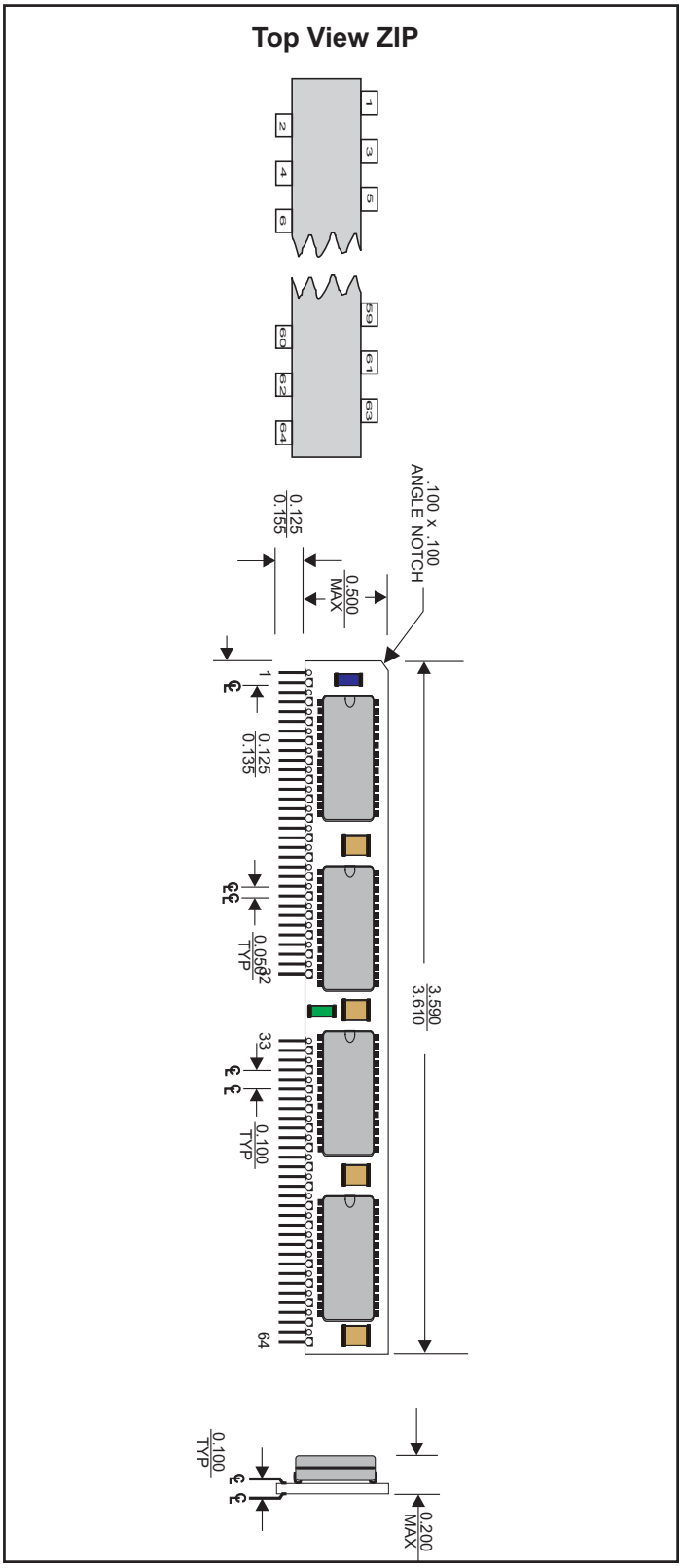
The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accutek if other information is required.

EXAMPLES:

AK63232Z-12

MECHANICAL DIMENSIONS

Inches



Accutek reserves the right to make changes in specifications at any time and without notice. Accutek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.

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