AK5806
8ch Analog Front End IC

1. General description

The AK5806 is an 8 channels analog baseband IC with third order HPF, whose cutoff frequency is variable, and programmable gain amplifiers.
It is capable of adjusting the baseband signal gain and the frequency band widely.

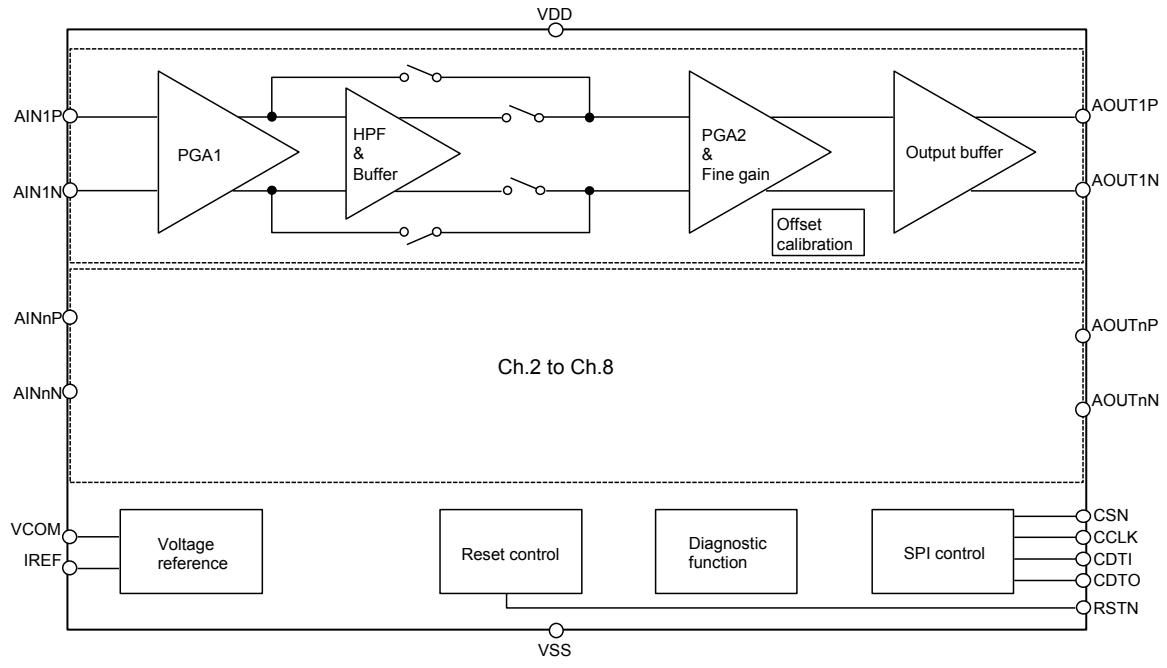
2. Features

- Signal Processing: 8-channel Differential I/O
- Signal band width: up to 5MHz
- Programmable Gain Amplifier:
  (Coarse) 0dB to 42dB, 6dB/step (Fine) −6dB to +5.625dB, 0.375dB/step
- 3rd-order HPF with Adjustable Cutoff Frequency: 25 kHz to 1MHz
- Offset Cancelling Function
- Operational Temperature: −40 to 125ºC
- Package: 64-pins HTQFP

3. Application

- Millimeter wave radar
- Laser rangefinder
- Ultrasonic sensor
- Signal conditioning before AD conversion
  etc.

4. Block diagram



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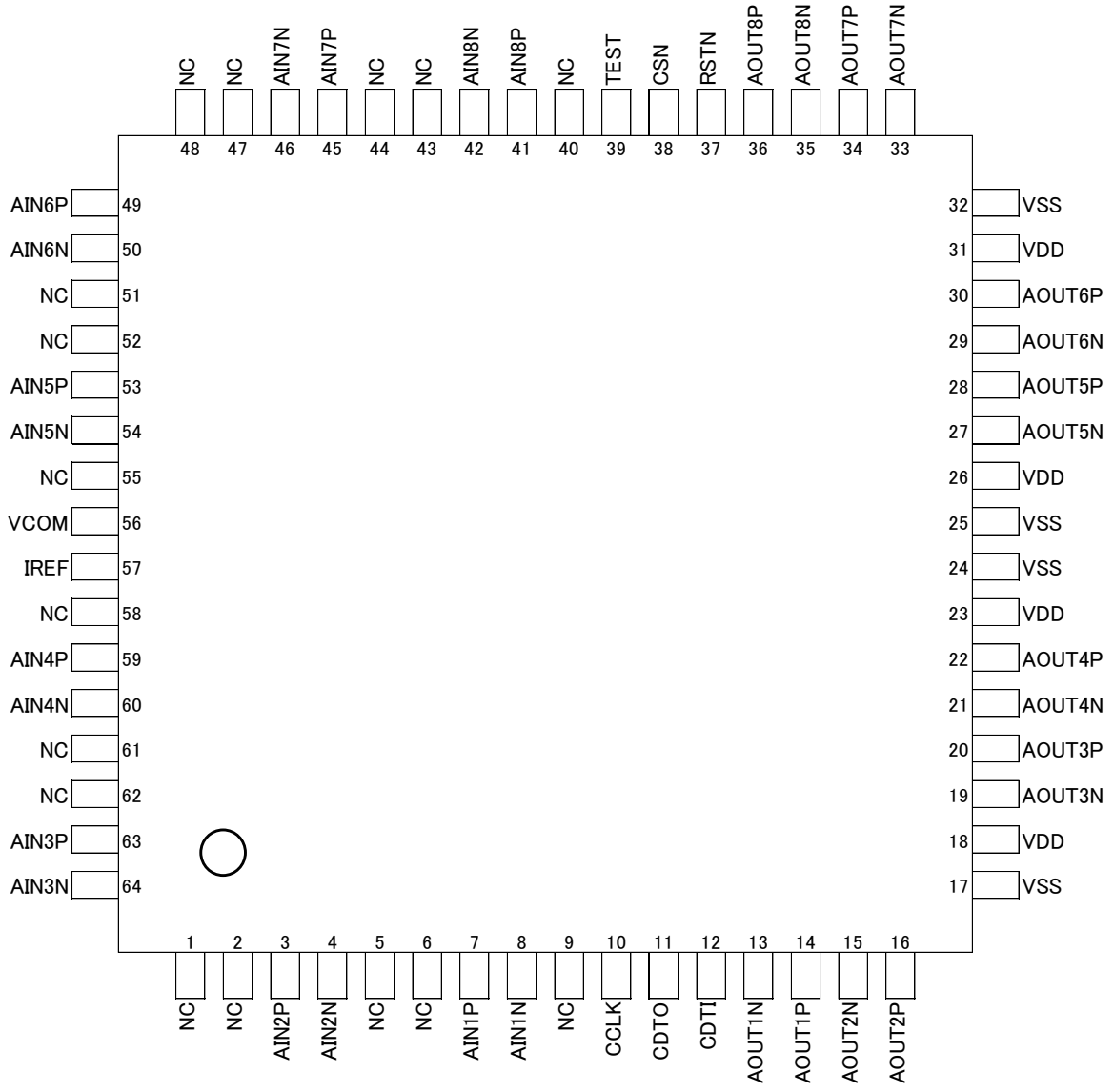
6. Pin layout and functions

6.1. Pin layout



TOP View
Figure 2

6.2. Pin functions

Pin #	Pin name	I/O	Function
1	NC	I	No connect pin. Connect to No.64 pin.
2	NC	I	No connect pin. Connect to No.3 pin.
3	AIN2P	I	Analog Signal Input Pin
4	AIN2N	I	Analog Signal Input Pin
5	NC	I	No connect pin. Connect to No.4 pin.
6	NC	I	No connect pin. Connect to No.7 pin.
7	AIN1P	I	Analog Signal Input Pin
8	AIN1N	I	Analog Signal Input Pin
9	NC	I	No connect pin. Connect to No.8 pin.
10	CCLK	I	Clock Input Pin for SPI Communication
11	CDTO	O	Data Output Pin for SPI Communication
12	CDTI	I	Data Input Pin for SPI Communication
13	AOUT1N	O	Analog Signal Output Pin
14	AOUT1P	O	Analog Signal Output Pin
15	AOUT2N	O	Analog Signal Output Pin
16	AOUT2P	O	Analog Signal Output Pin
17	VSS	-	Ground pin
18	VDD	-	Power Supply pin
19	AOUT3N	O	Analog Signal Output Pin
20	AOUT3P	O	Analog Signal Output Pin
21	AOUT4N	O	Analog Signal Output Pin
22	AOUT4P	O	Analog Signal Output Pin
23	VDD	-	Power Supply pin
24	VSS	-	Ground pin
25	VSS		Ground pin
26	VDD		Power Supply pin
27	AOUT5N	O	Analog Signal Output Pin
28	AOUT5P	O	Analog Signal Output Pin
29	AOUT6N	O	Analog Signal Output Pin
30	AOUT6P	O	Analog Signal Output Pin
31	VDD	-	Power Supply pin
32	VSS	-	Ground pin
33	AOUT7N	O	Analog Signal Output Pin
34	AOUT7P	O	Analog Signal Output Pin
35	AOUT8N	O	Analog Signal Output Pin
36	AOUT8P	O	Analog Signal Output Pin
37	RSTN	I	Reset Input Pin (Internal Pull-down)
38	CSN	I	Chip Select Input Pin for SPI Communication
39	TEST	I	AKM Test Mode Pin. It must be connected to VSS.
40	NC	I	No connect pin. Connect to No.41 pin.
41	AIN8P	I	Analog Signal Input Pin
42	AIN8N	I	Analog Signal Input Pin
43	NC	I	No connect pin. Connect to No.42 pin.

Pin #	Pin name	I/O	Function
44	NC	I	No connect pin. Connect to No.45 pin.
45	AIN7P	I	Analog Signal Input Pin
46	AIN7N	I	Analog Signal Input Pin
47	NC	I	No connect pin. Connect to No.46 pin.
48	NC	I	No connect pin. Connect to No.49 pin.
49	AIN6P	I	Analog Signal Input Pin
50	AIN6N	I	Analog Signal Input Pin
51	NC	I	No connect pin. Connect to No.50 pin.
52	NC	I	No connect pin. Connect to No.53 pin.
53	AIN5P	I	Analog Signal Input Pin
54	AIN5N	I	Analog Signal Input Pin
55	NC	I	No connect pin. Connect to No.54 pin.
56	VCOM	O	Internal Common Voltage Output Pin This pin should be connected to VSS via a 1.0μF (±10%) ceramic capacitor.
57	IREF	O	Analog Reference Current Output Pin This pin should be connected to VSS via a 6.8kΩ (±1%) resistor.
58	NC	I	No connect pin. Connect to No.59 pin.
59	AIN4P	I	Analog Signal Input Pin
60	AIN4N	I	Analog Signal Input Pin
61	NC	I	No connect pin. Connect to No.60 pin.
62	NC	I	No connect pin. Connect to No.63 pin.
63	AIN3P	I	Analog Signal Input Pin
64	AIN3N	I	Analog Signal Input Pin

7. Absolute Maximum Ratings

Item	Min.	Max.	Unit	Notes
Supply Voltage	−0.3	4.4	V	
Digital Input Pin Voltage	−0.3	4.4	V	CSN, CDTI, CCLK, RSTN pins
Input/Output Pin Voltage	−0.3	VDD+0.3 (≤4.4)	V	
Input Current (Iin)	−10	10	mA	Except Power Supply Pin
Storage Temperature	−65	150	°C	

- All voltages are with respect to ground at 0V (Reference Voltage).
- If digital output pins are connected to the data bus, the data bus operating voltage should be in the same range as shown above Input/Output Pin Voltage.
- Operation at or beyond these limits may result in permanent damage to the device.

8. Recommended Operating Conditions

Item	Min.	Typ.	Max.	Unit	Notes
Supply Voltage (VDD)	3.135	3.300	3.465	V	
Operating Temperature Range (Ta)	–40		125	°C	

- All voltages are with respect to ground at 0V (Reference Voltage).

9. Electrical characteristics

9.1. DC Characteristics

(Ta: −40°C to 125°C / VDD: 3.135 to 3.465V)

Item	Pin	Min.	Typ.	Max.	Unit	Condition
High Level Input Voltage (VIH)	CSN CCLK CDTI	0.7xVDD		3.465	V	
Low Level Input Voltage (VIL)		0		0.3xVDD	V	
Input Pull-up Current		−66	−33	−10	μA	0V Input
Input Leak Current		−10		+10	μA	VDD Input
High Level Output Voltage (VOH)	CDTO	VDD−0.5		VDD	V	IOH = −2mA
Low Level Output Voltage (VOL)		0		0.5	V	IOL = 2mA
Output Leak Current		−10		+10	μA	
High Level Reset Input Voltage	RSTN	0.7xVDD		3.465V	V	
Low Level Reset Input Voltage		0		0.3xVDD	V	
Reset Input Current		10	33	66	μA	VDD Input
Reset Input Leak Current		−10		+10	μA	0V Input
TEST Pin Pull-down Current	TEST	10	33	66	μA	

9.2. AC Timing

Ta: −40°C to 125°C / VDD: 3.135 to 3.465V

9.2.1. Reset input

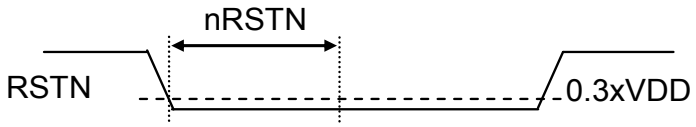


Figure 3

Item	Symbol	Min.	Typ.	Max.	Unit
Reset Filter	nRSTN	10		100	μs

Low input under 10μs will be rejected. A reset input does not synchronized with the CCLK.

9.2.2. Power up Sequence

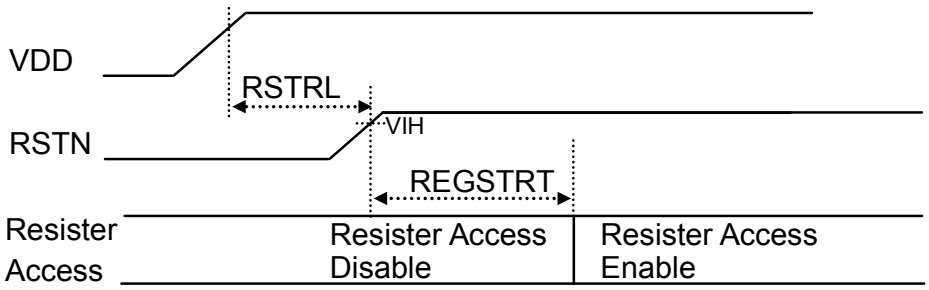


Figure 4

Item	Symbol	Min.	Typ.	Max.	Unit
RESET Release	RSTRL	100			μs
Register access start	REGSTRT	1			ms

9.2.3. Serial Communication Interface Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
CCLK period	T_{SCLK}	100			ns	
from CSN↓ to CCLK↓	T_{CSC}	16			ns	
from CCLK↓ to CSN↑	T_{ASC}	16			ns	
Clock high time	T_{SDC}	30			ns	
Clock low time	T_{SDC}	30			ns	
CDTI data input setup time	T_{SUI}	5			ns	
CDTI data input hold time	T_{HI}	11			ns	
CDTO data output delay time	T_{SUO}			24	ns	
CDTO data output hold time	T_{HO}	6			ns	
CSN negate time	T_{NEG}	$2xT_{SCLK}$			ns	
from CSN↑ to CDTO Hi-Z	T_{CCZ}			21	ns	

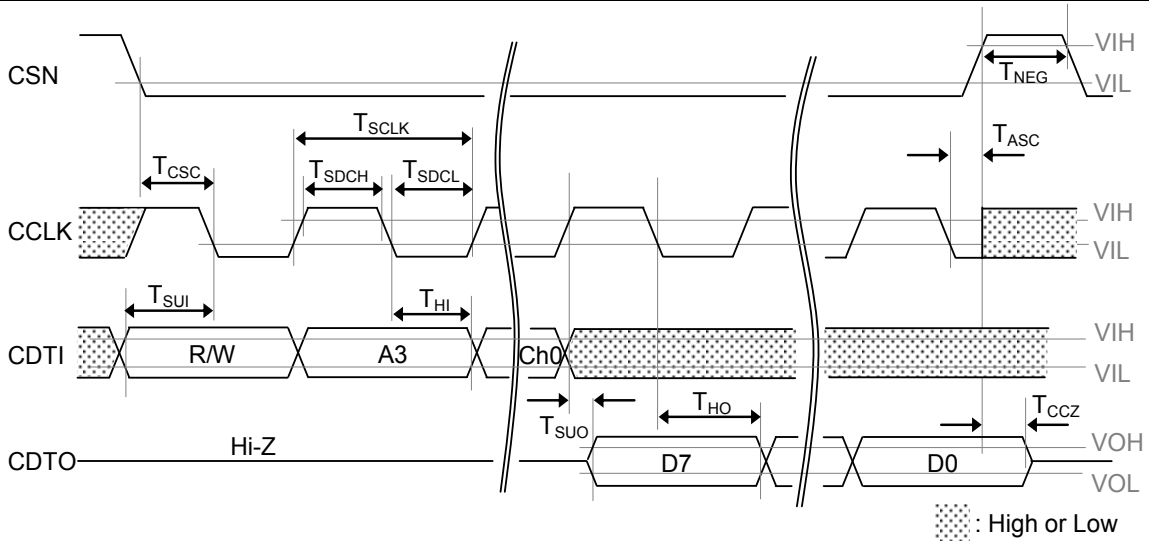


Figure 5

9.3. Analog Characteristics

Conditions:

Fin= 500Hz to 5MHz, HPF-Fc (3dB degraded frequency) = 25 kHz or Bypass, PGA1= 24dB, PGA2= 18dB, Fine gain= +5.625dB, VDD= 3.135 to 3.465V, Ta = −40 to 125ºC, the external load capacitance is less than 33pF, the external load resistance is more than 2kΩ via the external capacitor of AOUT pin, unless otherwise specified. Analog characteristics may degrade during SPI communication.

9.3.1. Analog Input Signal

Item	Min.	Typ.	Max.	Unit	Notes
Differential Input Voltage Amplitude			4.0	Vpp	0dB gain
Input Leak Current	−1		+1	μA	1MΩ or more, Differential Input Voltage: under 1.0Vpp

9.3.2. Analog Output Signal

Item	Min.	Typ.	Max.	Unit	Condition
Maximum Output Voltage	2.0			Vpp	The amplitude should satisfy the THD value.
Output Offset Voltage	−100		+100	mV	After offset calibration
THD (Distortion)		0.15	0.8	%	Differential Input Voltage: 1.0Vpp Differential Output Voltage: 2.0Vpp

9.3.3. Input Referred Noise Density

(PGA1=24dB, PGA2=0dB, Fine gain=0dB)

Item	Min.	Typ.	Max.	Unit	Condition	
Input Referred Noise density		−150	−146	dBm/Hz	Bypass mode	100kHz
		−150	−146			1MHz
		−150	−142	dBm/Hz	HPF mode (25kHz)	100kHz
		−150	−145			1MHz

9.3.4. Internal High Pass Filter

Item	Min.	Typ.	Max.	Unit	Condition
Minimum Cutoff Frequency		25		kHz	
Maximum Cutoff Frequency		1000		kHz	
Cutoff Frequency Accuracy	−47		+47	%	

9.3.5. Coarse Gain Control

Item	Min.	Typ.	Max.	Unit	Condition
0dB setting	−2	0	+2	dB	Fine gain: 0dB
6dB setting	4	6	8		
12dB setting	10	12	14		
18dB setting	16	18	20		
24dB setting	22	24	26		
30dB setting	28	30	32		
36dB setting	34	36	38		
42dB setting	40	42	44		

9.3.6. Fine Gain Control

Item	Min.	Typ.	Max.	Unit	Condition
Maximum gain	+5.225	+5.625	+6.025	dB	
Minimum gain	−6.4	−6	−5.6	dB	
Gain step	0.1	0.375	0.6	dB	

9.3.7. Reference Voltage

Item	Min.	Typ.	Max.	Unit	Condition
Output Voltage (VCOM)	1.19	1.25	1.31	V	

9.3.8. Detection Function

Item	Min.	Typ.	Max.	Unit	Condition
VCOM Pin Over Voltage Detection	1.35		1.55	V	
VCOM Pin Low Voltage Detection	0.95		1.15	V	
IREF Pin Over Current Detection	170		430	μA	
IREF Pin Low Current Detection	50		130	μA	

9.3.9. Current Consumption

(PGA1=6dB, PGA2=0dB, Fine gain=0dB)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Normal Operation	IDD			300	mA	HPF Mode
				270	mA	Bypass Mode
Sleep Mode	SLIDD			30	mA	
Channel Off Setting	COIDD			10	mA	
During Reset	SIDD			100	μA	

9.3.10. Channel to channel mismatch

Condition: HPF-Fc(−3dB)=25kHz

Item	Mode	Min.	Typ.	Max.	Unit	Condition
Gain	Bypass Mode			1	dB	5MHz
	HPF Mode			1		5MHz
Phase	Bypass Mode			2	deg.	1MHz
			4	8		5MHz
	Bypass Mode			2		1MHz
			5	9		5MHz

9.3.11. Others

Item	Min.	Typ.	Max.	Unit	Condition
In-band Ripple Mode (Bypass Mode)		0.1	0.5	dB	500Hz to 500kHz
		2.0	3.0		5MHz
Channel Separation (Isolation)	52	60		dB	500Hz
	52	60			5MHz
PSRR	10			dB	PGA1=24dB,PGA2=18dB, Fine gain=+5.625dB,100kHz
	10			dB	PGA1=24dB,PGA2=18dB, Fine gain=+5.625dB, 500kHz

10. Functional Descriptions

10.1. Analog input

There are 8 channels for analog input signal and they support differential inputs. The path using internal HPF filter and the path not using the internal HPF can be chosen externally.

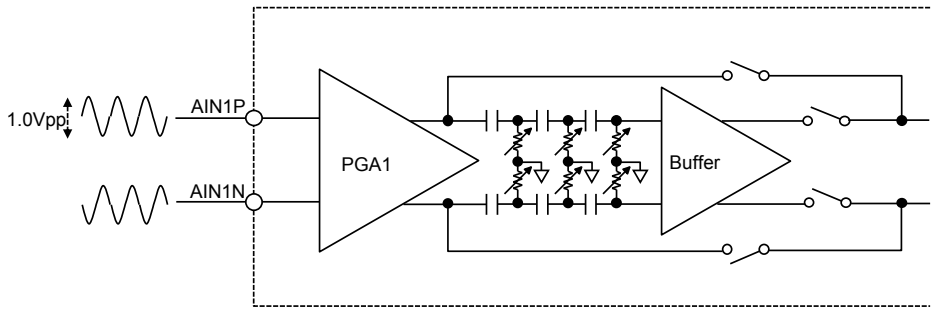


Figure 6

AFEPD [8:1] bits control the ON/OFF of the signal processing for each channel. Input pins of unused channel should be connected to VSS.

10.2. Internal High Pass Filter

The AK5806 integrates 3rd-order high pass filter and the filter characteristics can be changed by changing internal resistance. The HPF setting range is from 25 kHz to 1 MHz as attenuating the output amplitude frequency for 3dB when the input frequency is 5 MHz. (HPFC [2:0] bits)

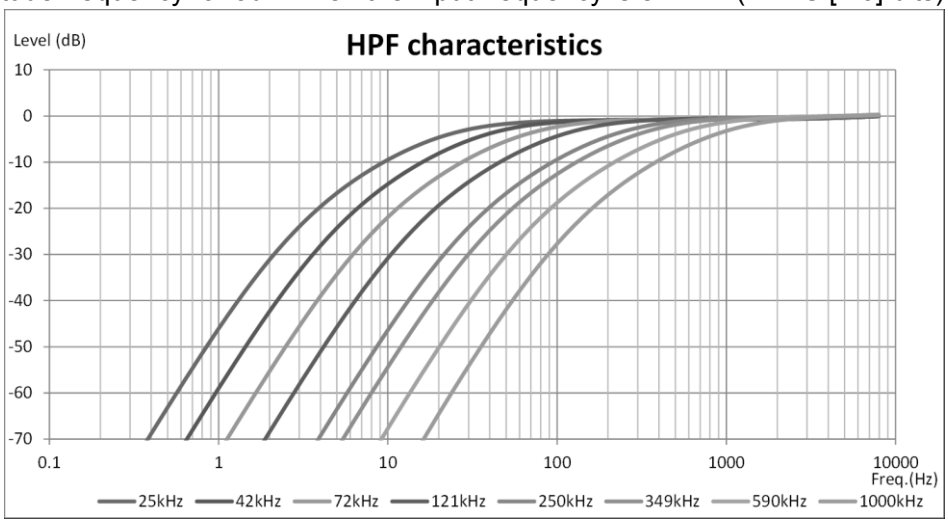


Figure 7

10.3. Coarse Gain Control

The AK5806 integrates two amplifiers that are capable of adjusting the gain in about 6dB steps for each channel. (PGA1, PGA2)

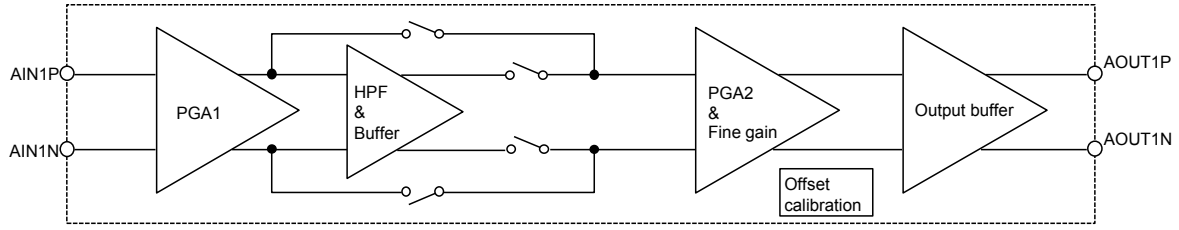


Figure 8

- PGA1: 0dB to 24dB (PGA1G[2:0] register)
- PGA2: 0dB to 18dB (PGA2G[1:0] register)

10.4. Fine Gain Control

The AK5806 integrates a gain amplifier that is capable of monotonic increase by about 0.375dB steps.

10.5. Reference Voltage

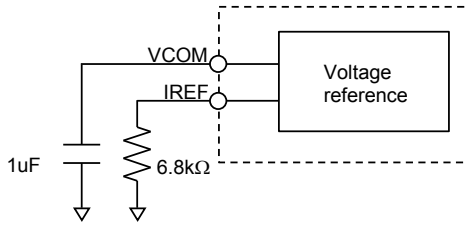


Figure 9

The AK5806 generates reference voltage for analog circuits from the internal band gap voltage.

10.6. Power Management

AK5806 has the two kind of power save mode as follows.

- Sleep Mode：PGA1, PGA2 and HPF are power downed.
- Signal Processing off Mode: PGA1, PGA2, HPF and Output buffer are power downed.

10.7. Offset Cancellation

The AK5806 has an offset cancellation circuit to correct the output offset voltage. Input path for external signals will be OFF when the offset cancelling is started by register setting. Offset cancellation value changes as the output offset will be in the range of ±100mV while internal offset compensation value is kept by registers. Registers for offset cancellation are shown below.

- ENDOFCAL-bit: Offset Cancellation Operation Status Register
- EROF [8:1]-bit: Offset Cancellation Result Status Register; It shows whether the offset cancelling result is in the correction range or not.
- OFCAL-bit: Offset Cancellation Start Setting Register
- OFCAL_E-bit: Offset Cancellation Function Enable Register; It shows whether the offset cancelling result is included in the output signal or not.

Offset cancellation sequence is shown below.

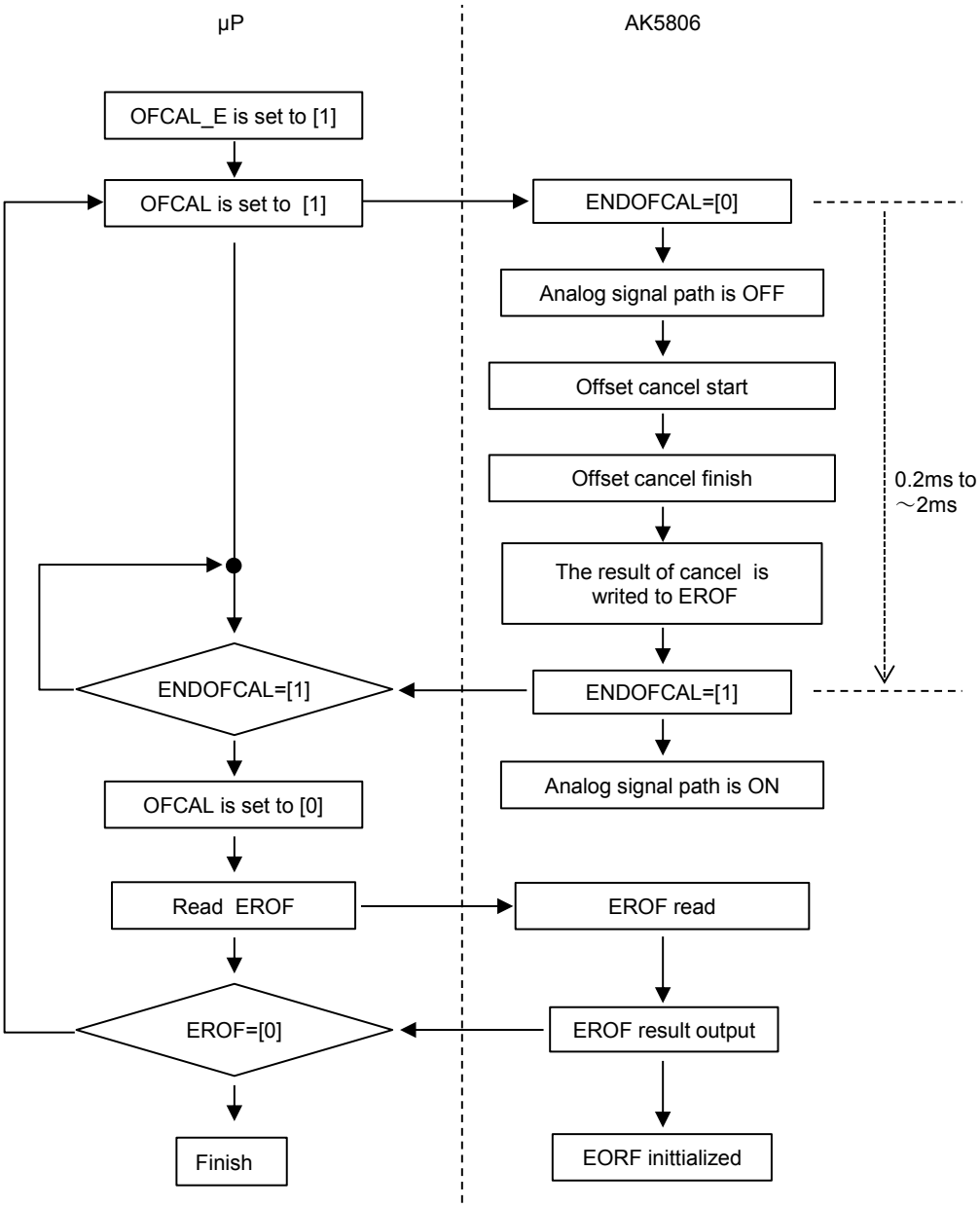


Figure 10

10.8. Serial Communication Interface (SPI)

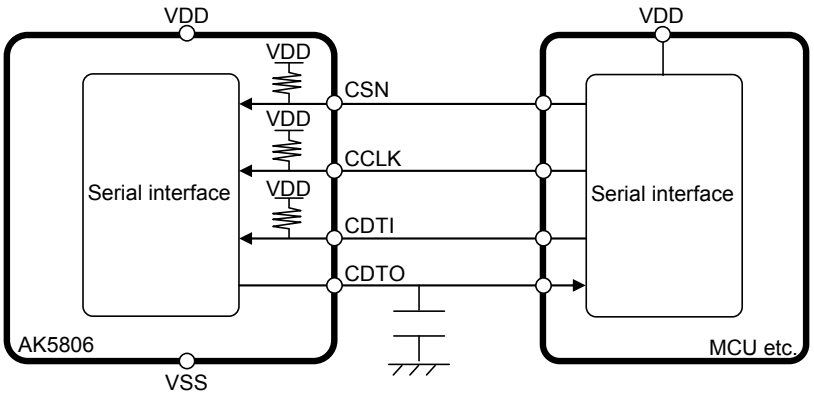


Figure 11

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R/W	Address[5:0]						D [7:0]								P
		MSB					LSB	MSB							LSB	

- R/W bit: ”[0]:Write”, “[1]:Read” - Address bit: Register address bit
- D bit: Register data bit

The D0 bit is assigned for parity check (EVEN Parity).

Example:

Parity Data = "0" when {Address [5:0], D [7:0]} = {00000000000000}

Parity Data = "1" when {Address [5:0], D [7:0]} = {10000000000000}

10.8.1. Write format

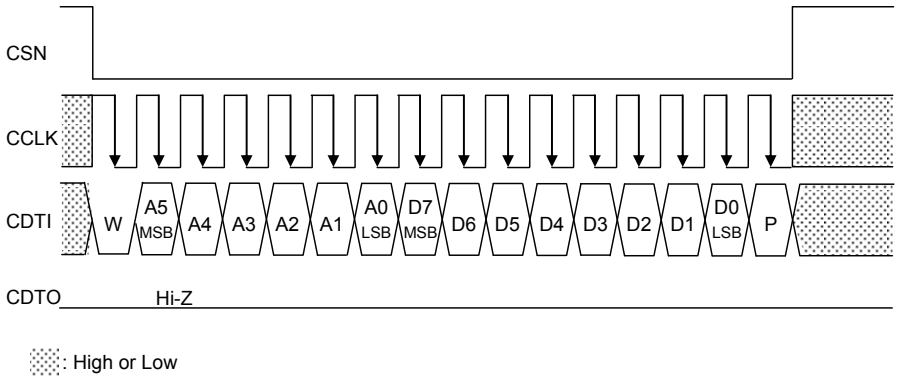


Figure 12

10.8.2. Read Format

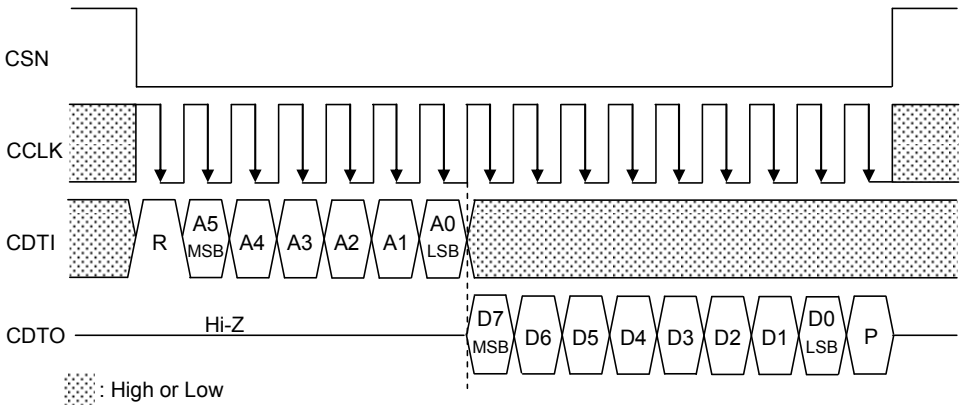


Figure 13

11. Register

11.1. Register Map

Address [5:0]	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	R/W	Default Value
0x00	CPID[3:0]				VER[3:0]				R	0x61
0x01	Reserved			ERVCOM	ERSPI	Reserved		ERIREF	R	0x80
0x02	Reserved							ENDOFCAL	R	0x01
0x03	EROF[8:1]								R	0x00
0x04	Reserved								R/W	0x00
0x05	Reserved						OFCAL_E	OFCAL	R/W	0x00
0x06	Reserved							SLP	R/W	0x00
0x07	AFEPD[8:1]								R/W	0x00
0x08	Reserved			PGA2G[1:0]		PGA1G[2:0]			R/W	0x00
0x09	Reserved			FG1C[4:0]					R/W	0x10
0x0A	Reserved			FG2C[4:0]					R/W	0x10
0x0B	Reserved			FG3C[4:0]					R/W	0x10
0x0C	Reserved			FG4C[4:0]					R/W	0x10
0x0D	Reserved			FG5C[4:0]					R/W	0x10
0x0E	Reserved			FG6C[4:0]					R/W	0x10
0x0F	Reserved			FG7C[4:0]					R/W	0x10
0x10	Reserved			FG8C[4:0]					R/W	0x10
0x11	Reserved			PE	HPF_E	HPFC[2:0]			R/W	0x00
0x12 - 0x1F	Reserved								R/W	0x00

Register write is not available on “Reserved” bits.

11.2. Register Definitions

Sub Address 0x00

D[7:0]	Name	Definition	Notes
[3:0]	VER[3:0]	Chip Version ID	4’b0001 (Read only)
[7:4]	CHIPID[3:0]	Chip Information ID	4’b0110 (Read only)

Sub Address 0x01

D[7:0]	Name	Definition	Notes
[0]	ERIREF	IREF pin Abnormal Current Monitoring Register 0: Normal Status, 1: IREF pin Over Current Status*	(Read only)
[2:1]	Reserved	Reserved	
[3]	ERSPI	SPI communication Error Monitoring Register (Clock Count result or parity check result when CSN input mode) 0: No SPI Communication Error, 1: SPI Communication Error	(Read only)
[4]	ERVCOM	VCOM pin Abnormal Voltage Monitoring Register 0: Normal Status, 1: Abnormal Voltage Status*	(Read only)
[7:5]	Reserved	Reserved	

*All blocks except SPI communication block are powered down. Their states are cleared by the RSTN pin.

Sub Address 0x02

D[7:0]	Name	Definition	Notes
[0]	ENDOFCAL	Offset Cancellation Operation Status Register 0: During Calibration , 1: Calibration Finished	(Read only)
[7:1]	Reserved	Reserved	

Sub Address 0x03

D[7:0]	Name	Definition	Notes
[7:0]	EROF[8:1]	Offset Cancellation Result Status Register 0: No error (Default) , 1: Error	EROF1: Channel: 1 ~ EROF8:Channel 8 (Read only)

Sub Address 0x04

D[7:0]	Name	Definition	Notes
[7:0]	Reserved	Reserved	

Sub Address 0x05

D[7:0]	Name	Definition	Notes
[0]	OFCAL	Offset Cancellation Start Setting Register 0: Cancellation Stop 1: Cancellation Start	Offset cancellation function is disabled when OFCAL_E-bit= “0”.
[1]	OFCAL_E	Offset Cancellation Function Enable Register 0: Cancellation Disable 1: Cancellation Enable	
[7:2]	Reserved	Reserved	

Sub Address 0x06

D[7:0]	Name	Definition	Notes
[0]	SLP	Sleep Mode Setting Register (All Channels) 0: Normal Operation 1: Sleep Mode	
[7:1]	Reserved	Reserved	

Sub Address 0x07

D[7:0]	Name	Definition	Notes
[0]	AFEPD 1	Signal Process Circuit Stop Register 0: Circuit is in operation (Default) 1: Circuit is stopped	Channel 1
[1]	AFEPD 2		Channel 2
[2]	AFEPD 3		Channel 3
[3]	AFEPD 4		Channel 4
[4]	AFEPD 5		Channel 5
[5]	AFEPD 6		Channel 6
[6]	AFEPD 7		Channel 7
[7]	AFEPD 8		Channel 8

Sub Address 0x08

D[7:0]	Name	Definition	Notes
[2:0]	PGA1G[2:0]	PGA1 gain (All channels) 000: 0dB (Default), 001: 6dB 010: 12dB, 011: 18dB, 1XX: 24dB	
[4:3]	PGA2G[1:0]	PGA2 gain (All channels) 00: 0dB (Default), 01: 6dB 10: 12dB, 11: 18dB	
[7:5]	Reserved	Reserved	

Sub Address 0x09 – Sub Address 0x10

D[7:0]	Name	Definition	Notes
[4:0]	FG1C [4:0] (Sub address 0x09, channel 1) FG2C [4:0] (Sub address 0x0A, channel 2) FG3C [4:0] (Sub address 0x0B, channel 3) FG4C [4:0] (Sub address 0x0C, channel 4) FG5C [4:0] (Sub address 0x0D, channel 5) FG6C [4:0] (Sub address 0x0E, channel 6) FG7C [4:0] (Sub address 0x0F, channel 7) FG8C [4:0] (Sub address 0x10, channel 8)	Fine Gain Control 00000: −6dB | 10000: 0dB (Default) | 11111: +5.625dB (Typical: 0.375dB/LSB)	
[7:5]	Reserved	Reserved	

Sub Address 0x11

D[7:0]	Name	Definition	Notes
[2:0]	HPFC [2:0]	HPF Characteristics Control (All Channels) 000:25kHz, 001:42kHz 010:72kHz, 011:121kHz 100:250kHz, 101:349kHz 110:590kHz, 111:1000kHz	
[3]	HPF_E	Internal HPF Enable HPF (All Channels) 0: Bypass Mode (Default) 1: HPF Mode	
[4]	PE	Parity Bit Detection Setting 0: Detection Disable (Default) 1: Detection Enable	(Detection Disable) Register Write: Ignore Parity Bit Register Read: Add Parity Bit (Detection Enable): Register Write: Execute Parity Bit Error Detection* Register Read: Add Parity Bit *When a parity error is detected, register writing is ignored and the error status is shown in ERSPI bit.
[7:5]	Reserved	Reserved	

12. Example of External Connection Diagram

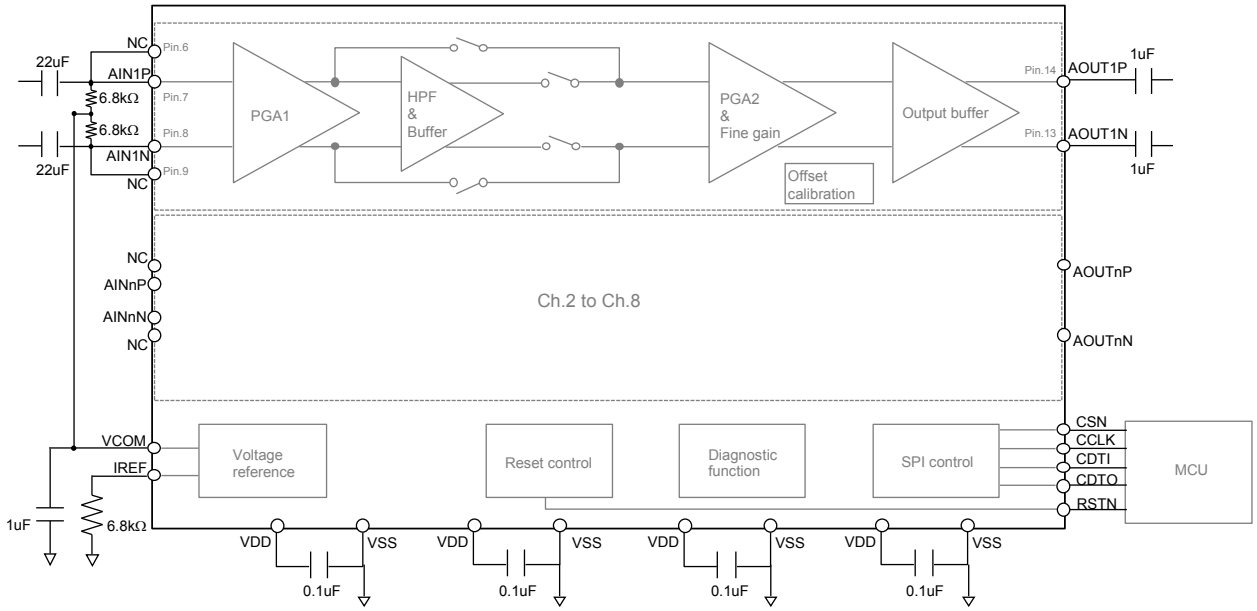


Figure 14

13. Package

13.1. Outline Dimensions

64pin-HTQFP package, Pin pitch: 0.5mm

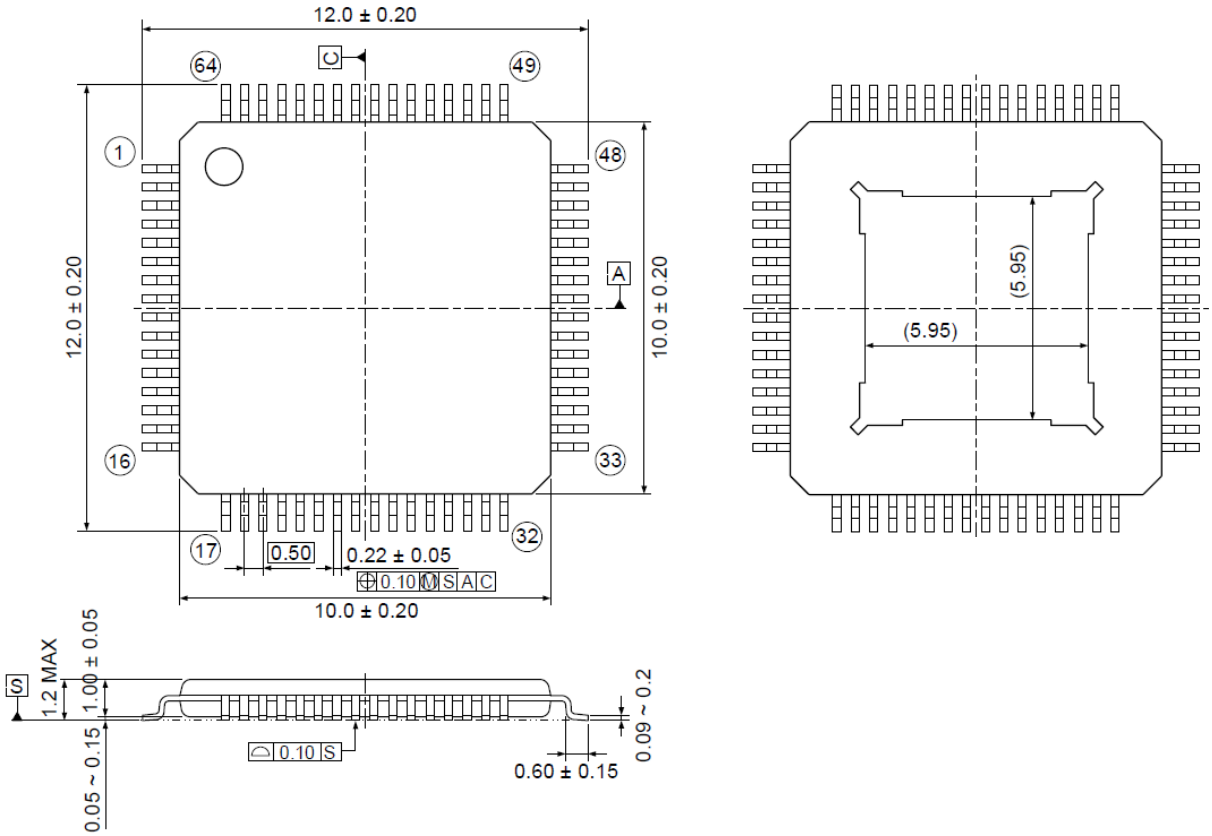


Figure 15

13.2. Foot Pattern

This figure is an example. It should be designed to be appropriate design for each PCB board.

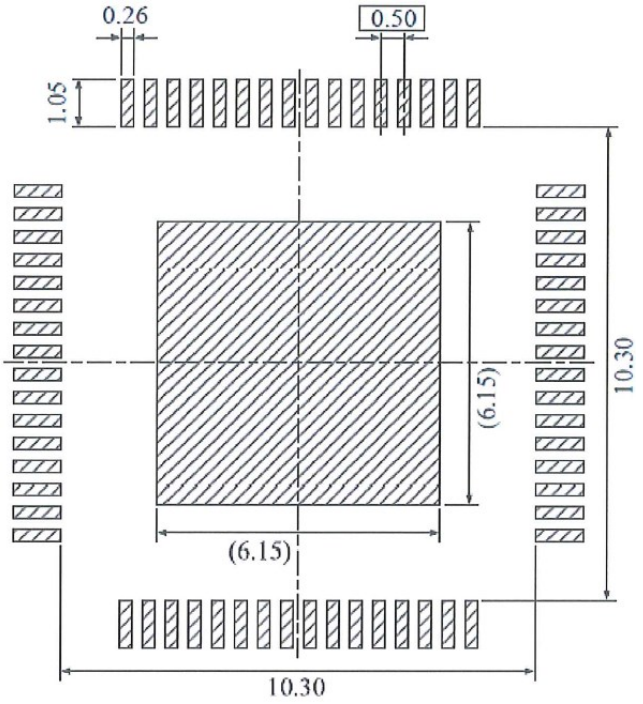


Figure 16

13.3. Marking

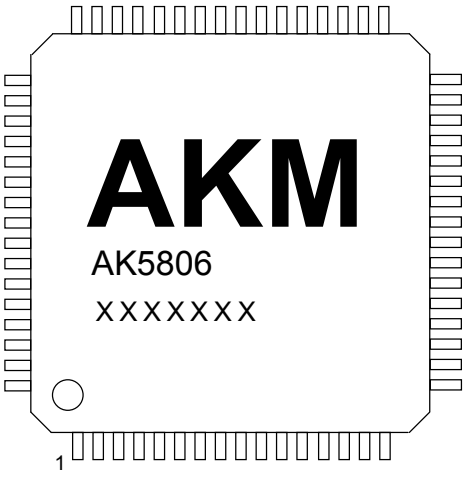


Figure 17

Logo: AKM
Marketing code: AK5806
Date code: XXXXXXX

14. Ordering Guide

AK5806	−40ºC to 125 ºC	64pin HTQFP

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