AK4950

24bit Stereo CODEC with MIC/SPK/Cap-less VIDEO-AMP & mini DSP

GENERAL DESCRIPTION

The AK4950 is a 24bit stereo CODEC with a microphone, speaker and headphone amplifiers. The input circuits include a microphone amplifier and the output circuits include a speaker amplifier. It is suitable for portable application with recording/playback function. The integrated charge pump generates an internal negative power supply rail and removes the output coupling capacitor. A one channel composite In/Out video amplifier is also integrated. Digital sound processing is provided by the internal DSP. The AK4950 is available in a small 32pin QFN (4mm x 4mm, 0.4mm pitch), saving more board space.

FEATURES

1. Recording Functions
- **Stereo Single-ended input with two Selectors**
- **MIC Amplifier (+24dB/+21dB/+18dB/+16dB/+14dB/+11dB/+8dB/+5dB/0dB)**
- **Digital ALC (Automatic Level Control)**
  (Setting Range: +35.625dB ~ –54dB, 0.375dB Step)
- **ADC Performance: S/(N+D): 83dB, DR, S/N: 88dB (MIC-Amp=+18dB)**
  S/(N+D): 85dB, DR, S/N: 96dB (MIC-Amp=0dB)
- **MIC Sensitivity Compensation**
- **Wind-noise Reduction Filter**
- **4 Band Notch Filter**
- **Stereo Separation Emphasis Circuit**
- **Digital MIC Interface**

2. Playback Functions
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**
- **Digital ALC (Automatic Level Control)**
  (Setting Range: +35.625dB ~ –54dB, 0.375dB Step)
- **Digital Volume Control (+12dB ~ –78dB, 0.375dB Step)**
- **Stereo Separation Emphasis Circuit**
- **Stereo Line Output**
  - S/(N+D): 83dB, S/N: 92dB
- **Mono Mixing Output**
- **Mono Speaker-Amplifier**
  - SPK-Amp Performance: S/(N+D): 75dB@150mW, 70dB@250mW,
  S/N: 95dB
  - Thermal Shut-down
  - BTL Output
  - Output Power: 400mW@8Ω (SVDD=3.3V)
- **Analog Mixing: Mono Input**

3. Power Management

4. Master Clock:

(1) PLL Mode
- **Frequencies: 11.2896MHz, 12MHz, 13.5MHz, 24MHz, 25MHz, 27MHz (MCKI pin)**
  32fs or 64fs (BICK pin)

(2) External Clock Mode
- **Frequencies: 512fs or 1024fs (MCKI pin)**

5. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs
- **PLL Slave Mode (BICK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (MCKI pin):**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **PLL Master Mode:**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **EXT Master/Slave Mode:**
  7.35kHz ~ 48kHz (512fs), 7.35kHz ~ 13kHz (1024fs)

6. μP I/F: 3-wire Mode, I^2C Bus (Ver 1.0, 400kHz Fast-Mode)

7. Master/Slave mode

8. Audio Interface Format: MSB First, 2's complement
- **ADC: 24bit MSB justified, 16/24bit I^2S**
- **DAC: 24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 16/24bit I^2S**

9. Video Functions
- **One Composite Signal Input**
- **Capacitor-less Video Amplifier for Composite Signal Output**
  Gain: +6 / +9 / +12 / +16.5dB
- **LPF**
- **Charge Pump Circuit for Negative Power Supply**

10. Ta = –30 ~ 85°C

11. Power Supply:
- **Analog Power Supply (AVDD): 2.7 ~ 3.6V**
- **Digital I/O Power Supply (TVDD): 1.6 ~ 3.6V**

12. Package: 32pin QFN (4 x 4mm, 0.4mm pitch)

■ Block Diagram

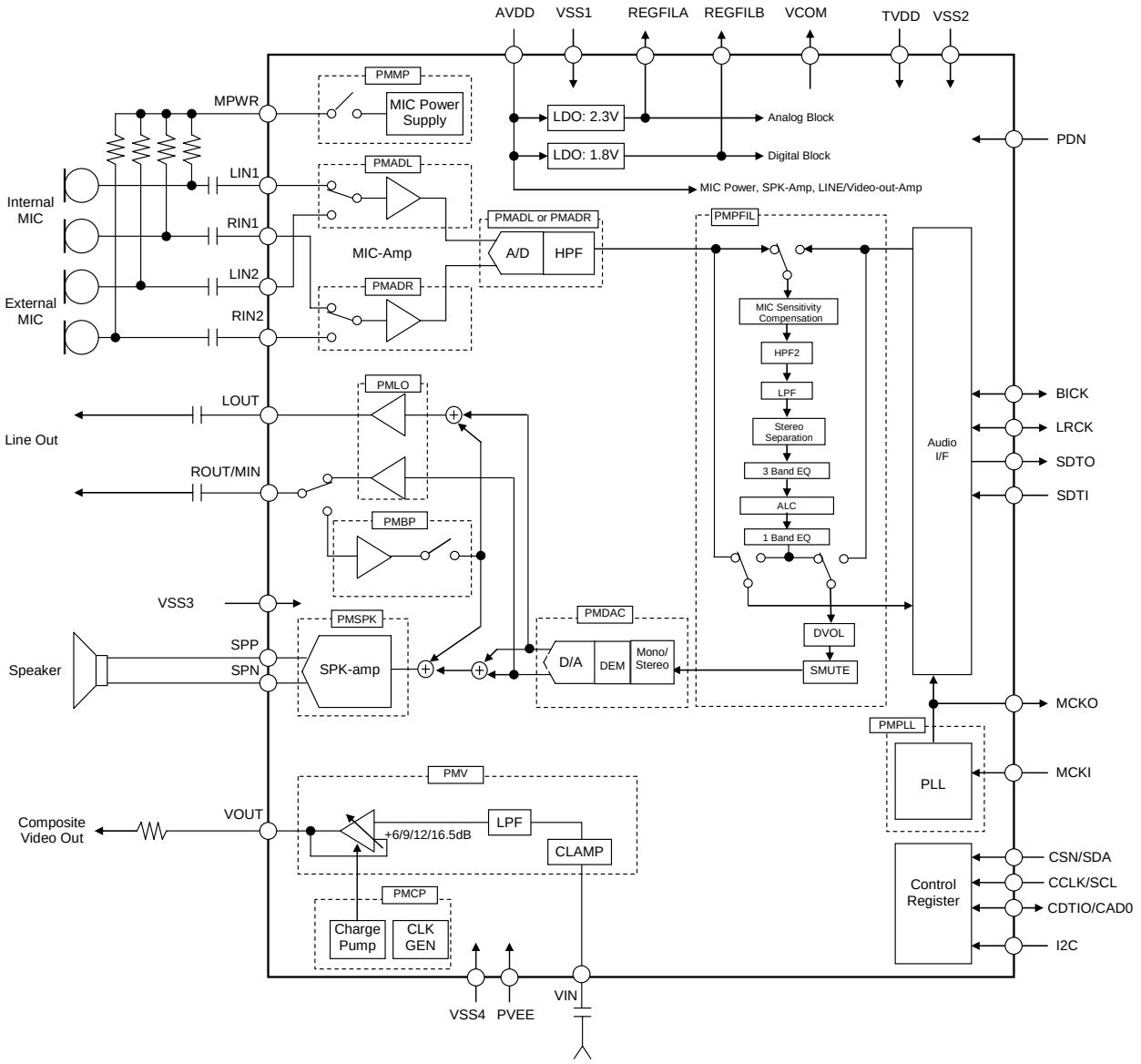


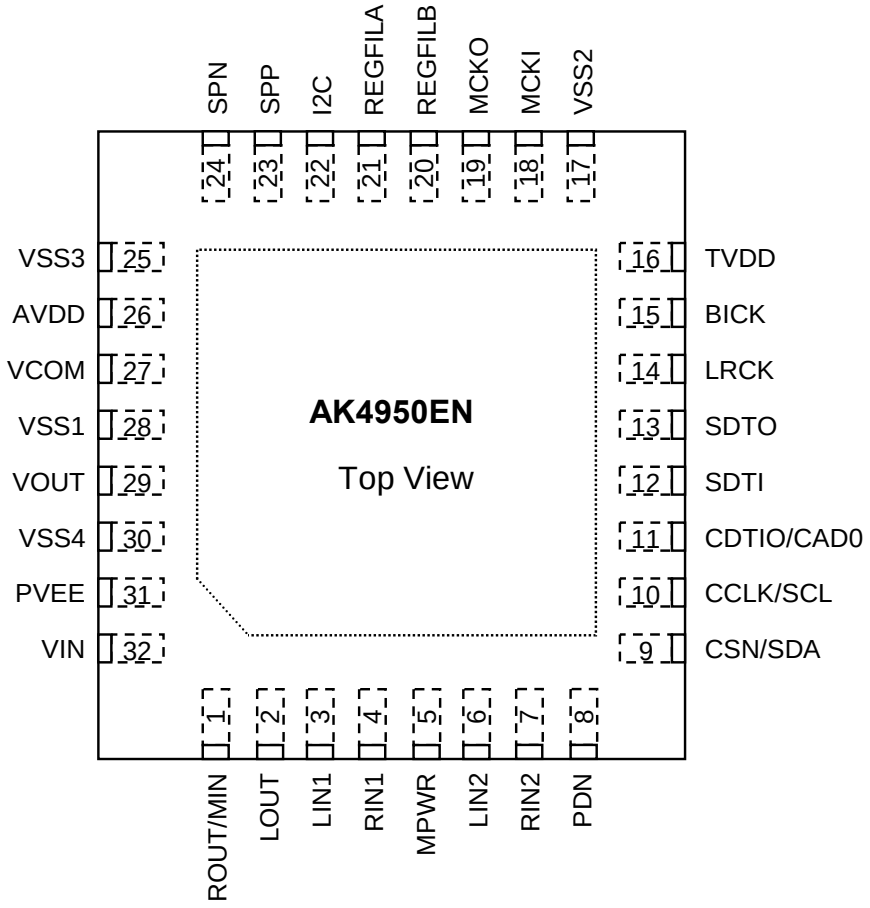
Figure 1. Block Diagram

Total: 32pin

■ Ordering Guide

AK4950EN	–30 ~ +85°C	32pin QFN (0.4mm pitch)
AKD4950	Evaluation board for AK4950	

■ Pin Layout



PIN/FUNCTION

No	Pin Name	I/O	Function
1	ROUT	O	Rch Analog Output Pin (PMBP bit = "0")
	MIN	I	Mono Analog Signal Input Pin (PMBP bit = "1")
2	LOUT	O	Lch Analog Output Pin
3	LIN1	I	Lch Analog Input Line Input 1Pin (DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
4	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0")
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")
5	MPWR	O	MIC Power Supply Pin for Microphone
6	LIN2	I	Lch Analog Input 2 pin
7	RIN2	I	Rch Analog Input 2 Pin
8	PDN	I	Power-down & Reset When "L", the AK4950 is in power-down mode and is held in reset. The AK4950 must be always reset upon power-up.
9	CSN	I	Chip Select Pin (I2C pin = "L")
	SDA	I/O	Control Data Input/Output Pin (I2C pin = "H")
10	CCLK	I	Control Data Clock Pin (I2C pin = "L")
	SCL	I	Control Data Clock Pin (I2C pin = "H")
11	CDTIO	I/O	Control Data Input/Output Pin (I2C pin = "L")
	CAD0	I	Chip Address Select Pin (I2C pin = "H")
12	SDTI	I	Audio Serial Data Input Pin
13	SDTO	O	Audio Serial Data Output Pin
14	LRCK	I/O	Input/Output Channel Clock Pin
15	BICK	I/O	Audio Serial Data Clock Pin
16	TVDD	-	Digital I/F Power Supply Pin
17	VSS2	-	Ground 2 Pin
18	MCKI	I	External Master Clock Input Pin
19	MCKO	O	Master Clock Output Pin
20	REGFILB	O	LDO Voltage Output pin for Digital Logic (typ 1.8V) This pin must be connected to the VSS1 pin with a 1.0μF capacitor (±50% including tolerance and temperature allowance) in series.
21	REGFILA	O	LDO Voltage Output pin for Analog Logic (typ 2.3V) This pin must be connected to the VSS1 pin with a 2.2μF capacitor (±50% including tolerance and temperature allowance) in series.
22	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire mode The input circuit of the I2C pin is operated by AVDD.
23	SPP	O	Speaker Amp Positive Output Pin
24	SPN	O	Speaker Amp Negative Output Pin
25	VSS3	-	Ground 3 Pin
26	AVDD	-	Analog Power Supply Pin This pin must be connected to VSS4 with a 0.1μF ceramic capacitor in series.
27	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs.
28	VSS1	-	Ground 1 Pin
29	VOUT	O	Composite Video Output Pin
30	VSS4	-	Ground 4 Pin
31	PVEE	O	Negative Voltage Output Pin for Video Output This pin must be connected to VSS4 with a 2.2μF ceramic capacitor in series.
32	VIN	I	Composite Video Input Pin

Note 1. All input pins except analog input pins (MIN, LIN1, RIN1, LIN2, RIN2, VIN) must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, SPN, SPP, ROUT/MIN, LOUT, RIN2, LIN2, LIN1/DMDAT, RIN1/DMCLK, VIN, VOUT	These pins must be open.
Digital	MCKO	This pin must be open.
	MCKI	This pin must be connected to VSS2.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4=0V; Note 2)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital I/O	TVDD	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 4)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 5)		VIND	–0.3	TVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 6)		Pd1	-	450	mW

Note 2. All voltages are with respect to ground.
Note 3. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog ground plane.
Note 4. MIN, LIN1, RIN1, LIN2, RIN2, VIN, I2C pins
Note 5. PDN, CSN, CCLK, CDTIO, SDTI, LRCK, BICK, MCKI pins
Note 6. In case that PCB wiring density is over 200% and its surface wiring density is over 50%. This power is the AK4950 internal dissipation that does not include power dissipation of externally connected speakers.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=0V; Note 2)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 7)	Analog	AVDD	2.7	3.3	3.6	V
	Digital I/O	TVDD	1.6	1.8	3.6	V

Note 2. All voltages are with respect to ground.
Note 7. The power-up sequence between AVDD and TVDD is not critical. The PDN pin must be “L” upon power up, and should be changed to “H” after all power supplies are supplied to avoid an internal circuit error.

*** When TVDD is powered ON and the PDN pin is “L”, AVDD can be powered ON/OFF. When the AK4950 is powered ON from power-down state, the PDN pin must be “H” after all power supplies are ON.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=3.3V, TVDD= 1.8V; VSS1=VSS2=VSS3=VSS4=0V; fs=44.1kHz, BICK=64fs;
Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Unit
MIC Amplifier: LIN1, RIN1, LIN2, RIN2 pins						
Input Resistance			23	33	43	kΩ
Gain	MGAIN3-0 bits = "0000"		-1	0	+1	dB
	MGAIN3-0 bits = "0001"		+4	+5	+6	dB
	MGAIN3-0 bits = "0010"		+7	+8	+9	dB
	MGAIN3-0 bits = "0011"		+10	+11	+12	dB
	MGAIN3-0 bits = "0100"		+13	+14	+15	dB
	MGAIN3-0 bits = "0101"		+15	+16	+17	dB
	MGAIN3-0 bits = "0110"		+17	+18	+19	dB
	MGAIN3-0 bits = "0111"		+20	+21	+22	dB
	MGAIN3-0 bits = "1000"		+23	+24	+25	dB
MIC Power Supply: MPWR pin						
Output Voltage (Note 8)		MICL bit = "0"	2.3	2.5	2.7	V
		MICL bit = "1"	2.0	2.2	2.4	V
Output Noise Level (A-weighted)			-	–108	-	dBV
Load Resistance			0.5	-	-	kΩ
Load Capacitance			-	-	30	pF
PSRR (fin =1kHz)			-	100	-	dB
ADC Analog Input Characteristics **:** LIN1/RIN1/LIN2/RIN2 pins → ADC → IVOL, IVOL=0dB, ALC=OFF						
Resolution/			-	-	24	Bits
Input Voltage (Note 9)		(Note 10)	-	0.261	-	Vpp
		(Note 11)	1.86	2.07	2.28	Vpp
S/(N+D)	(–1dBFS)	(Note 10)	73	83	-	dBFS
		(Note 11)	-	85	-	dBFS
D-Range	(–60dBFS, A-weighted)	(Note 10)	78	88	-	dB
		(Note 11)	-	96	-	dB
S/N	(A-weighted)	(Note 10)	78	88	-	dB
		(Note 11)	-	96	-	dB
Interchannel Isolation		(Note 10)	75	90	-	dB
		(Note 11)	-	100	-	dB
Interchannel Gain Mismatch		(Note 10)	-	0	0.5	dB
		(Note 11)	-	0	0.5	dB

Note 8. AVDD should be in the range of 2.7 ~ 3.6V when MICL bit is "1". It should be in the range of 3.0~3.6V when MICL bit is "0".
Note 9. Vin = 0.9 x 2.3Vpp (typ) @MGAIN3-0 bits = "0000" (0dB)
Note 10. MGAIN3-0 bits = "0110" (+18dB)
Note 11. MGAIN3-0 bits = "0000" (0dB)

Parameter		min	typ	max	Unit
DAC Characteristics:					
Resolution		-	-	24	Bits
Stereo Line Output Characteristics: DAC → LOUT, ROUT pins, ALC=OFF, DVOL=OVOL =0dB, LOVL1-0 bit = "01", R_L=10kΩ, PMBP bit= "0"					
Output Voltage (Note 12)	LOVL0 bit = "1"	2.27	2.52	2.77	Vpp
	LOVL0 bit = "0"	1.94	2.16	2.38	Vpp
S/(N+D) (–3dBFS)		73	83	-	dBFS
S/N (A-weighted)		82	92	-	dB
Interchannel Isolation		85	100	-	dB
Interchannel Gain Mismatch		-	-	0.8	dB
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	30	pF
PSRR (fin =1kHz)		-	80	-	dB
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, DVOL=OVOL =0dB, R_L=8Ω, BTL					
Output Voltage					
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)		3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)		-	1.79	-	Vrms
S/(N+D)					
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	75	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)		20	70	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)		-	65	-	dB
S/N SPKG1-0 bits = "01", –0.5dBFS(Po=250mW) (A-weighted)		85	95	-	dB
Load Resistance		6.8	-	-	Ω
Load Capacitance		-	-	30	pF
PSRR (fin =1kHz)		-	60	-	dB

Note 12. AVDD should be in the range of 3.0~3.6V when LOVL0 bit is "1". It should be in the range of 2.7~3.6V when LOVL0 bit is "0".

Parameter			min	typ	max	Unit
Mono Input: MIN pin, External Resistance mode (PMBP bit =“1”, BPM bit = “1”, BPVCM bit = “0”, BPLVL2-0 bits = “000”), External Input Resistance= 66kΩ						
Maximum Input Voltage (Note 13)			-	1.54	-	Vpp
Gain (Note 14)						
	MIN → LOUT	LOVL1-0 bit = “00”	–4.5	0	+4.5	dB
		LOVL1-0 bit = “01”	-	+1.34	-	dB
		LOVL1-0 bit = “10”	-	+2	-	dB
		LOVL1-0 bit = “11”	-	+3.34	-	dB
	MIN → SPP/SPN					
		ALC bit = “0”, SPKG1-0 bits = “00”	+1.6	+6.1	+10.6	dB
		ALC bit = “0”, SPKG1-0 bits = “01”	-	+8.1	-	dB
		ALC bit = “0”, SPKG1-0 bits = “10”	-	+10.1	-	dB
		ALC bit = “0”, SPKG1-0 bits = “11”	-	+12.1	-	dB
		ALC bit = “1”, SPKG1-0 bits = “00”	-	+8.1	-	dB
		ALC bit = “1”, SPKG1-0 bits = “01”	-	+10.1	-	dB
		ALC bit = “1”, SPKG1-0 bits = “10”	-	+12.1	-	dB
		ALC bit = “1”, SPKG1-0 bits = “11”	-	+14.1	-	dB
Mono Input: MIN pin, Internal Resistance Mode (PMBP bit =“1”, BPM bit = “0” , BPVCM bit = “0”, BPLVL2-0 bits = “000”)						
Input Resistance			56	66	76	kΩ
Maximum Input Voltage (Note 13)			-	1.54	-	Vpp
Gain						
	MIN → LOUT	LOVL1-0 bit = “00”	-1	0	+1	dB
		LOVL1-0 bit = “01”	-	+1.34	-	dB
		LOVL1-0 bit = “10”	-	+2	-	dB
		LOVL1-0 bit = “11”	-	+3.34	-	dB
	MIN → SPP/SPN					
		ALC bit = “0”, SPKG1-0 bits = “00”	+4.1	+6.1	+8.1	dB
		ALC bit = “0”, SPKG1-0 bits = “01”	-	+8.1	-	dB
		ALC bit = “0”, SPKG1-0 bits = “10”	-	+10.1	-	dB
		ALC bit = “0”, SPKG1-0 bits = “11”	-	+12.1	-	dB
		ALC bit = “1”, SPKG1-0 bits = “00”	-	+8.1	-	dB
		ALC bit = “1”, SPKG1-0 bits = “01”	-	+10.1	-	dB
		ALC bit = “1”, SPKG1-0 bits = “10”	-	+12.1	-	dB
		ALC bit = “1”, SPKG1-0 bits = “11”	-	+14.1	-	dB

Note 13. The maximum value is AVDD Vpp when BPVCM bit = “1”. However, it must be set that the output level of MIN-Amp is less than 0.1Vpp by setting BPLVL2-0 bits.

Note 14. The gain is in inverse proportion to external input resistance.

Parameter		min	typ	max	Unit
Video Signal Input					
External Resistor (Note 16)	R1 (Figure 2)	-	-	600	Ω
External Capacitor	C1 (Figure 2)	0.05	0.1	0.2	μF
Maximum Input Voltage: VG1-0 bits = "00" (+6dB)		-	1.0	1.24	Vpp
Pull Down Current		-	0.4	-	μA
Video Analog Output (Figure 3)					
Output Gain fin=100kHz Sine wave Input (Note 15)	VG1-0 bits = "00", 1.0Vpp Input	5.5	6.0	6.5	dB
	VG1-0 bits = "01", 0.7Vpp Input	8.5	9.0	9.5	
	VG1-0 bits = "10", 0.5Vpp Input	11.5	12.0	12.5	
	VG1-0 bits = "11",0.3Vpp Input	16	16.5	17	
DC Output Offset Level (Note 15)	Signal Input (Pedestal Level)	–100	0	100	mV
	No Signal Input	-	–572	-	mV
S/N(Note 17) VG1-0 bits = "00"(+6dB)	BW = 100kH ~ 6MHz, S = 0.7Vpp Input	58	70	-	dB
Maximum Output Voltage (Note 15)	fin = 100kHz (Sine wave)	2.62	-	-	Vpp
Secondary Harmonic Distortion VG1-0 bits = "00"(+6dB), f = 3.58MHz, 1.0Vpp: –40 ~ 100IRE, Sine Wave Input		-	–40	–30	dB
Load Resistance		140	150	-	Ω
Load Capacitance	C2 (Figure 3)	-	-	15	pF
	C3 (Figure 3)	-	-	400	pF
PSRR VG1-0 bits = "00"(+6dB)	fin = 10kHz	-	60	-	dB
	fin = 100kHz	-	45	-	dB
LPF for VIN signal : (Note 15)					
Frequency Response (f = 100kHz, 1.0Vpp, Sine wave Input)					
	Response at 6.75MHz	–3.0	0	+1.5	dB
	Response at 27MHz	-	–40	–30	
Group Delay	|GD3MHz–GD6MHz|	-	10	100	ns

Note 15. This is a value at measurement point in Figure 3. 1.0Vpp input is the value when VG1-0 bits ="00". Input amplitude is in inverse proportion to the gain. S/N is measured at measurement point 2.

Note 16. PMV bit must be set to "0" if the input impedance of the VIN pin exceeds 600Ω when the input signal is stopped or when the VIN pin input circuit is powered down.

Note 17. S/N = 20xlog (Output Voltage[Vpp]/Noise Level[Vrms]). Output Voltage = 0.7 [Vpp].

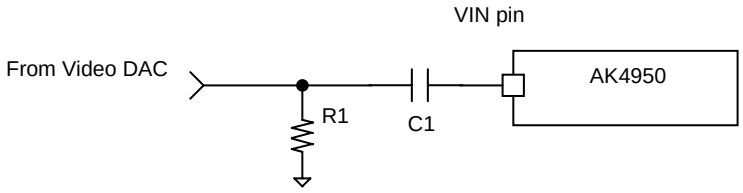


Figure 2. External Resistor of Video Signal Input pin

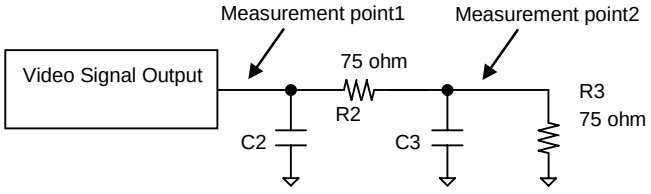


Figure 3. Load Capacitance C2 and C3

Parameter		min	typ	max	Unit
Power Supplies:					
Power Up (PDN pin = "H")					
	All Circuit Power-up (Note 18)				
	AVDD+TVDD	-	22.2	33	mA
	MIC + ADC (Note 15)				
	AVDD+TVDD	-	5.5	-	mA
	DAC + Lineout (Note 16)				
	AVDD+TVDD	-	5.2	-	mA
	DAC + SPK-Amp				
	AVDD+TVDD	-	6	-	mA
	Video Block (Note 22)				
	AVDD	-	12.7	19	mA
Power Down (PDN pin = "L") (Note 17)					
	AVDD+TVDD	-	1	5	μA

Note 18. When PMADL=PMADR=PMDAC=PMPFIL =PMLO=PMSPK=PMPLL=MCKO=PMBP=PMMP=M/S= PMV bits = "1", SPK-amp No load, and black signal is only input to the VIN pin in PLL Master Mode (MCKI=12MHz). In this case, the output current of the MPWR pin is 0mA. AVDD=20.7mA (typ), TVDD=1.5mA (typ).

Note 19. When PMADL = PMADR bits= "1" and PMPFIL bit = "1" in EXT Slave Mode (PMPLL=M/S=MCKO bits ="0").

Note 20. When PMDAC = PMLO bits= "1" and PMPFIL bit = "1" in EXT Slave Mode (PMPLL=M/S=MCKO bits ="0").

Note 21. When PMDAC = PMSPK =SPPSN bits = "1", PMPFIL bit = "1", and No load at SPK-amp in EXT Slave Mode (PMPLL=M/S=MCKO bits ="0").

Note 22. When PMV=PMCP bits = "1", No-load, and the black signal is only input to the VIN pin.

Note 23. All digital input pins are fixed to TVDD or VSS2.

FILTER CHARACTERISTICS

(Ta =25°C; AVDD=2.7 ~ 3.6V, TVDD =1.6 ~ 3.6V; fs=44.1kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 24)	±0.16dB	PB	0	-	17.3	kHz
	–0.66dB		-	19.4	-	kHz
	–1.1dB		-	19.9	-	kHz
	–6.9dB		-	22.1	-	kHz
Stopband (Note 24)		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 25)		GD	-	19	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	3.4	-	Hz
	–0.5dB		-	10	-	Hz
	–0.1dB		-	22	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 24)	±0.05dB	PB	0	-	20.0	kHz
	–6.0dB		-	22.05	-	kHz
Stopband (Note 24)		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.02	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 25)		GD	-	20	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 24. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz. For example, it is 0.454 x fs (ADC) when PB=20.0kHz (@–1.0dB).

Note 25. A calculating delay time which induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the DAC, this time is from setting the 24-bit data of a channel from the input register to the output of analog signal. Group delay time is the same as the value shown above even when a signal path that includes the programmable filters (1st order HPF + 1st order LPF + 3-band Equalizer + ALC + Equalizer) is selected.

DC CHARACTERISTICS

(Ta =25°C; AVDD=2.7 ~ 3.6V, TVDD =1.6 ~ 3.6V; fs= 44.1kHz; DEM=OFF)

Parameter	Symbol	min	typ	max	Unit
Audio Interface & Serial µP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)					
High-Level Input Voltage					
(Except I2C pin, TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
(Except I2C pin, TVDD < 2.2V)		80%TVDD	-	-	V
(I2C pin)	VIH1	70%AVDD	-	-	V
Low-Level Input Voltage					
(Except I2C pin, TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
(Except I2C pin, TVDD < 2.2V)		-	-	20%TVDD	V
(I2C pin)	VIL1	-	-	30%AVDD	V
Audio Interface & Serial µP Interface (CDTIO, SDA MCKO, BICK, LRCK, SDTO pins Output)					
High-Level Output Voltage (Iout = −80µA)	VOH	TVDD−0.2	-	-	V
Low-Level Output Voltage					
(Except SDA pin : Iout = 80µA)	VOL1	-	-	0.2	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout = 3mA)	VOL2	-	-	0.4	V
(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Input Leakage Current	Iin	-	-	±10	µA
Digital MIC Interface (DMDAT pin Input ; DMIC bit = "1")					
High-Level Input Voltage	VIH2	65%AVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	35%AVDD	V
Digital MIC Interface (DMCLK pin Output ; DMIC bit = "1")					
High-Level Output Voltage (Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 80µA)	VOL3	-	-	0.4	V
Input Leakage Current	Iin2	-	-	±20	µA

SWITCHING CHARACTERISTICS

(Ta =25°C; AVDD=2.7 ~ 3.6V, TVDD =1.6 ~ 3.6V; C_L=20pF)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.256	-	12.288	MHz
Duty Cycle		dMCK	40	50	60	%
LRCK Output Timing						
Frequency		fs	8	-	48	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.256	-	12.288	MHz
Duty Cycle		dMCK	40	50	60	%
LRCK Input Timing						
Frequency		fs	8	-	48	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter			Symbol	min	typ	max	Unit
PLL Slave Mode (PLL Reference Clock = BICK pin)							
LRCK Input Timing							
Frequency			fs	7.35	-	48	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period	PLL3-0 bits = "0010"		tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = "0011"		tBCK	-	1/(64fs)	-	ns
Pulse Width Low			tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High			tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode							
MCKI Input Timing							
Frequency	512fs		fCLK	3.7632	-	24.576	MHz
	1024fs		fCLK	7.5264	-	13.312	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing							
Frequency	512fs		fs	7.35	-	48	kHz
	1024fs		fs	7.35	-	13	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period			tBCK	312.5	-	-	ns
Pulse Width Low			tBCKL	130	-	-	ns
Pulse Width High			tBCKH	130	-	-	ns
External Master Mode							
MCKI Input Timing							
Frequency	512fs		fCLK	3.7632	-	24.576	MHz
	1024fs		fCLK	7.5264	-	13.312	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing							
Frequency			fs	7.35	-	48	kHz
Duty Cycle			Duty	-	50	-	%
BICK Output Timing							
Period		BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
		BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle			dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 26)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 26)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 26)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Mode):					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 27)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 27)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command)(Note 29)	tCCZ	-	-	70	ns
Control Interface Timing (I²C Bus Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 30)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

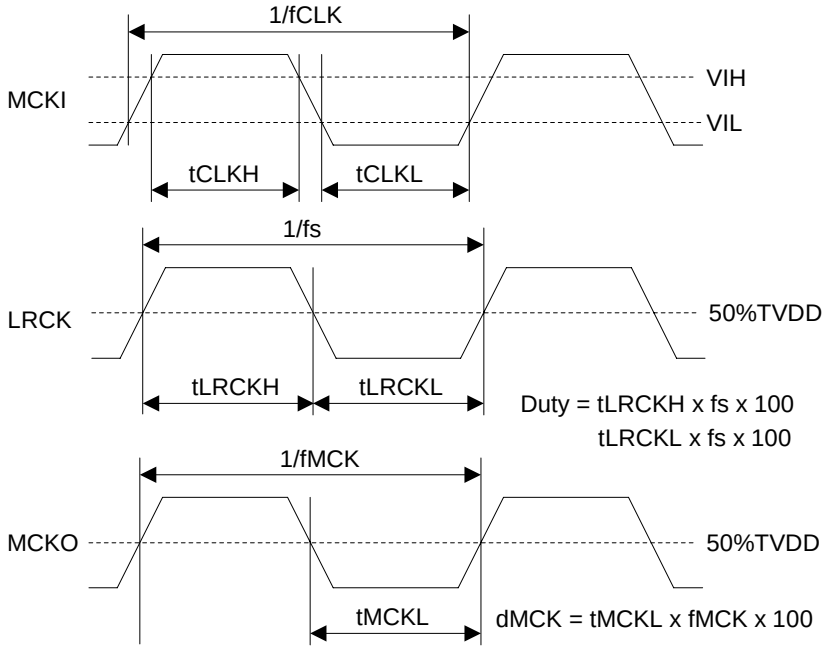
Note 26. BICK rising edge must not occur at the same time as LRCK edge.
Note 27. CCLK rising edge must not occur at the same time as CSN edge.
Note 28. I²C-bus is a trademark of NXP B.V.
Note 29. It is the time of 10% potential change of the CDTIO pin when R_L=1kΩ (pull-up or TVDD).
Note 30. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Parameter	Symbol	min	typ	max	Unit
Digital Audio Interface Timing; C_L=100pF					
DMCLK Output Timing					
Period	tSCK	-	1/(64fs)	-	ns
Rising Time	tSRise	-	-	10	ns
Falling Time	tSFall	-	-	10	ns
Duty Cycle	dSCK	40	50	60	%
Audio Interface Timing					
DMDAT Setup Time	tSDS	50	-	-	ns
DMDAT Hold Time	tSDH	0	-	-	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 31)	tPD	150	-	-	ns
PMADL or PMADR "↑" to SDTO valid (Note 32)					
ADRST bit = "0"	tPDV	-	1059	-	1/fs
ADRST bit = "1"	tPDV	-	267	-	1/fs

Note 31. The AK4950 can be reset by the PDN pin = "L". When restart the AK4950 after powered-down, set the PDN pin to "L" and change to "H" after a 10ms interval.

Note 32. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

■ Timing Diagram



Note 33. MCKO is not available at EXT Master mode.
Figure 4. Clock Timing (PLL/EXT Master mode)

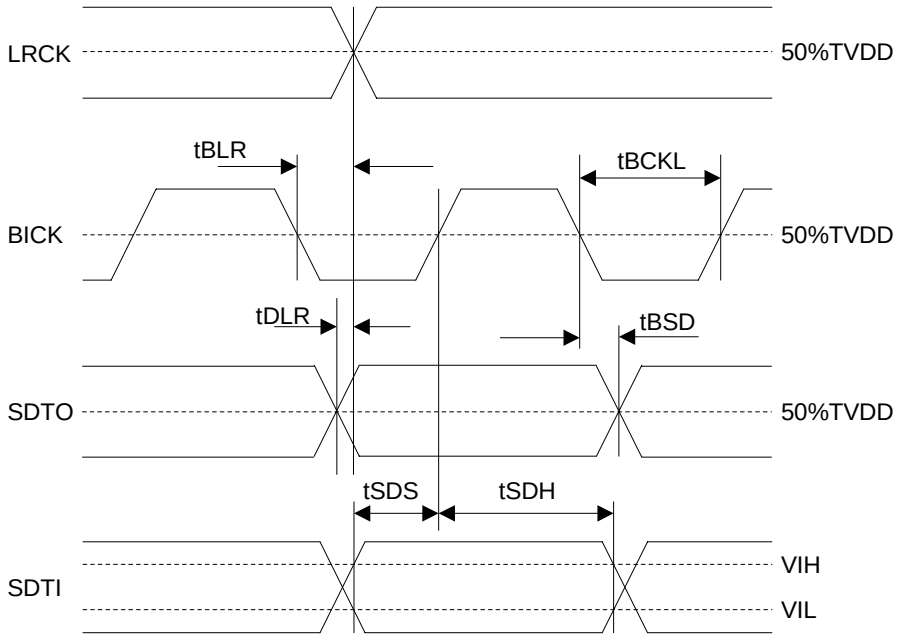


Figure 5. Audio Interface Timing (PLL/EXT Master mode)

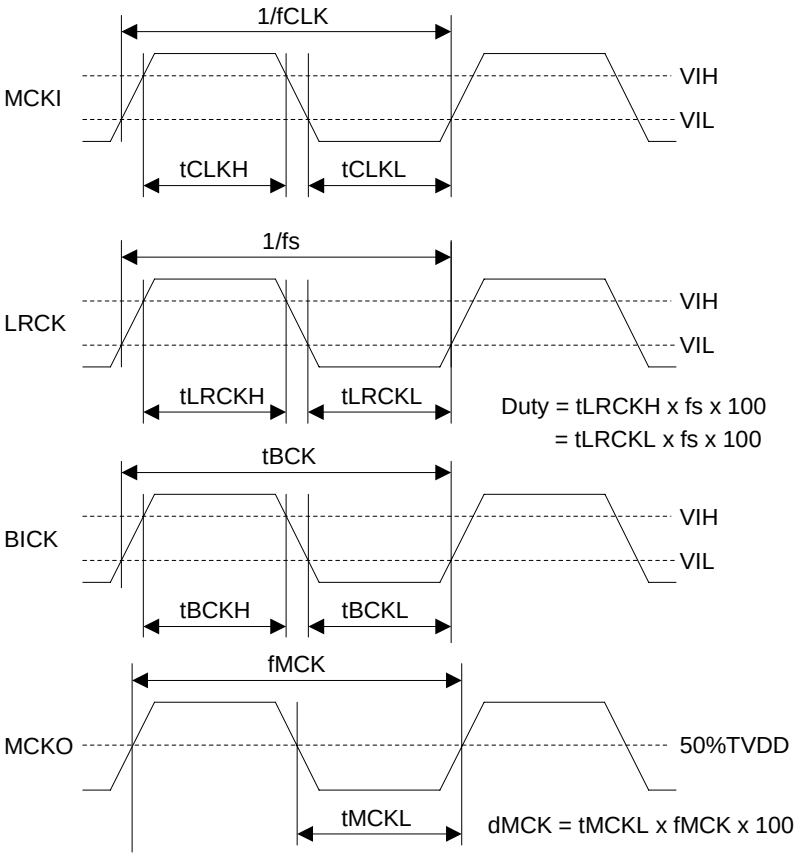


Figure 6. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin)

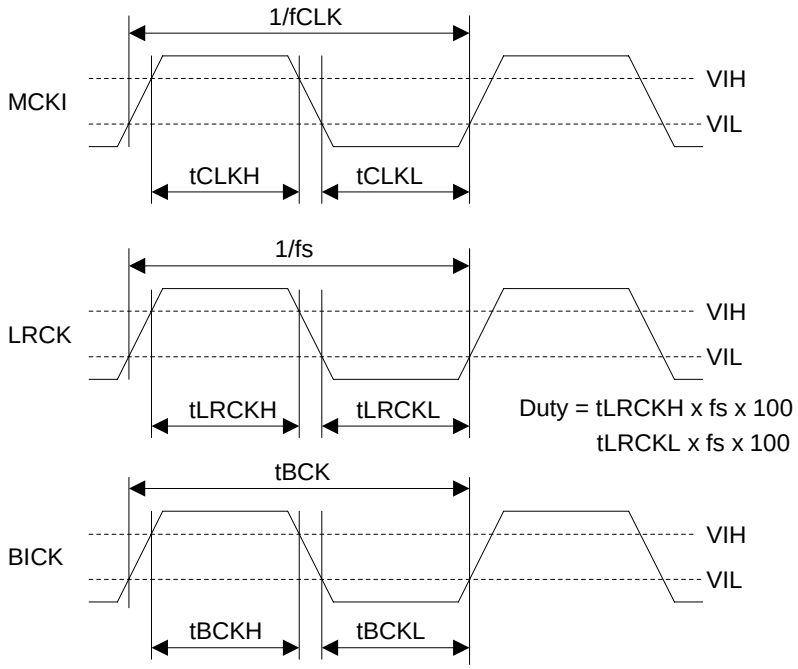


Figure 7. Clock Timing (EXT Slave mode)

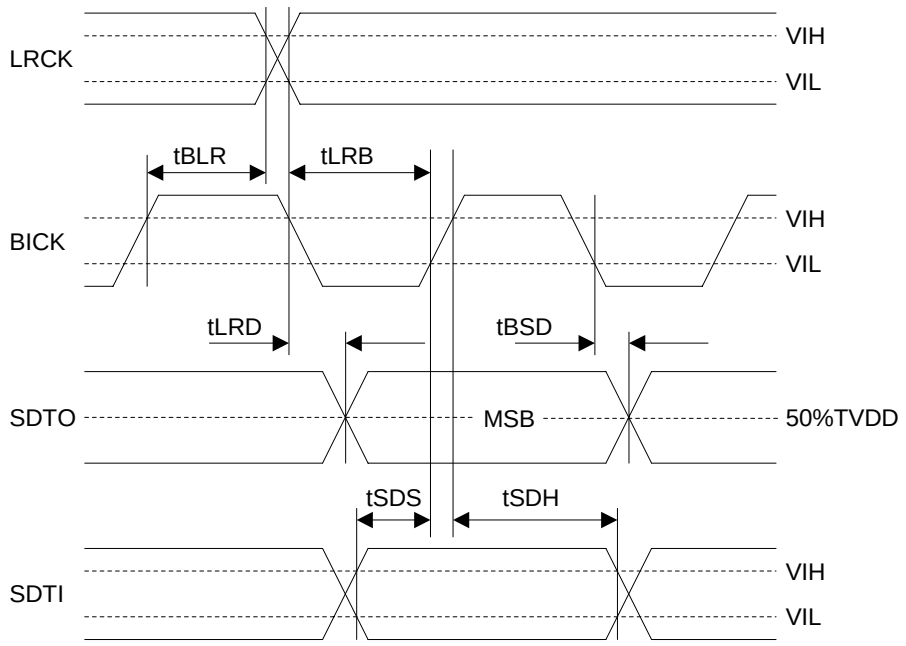


Figure 8. Audio Interface Timing (PLL/EXT Slave mode)

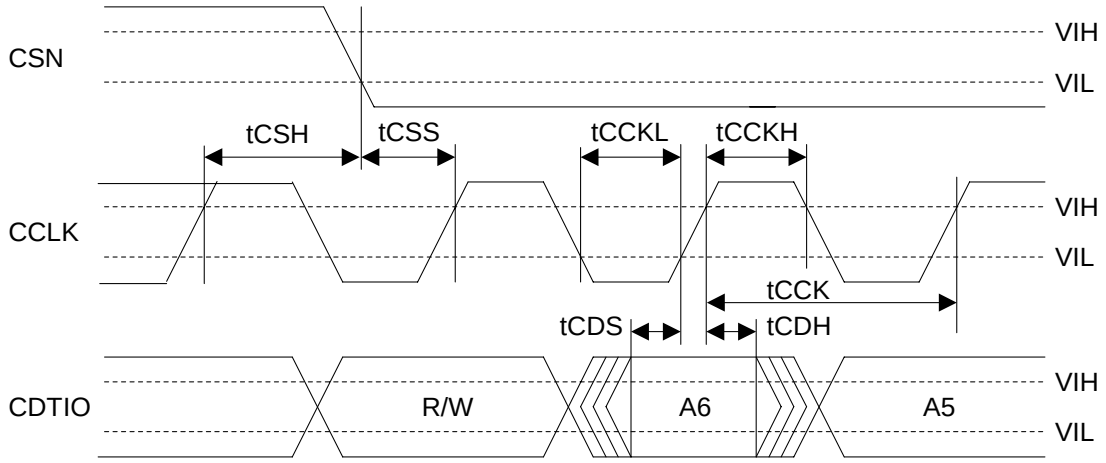


Figure 9. WRITE Command Input Timing

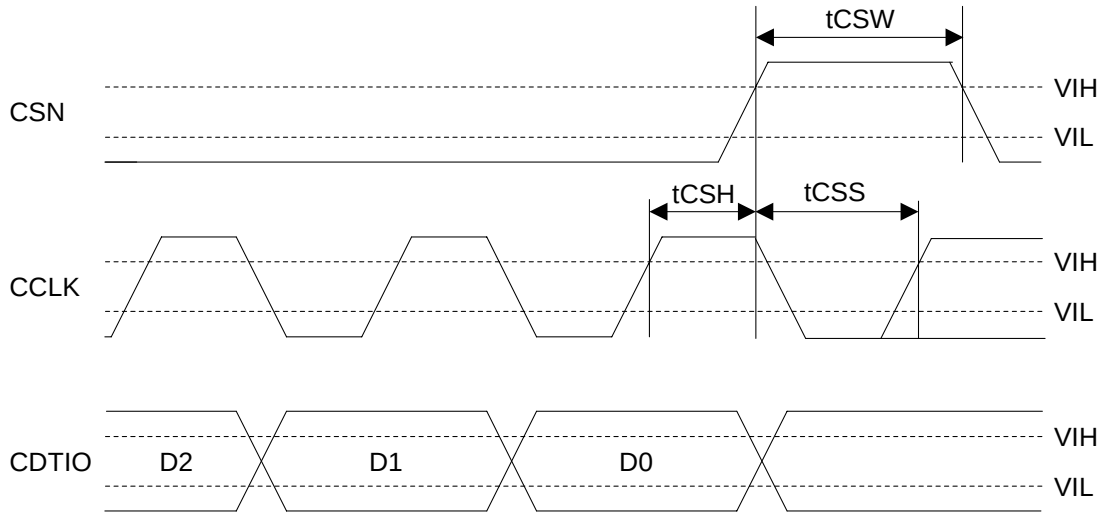


Figure 10. WRITE Data Input Timing

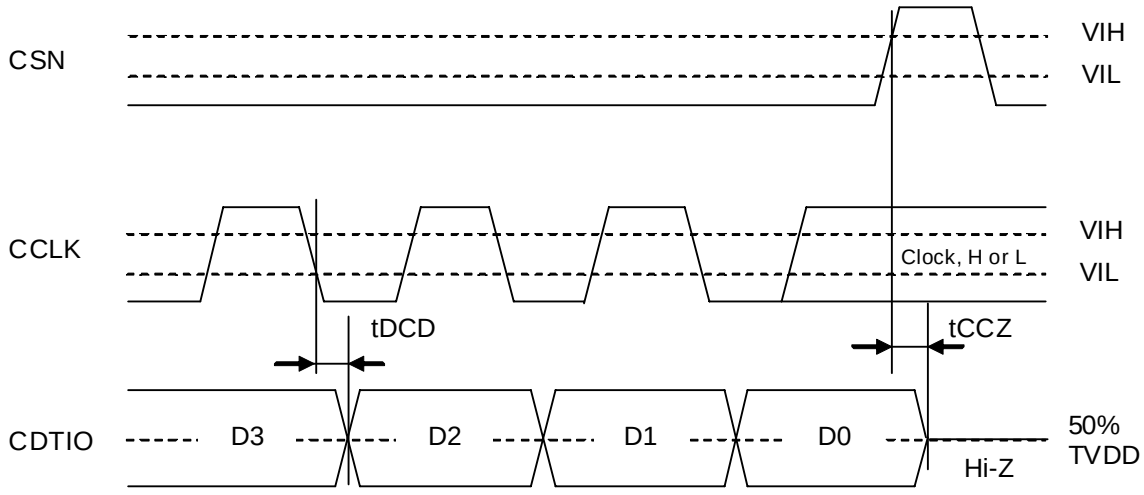


Figure 11. Read Data Output Timing

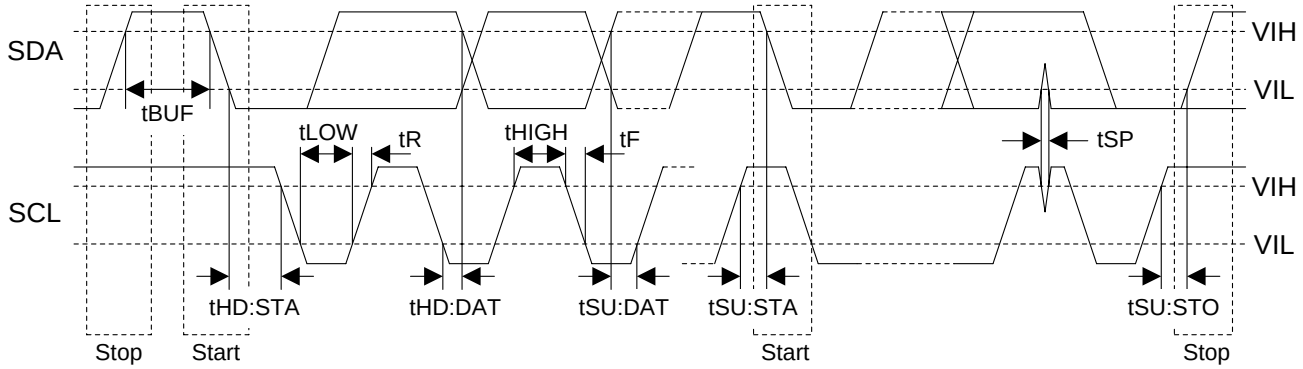
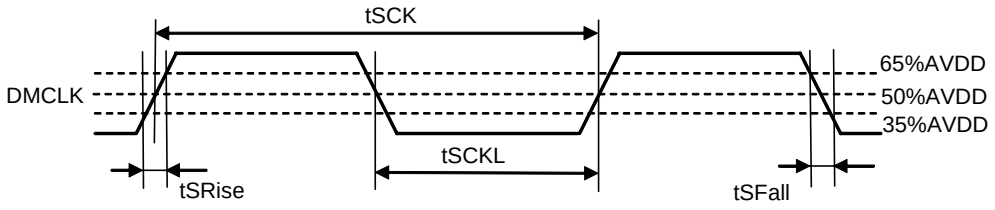


Figure 12. I^{2}C Bus Mode Timing



dSCK = 100 x tSCKL / tSCK

Figure 13. DMCLK Clock Timing

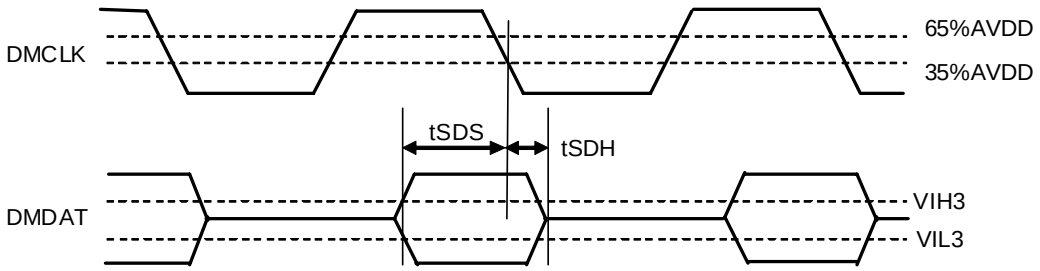


Figure 14. Audio Interface Timing (DCLKP bit = "1")

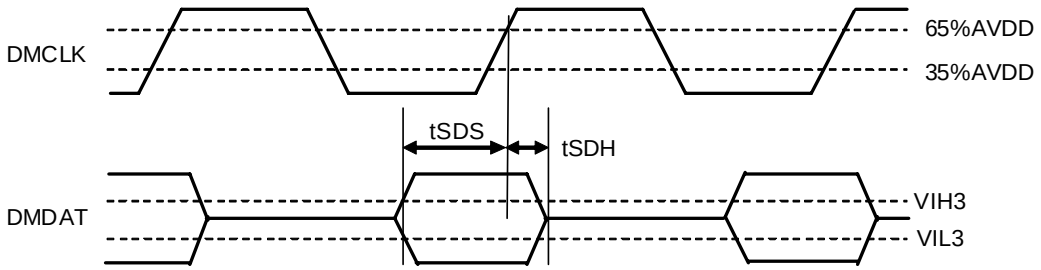


Figure 15. Audio Interface Timing (DCLKP bit = "0")

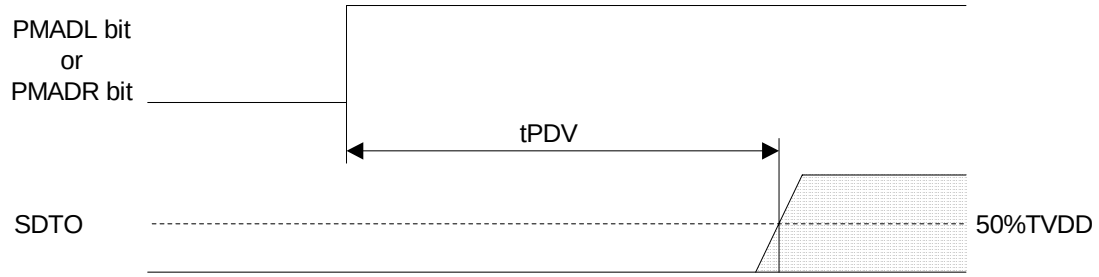


Figure 16. Power Down & Reset Timing 1

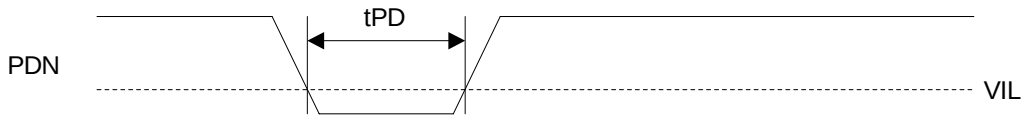


Figure 17. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 1, Table 2).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 34)	1	1	Table 4	Figure 18
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 4	Figure 19
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	Table 4	Figure 20
EXT Slave Mode	0	0	x	Figure 21
EXT Master Mode	0	1	x	Figure 22

Note 34. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from the MCKO pin.

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: BICK pin)	0	L	GND	Input (≥ 32fs)	Input (1fs)
EXT Slave Mode	0	L	Selected by FS3-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	0	L	Selected by FS1-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Note 35. When PMVCM bit = M/S bit = "1" and MCKI is input, LRCK and BICK are output even if PMDAC=PMADL= PMADR bits = "0".

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4950 is in power-down mode (PDN pin = "L") and when exits reset state, the AK4950 is in slave mode. After exiting reset state, the AK4950 goes to master mode by changing M/S bit to "1".

When the AK4950 is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes "1". The LRCK and BICK pins of the AK4950 must be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock times, when the AK4950 is supplied stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or the sampling frequency is changed, are shown in Table 4.

1) PLL Mode Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)	
2	0	0	1	0	BICK pin	32fs	2 ms	
3	0	0	1	1	BICK pin	64fs	2 ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10 ms	
6	0	1	1	0	MCKI pin	12MHz	10 ms	(default)
7	0	1	1	1	MCKI pin	24MHz	10 ms	
12	1	1	0	0	MCKI pin	13.5MHz	10 ms	
13	1	1	0	1	MCKI pin	27MHz	10 ms	
Others	Others				N/A			

Note 36. The resistor tolerance is ±5% and the capacitor tolerance is ±30%.

Table 4. PLL Mode Setting (*fs: Sampling Frequency, N/A: Not Available)

2) Setting of sampling frequency in PLL Mode

When PLL2 bit is "1" (PLL reference clock input is MCKI pin), the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
5	0	1	0	1	11.025kHz	
7	0	1	1	1	22.05kHz	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
15	1	1	1	1	44.1kHz	(default)
Others	Others				N/A	

Table 5. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1"
(Reference Clock = MCKI pin), (N/A: Not Available)

When PLL2 bit is "0" (PLL reference clock input pin is the BICK pin), the sampling frequency is selected by FS1-0 bits. (Table 6). * Since the default setting of FS3-0 bits is "1111" (Not Available), FS3-0 bits must be set when PLL2 bit = "0".

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	x	x	7.35kHz ≤ fs ≤ 12kHz	
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	0	x	x	24kHz < fs ≤ 48kHz	
Others	Others				N/A	(default)

Table 6. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1" PLL Slave Mode 2
(PLL Reference Clock: BICK pin), (x: Don't care, N/A: Not Available)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, the LRCK and BICK pins go to "L", and irregular frequency clock is output from the MCKO pin when MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin outputs "L" (Table 7).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

The BICK and LRCK pins do not output irregular frequency clocks such as PLL unlock state by setting PMPLL bit to "0". During PMPLL bit = "0", these pins output the same clocks as EXT Master Mode.

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except the case above)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	Table 9	Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". Then, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. The DAC outputs can be muted by setting DACL and DACS bits to "0".

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock (except the case above)	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, the internal PLL circuit generates MCKO, BICK and LRCK clocks. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 10).

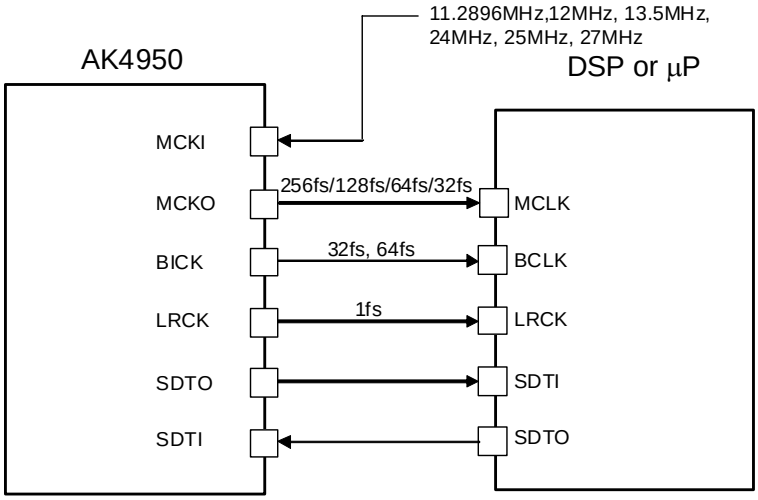


Figure 18. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 10. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to the MCKI, BICK or LRCK pins. The required clock for the AK4950 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL reference clock: MCKI pin

The BICK and LRCK inputs must be synchronized with MCKO output. The phase between MCKO and LRCK is not important. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5)

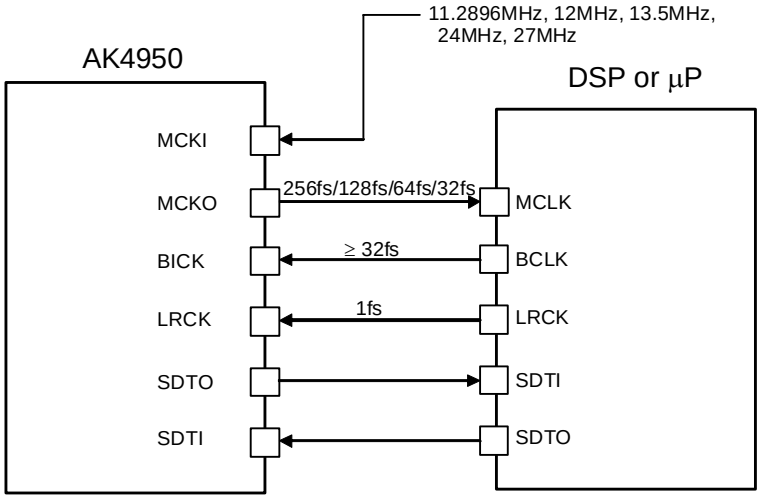


Figure 19. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK pin

The sampling frequency corresponds to a range from 7.35kHz to 48kHz by changing FS3-0 bits (Table 6).

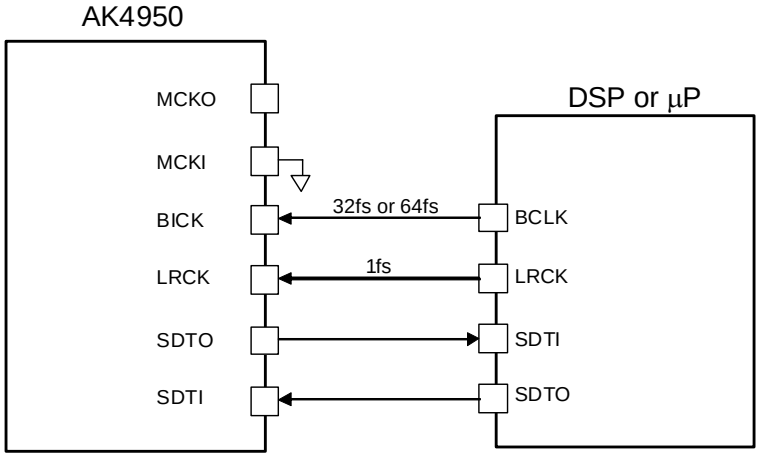


Figure 20. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4950 becomes EXT mode. Master clock can be input to the internal ADC and DAC directly from the MCKI pin without internal PLL circuit operation. This mode is compatible with I/F of a normal audio CODEC. The external clocks required to operate this mode are MCKI (512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) must be synchronized with LRCK. The phase between these clocks is not important. The input frequency of MCKI is selected by FS1-0 bits (Table 11).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
1	x	0	1	1024fs	7.35kHz ~ 13kHz	
2	x	1	0	512fs	7.35kHz ~ 26kHz	
3	x	1	1	512fs	7.35kHz ~ 48kHz	(default)
Others	Others			N/A	N/A	

(x: Don't care, N/A: Not Available)

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins is shown in Table 12.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
Mode3; 512fs	80dB
Mode2; 512fs	92dB
Mode1; 1024fs	92dB

Table 12. Relationship between MCKI and S/N of LOUT/ROUT pins

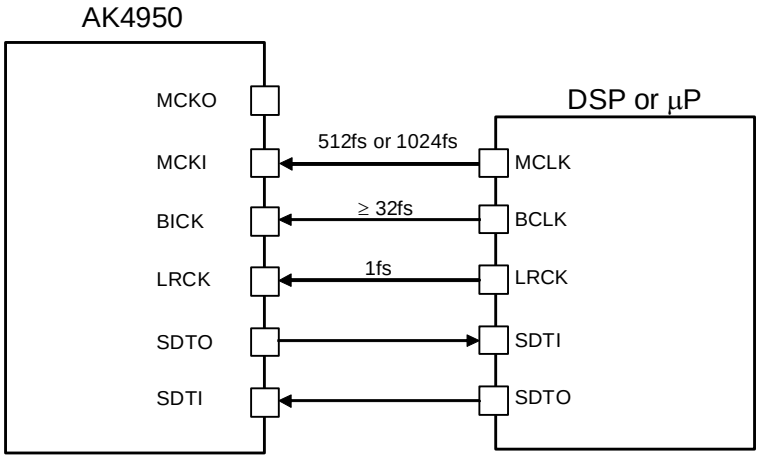


Figure 21. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The AK4950 becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock can be input to the internal ADC and DAC directly from the MCKI pin without the internal PLL circuit operation. The external clock required to operate the AK4950 is MCKI (512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (Table 13).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
1	x	0	1	1024fs	7.35kHz ~ 13kHz	
2	x	1	0	512fs	7.35kHz ~ 26kHz	
3	x	1	1	512fs	7.35kHz ~ 48kHz	(default)
Others	Others			N/A	N/A	

(x: Don't care, N/A: Not Available)

Table 13. MCKI Frequency at EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins is shown in Table 14.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
Mode3; 512fs	80dB
Mode2; 512fs	92dB
Mode1; 1024fs	92dB

Table 14. Relationship between MCKI and S/N of LOUT/ROUT pins

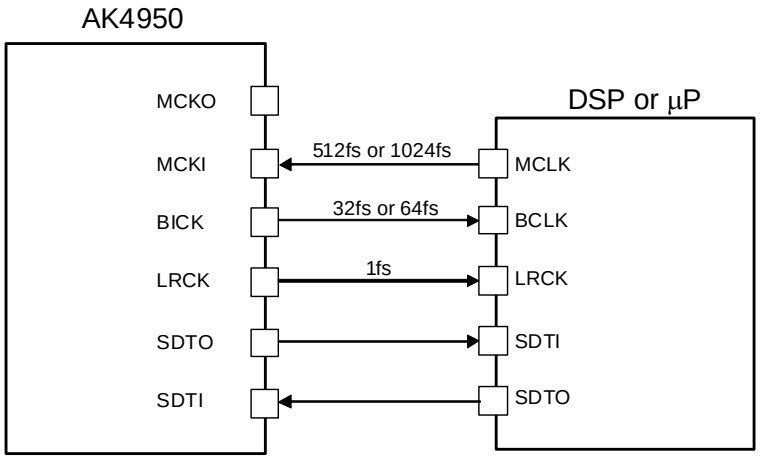


Figure 22. EXT Master Mode

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 15. BICK Output Frequency at Master Mode

■ System Reset

Upon power-up, the AK4950 must be reset by bringing the PDN pin = "L". It ensures that all internal registers are initialized. When restart the AK4950 after powered-down, the PDN pin should be set to "L" and hold 10ms. Then set the PDN pin to "H", and INIT bit should be set to "1" after clocks are input. It is recommended to set the PDN pin = "L" before power up the AK4950.

The ADC starts an initialization cycle if the one of PMADL or PMADR bit is set to "1" when both of the PMADL and PMADR bits are "0". The initialization cycle is set by ADRST bit (Table 16). During the initialization cycle, the ADC digital data outputs of both channels are forced to "0" in 2's complement. The ADC output reflects the analog input signal after the initialization cycle is finished. When using a digital microphone, the initialization cycle is the same as ADC's.

(Note) The initial data of ADC has offset data that depends on microphones and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer by setting ADRST bit or do not use the first data of ADC outputs.

ADRST bit	Init Cycle			
	Cycle	fs = 8kHz	fs = 16kHz	fs = 44.1kHz
0	1059/fs	132.4ms	66.2ms	24ms
1	267/fs	33.4ms	16.7ms	6.1ms

Table 16. ADC Initialization Cycle

■ Audio Interface Format

Four types of data formats are available and selected by setting the DIF1-0 bits (Table 17). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats are supported in both master and slave modes. LRCK and BICK are output from the AK4950 in master mode, but must be input to the AK4950 in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑") of BICK.

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	24bit MSB justified	24bit LSB justified	≥ 48fs	Figure 23	
1	0	1	24bit MSB justified	16bit LSB justified	≥ 32fs	Figure 24	
2	1	0	24bit MSB justified	24bit MSB justified	≥ 48fs	Figure 25	(default)
3	1	1	I^2S Compatible	I^2S Compatible	=32fs or ≥ 48fs	Figure 26	

Table 17. Audio Interface Format

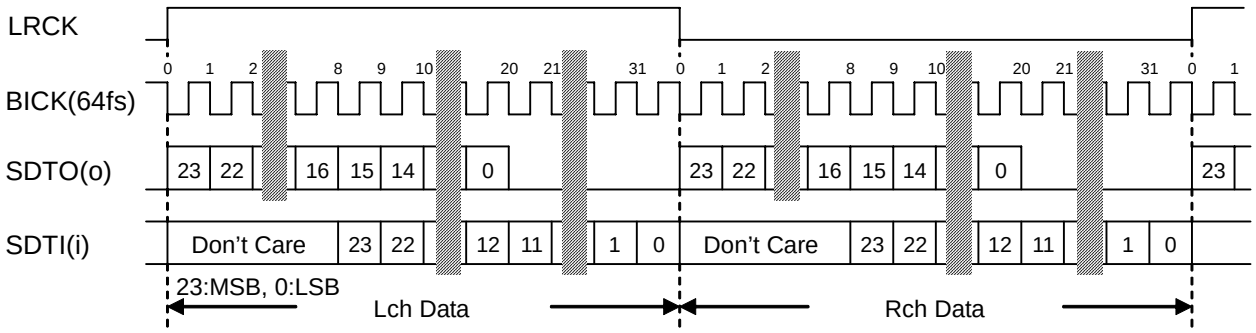


Figure 23. Mode 0 Timing

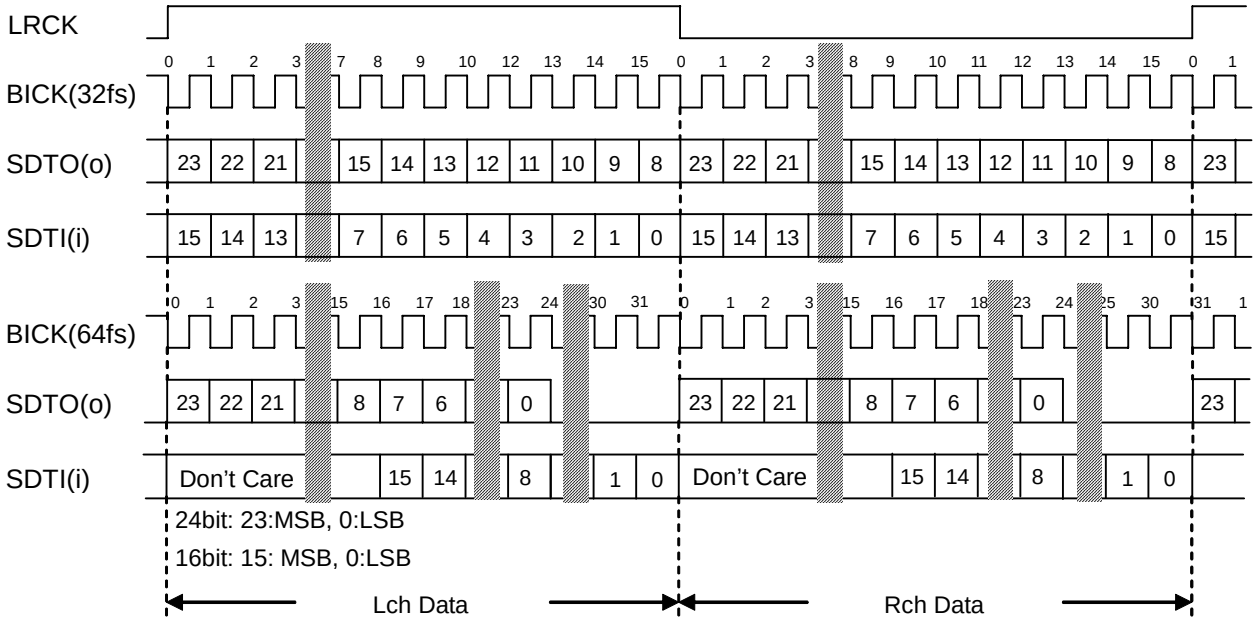


Figure 24. Mode 1 Timing

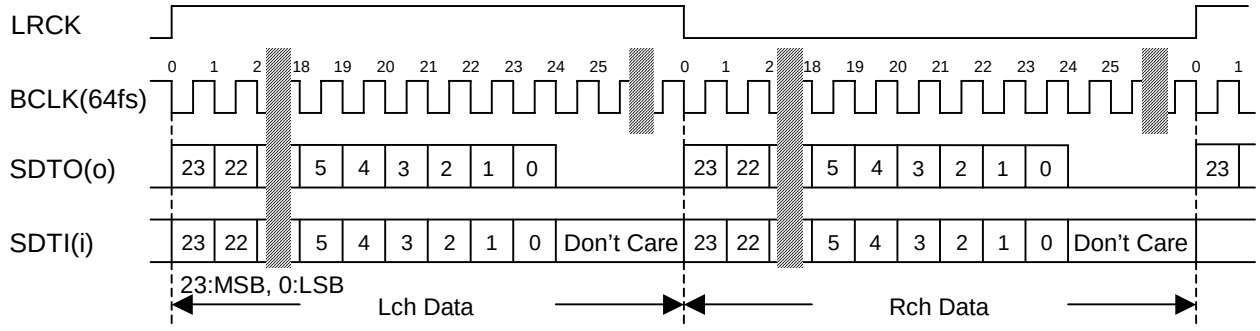


Figure 25. Mode 2 Timing

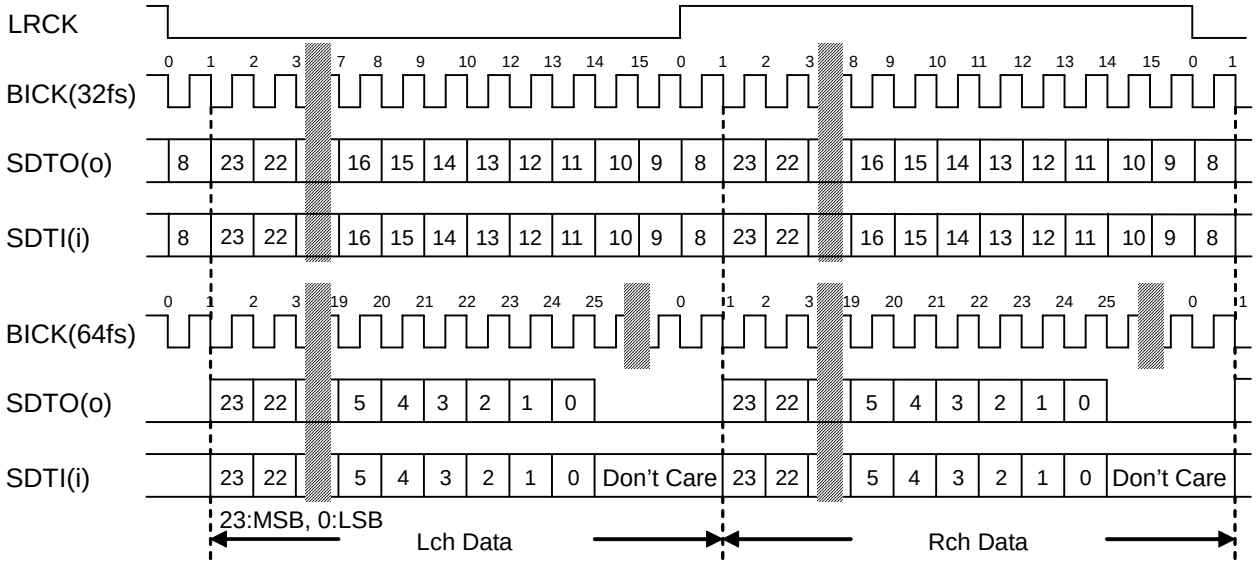


Figure 26. Mode 3 Timing

■ Mono/Stereo Mode

PMADL, PMADR, PMDML and PMDMR bits set mono/stereo ADC operation. When changing ADC operation and analog/digital microphone, PMADL, PMADR, PMDML and PMDMR bits must be set "0" at first. When PMDML or PMDMR bit = "1", the setting of PMADL and PMADR bits is ignored.

PMADL bit	PMADR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 18. Mono/Stereo ADC operation (Analog MIC)

PMDML bit	PMDMR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 19. Mono/Stereo ADC operation (Digital MIC)

■ MIC/LINE Input Selector

The AK4950 has an input selector. INL and INR bits select LIN1/LIN2 and RIN1/RIN2, respectively. When DMIC bit = "1", digital microphone input is selected regardless of INL and INR bits.

DMIC bit	INL bit	INR bit	Lch	Rch	
0	0	0	LIN1	RIN1	(default)
	0	1	LIN1	RIN2	
	1	0	LIN2	RIN1	
	1	1	LIN2	RIN2	
1	0	0	Digital Microphone		
	0	1			
	1	0			
	1	1			

Table 20. MIC/Line In Path Select (x: Don't care, N/A: Not available)

■ MIC Gain Amplifier

The AK4950 has a gain amplifier for microphone input. The gain of MIC-Amp is selected by the MGAIN3-0 bits (Table 21). The typical input impedance is 30kΩ.

MGAIN3 bit	MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0	0	0dB	
0	0	0	1	+5dB	
0	0	1	0	+8dB	
0	0	1	1	+11dB	
0	1	0	0	+14dB	
0	1	0	1	+16dB	
0	1	1	0	+18dB	(default)
0	1	1	1	+21dB	
1	0	0	0	+24dB	
Others				N/A	

(N/A: Not available)

Table 21. Input Gain

■ MIC Sensitivity Compensation

The AK4950 has microphone sensitivity (Inter-channel gain mismatch) compensation function controlled by MSGAINL3-0 bits (Lch) and MSGAINR3-0 bits (Rch)

MSGAINL3-0 bits MSGAINR3-0 bits	GAIN (dB)	Step	
0111	+5.25	0.75dB	
0110	+4.50		
0101	+3.75		
0100	+3.00		
0011	+2.25		
0010	+1.50		
0001	+0.75		
0000	0		(default)
1111	–0.75		
1110	–1.50		
1101	–2.25		
1100	–3.00		
1011	–3.75		
1010	–4.50		
1001	–5.25		
1000	–6.00		

Table 22. MIC Sensitivity Compensation

MIC sensitivity compensation gain can be written directly to the DSP by setting 01H and 02H (in 3-wire mode) or 81H and 82H (in I^2C mode) without setting MAGAINL/R3-0 bits. In this case, the gain can be set in a step less than 0.1dB.

The target gain is Y[dB],

$X=10^{(Y[dB]/20)} \times 2^{20}$ (Y[dB] ≤ +18dB)
Available Gain Setting Range: -∞ ≤ Gain < +18dB (The coefficient has a 20-bit accuracy)

Round X off to the closest whole number and convert it to two's complement.
MSB of the MIC sensitivity compensation register is a sign bit.

E.g.) MIC sensitivity compensation value = -3.0[dB]
$X = 10^{(-3/20)} \times 2^{20} = 742335$
742335(dec) = 0B53BE(hex): Register value to be written

The following is an access sequence to Register Map 2.

Sequence Example (3-wire Mode):

1. PMPFIL bit = "0"
2. INIT bit = "1"
3. COEW bit = "1"
4. Addr=01H, Data=xxxxxxH(24bit Data); Lch MIC Sensitivity Compensation Value
5. Addr=02H, Data=xxxxxxH(24bit Data); Rch MIC Sensitivity Compensation Value
6. COEW bit = "0"
7. PMPFIL bit = "1"; Programmable Block Power Up

(Note) When accessing to the DSP directly on the address 01H, 02H (in 3-wire mode) or 81H, 82H (in I^2C mode), do not access to MSGAINL/R3-0 bits of the address 2BH.

■ MIC Power

When PMMP bit = "1", the MPWR pin supplies the power for microphones. This output voltage is typically 2.5V @MICL bit ="0" (AVDD=3.0 ~ 3.6V), and typically 2.2V@MICL bit = "1" (AVDD=2.7 ~ 3.6V). The load resistance is minimum 0.5kΩ. In case of using two sets of stereo microphones, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR pin (Figure 27).

The MIC power performance is deteriorated considerably when output the MIC power and SPK-amp at the same time since the MPWR pin output uses VSS3 (SPK-amp VSS). Simultaneous operation of MIC power and SPK-amp is not recommended.

PMMP bit	MPWR pin	
0	Hi-Z	(default)
1	Output	

Table 23. MIC Power

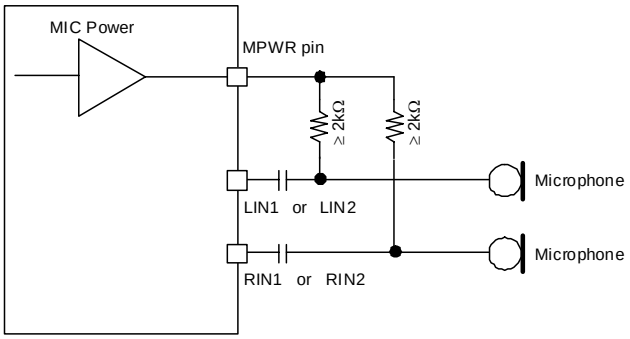


Figure 27. MIC Block Circuit

■ Digital MIC

1. Connection to Digital Microphones

When DMIC bit is set to "1", the LIN1 and RIN1 pins become DMDAT (digital microphone data input) and DMCLK (digital microphone clock supply) pins respectively. The same voltage as AVDD must be provided to the digital microphone. The Figure 28 and Figure 29 show stereo/mono connection examples. The DMCLK clock is input to a digital microphone from the AK4950. The digital microphone outputs 1bit data, which is generated by ΔΣModulator using DMCLK clock, to the DMDAT pin. PMDML/R bits control power up/down of the digital block (Decimation Filter and Digital Filter). PMADL/PMADR bits settings do not affect the digital microphone power management. The DCLKE bit controls ON/OFF of the output clock from the DMCLK pin. When the AK4950 is powered down (PDN pin= "L"), the DMCLK and DMDAT pins become floating state. Pull-down resistors must be connected to the DMCLK and DMDAT pins externally to avoid this floating state.

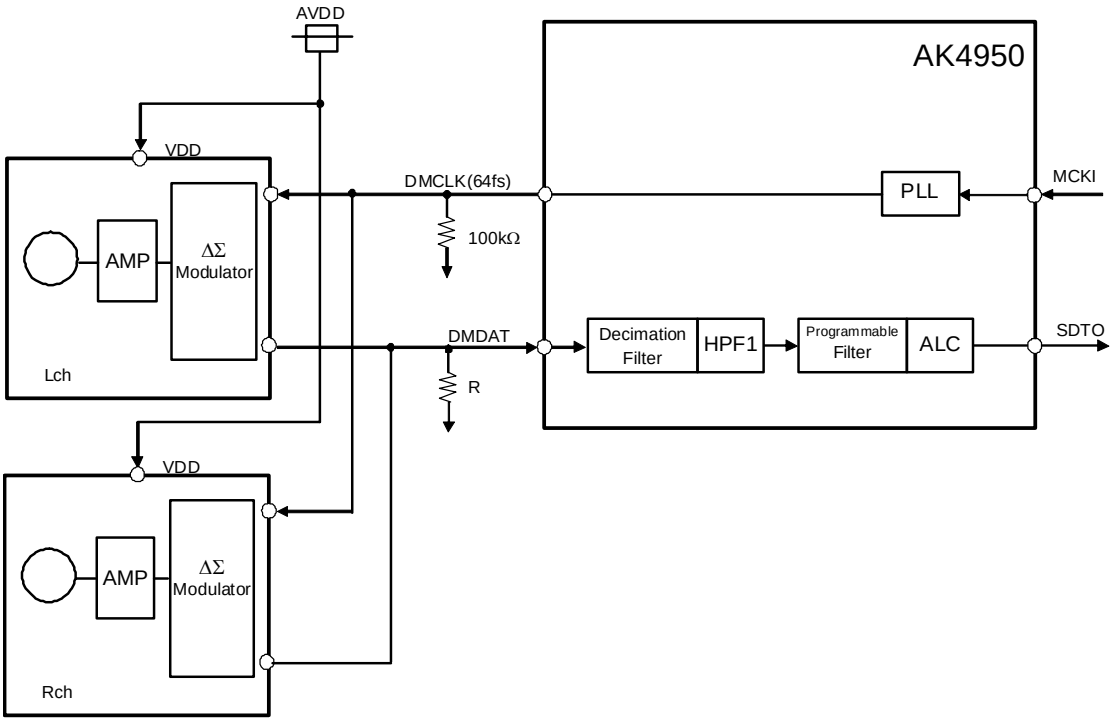


Figure 28. Connection Example of Stereo Digital MIC

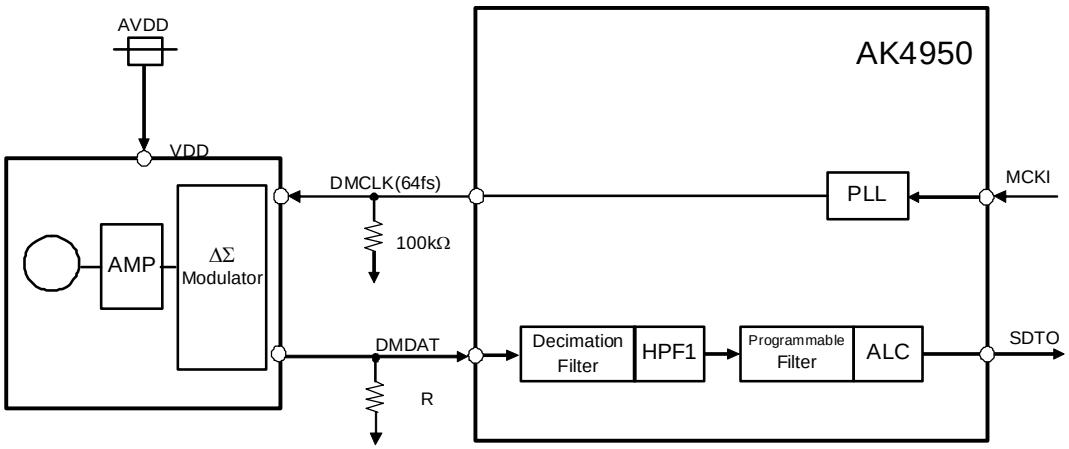


Figure 29. Connection Example of Mono Digital MIC

2. Interface

The input data channel of the DMDAT pin is set by DCLKP bit. When DCLKP bit = "1", L channel data is input to the decimation filter if DMCLK = "H", and R channel data is input if DMCLK = "L". When DCLKP bit = "0", R channel data is input to the decimation filter if DMCLK = "H", and L channel data is input if DMCLK = "L". The DMCLK only supports 64fs. It outputs "L" when DCLKE bit = "0", and outputs 64fs when DCLKE bit = "1". In this case, necessary clocks must be supplied to the AK4950 for ADC operation. The output data through "the Decimation and Digital Filters" is 24bit full scale when the 1bit data density is 0%~100%.

DCLKP bit	DMCLK = "H"	DMCLK = "L"	
0	Rch	Lch	(default)
1	Lch	Rch	

Table 24. Data In/Output Timing with Digital MIC (DCLKP bit = "0")

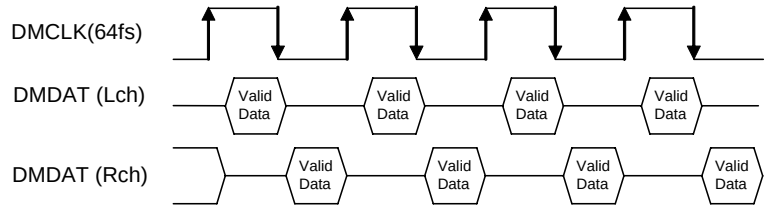


Figure 30. Data In/Output Timing with Digital MIC (DCLKP bit = "1")

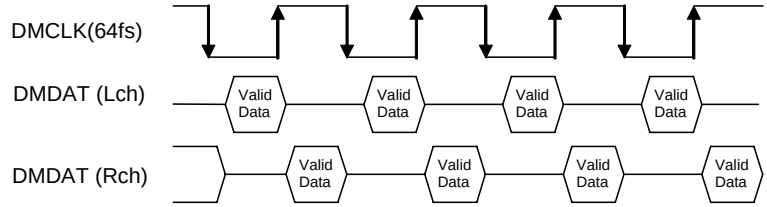
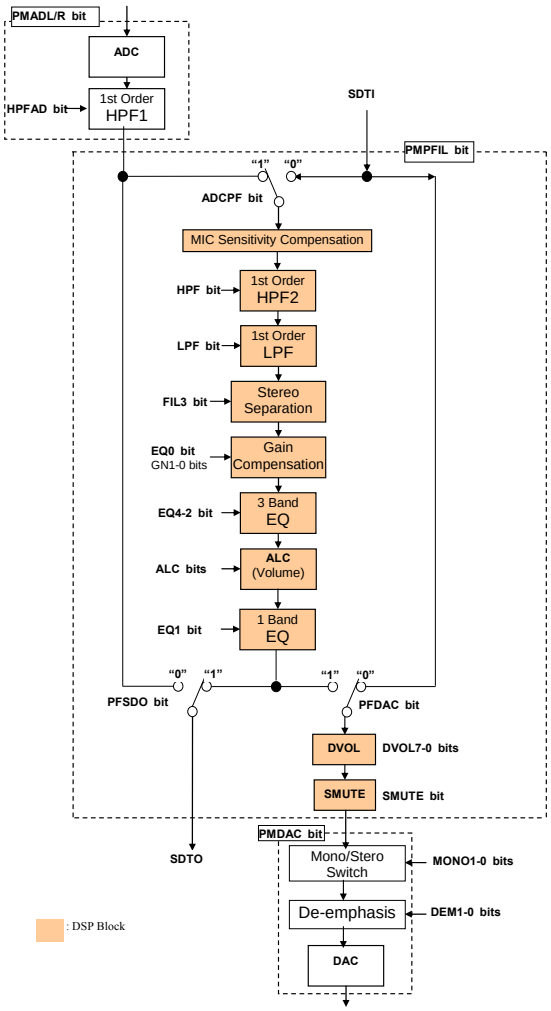


Figure 31. Data In/Output Timing with Digital MIC (DCLKP bit = "0")

■ Digital Block

The digital block consists of the blocks shown in Figure 32. Recording path and playback path is selected by setting ADCPF bit, PFDAC bit and PFSDO bit. (Figure 33 ~ Figure 36, Table 25)



(1) ADC: Includes the Digital Filter (LPF) for ADC as shown in "FILTER CHRACTERISTICS".
(2) HPF1: High Pass Filter (HPF) for ADC as shown in "FILTER CHRACTERISTICS".
(3) MIC Sensitivity Compensation: MIC volume control between L and R channels. (See "MIC Sensitivity Compensation")
(4) DAC: Includes the Digital Filter (LPF) for DAC as shown in "FILTER CHRACTERISTICS".
(5) HPF2: High Pass Filter. Applicable for use as Wind-Noise Reduction Filter. (See "Digital Programmable Filter Circuit")
(6) LPF: Low Pass Filter (See "Digital Programmable Filter Circuit")
(7) Stereo Separation: Stereo separation emphasis filter. (See "Digital Programmable Filter Circuit")
(8) Gain Compensation: Gain compensation consists of EQ and Gain control. It corrects frequency characteristics after stereo separation emphasis filter. (See "Digital Programmable Filter Circuit")
(9) 3 Band EQ: Applicable for use as Equalizer or Notch Filter. (See "Digital Programmable Filter Circuit")
(10) Volume: Digital volume control with ALC function. (See "Input Digital Volume" and "ALC Operation")
(11) 1 Band EQ: Applicable for use as Equalizer or Notch Filter. (See "Digital Programmable Filter Circuit")
(12) DVOL: Digital volume for playback path (See "Output Digital Volume2")
(13) SMUTE: Soft mute function
(14) Mono/Stereo Switching: Mono/Stereo lineout outputs select from DAC which described in <Mono Mixing Output> at "Stereo Line Outputs".
(15) De-emphasis: De-emphasis filter (See "De-emphasis Filter Control")

Figure 32. Digital Block Path Select

Mode	ADCPF bit	PFDAC bit	PFSDO bit	Figure
Recording Mode 1	1	0	1	Figure 33
Playback Mode 1	0	1	0	Figure 34
Recording Mode 2 & Playback Mode 2	x	0	0	Figure 35
Loopback Mode	1	1	1	Figure 36

Table 25. Recording Playback Mode (x: Don't care)

When changing those modes, PMPFIL bit must be "0".

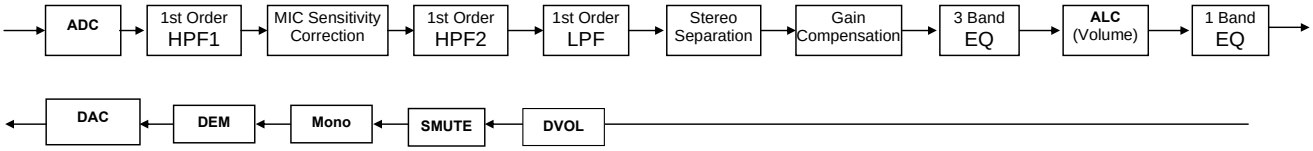


Figure 33. The Path in Recording Mode 1 (default)

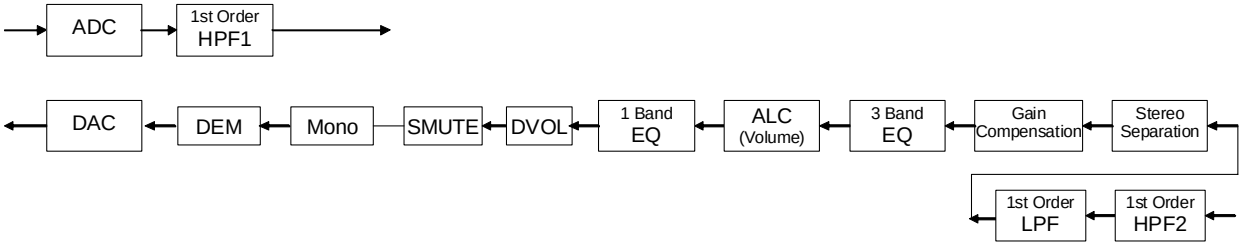


Figure 34. The Path in Playback Mode 1

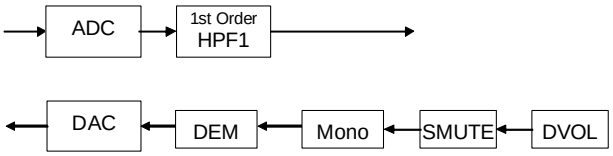


Figure 35. The Path in Recording Mode 2 & Playback Mode 2

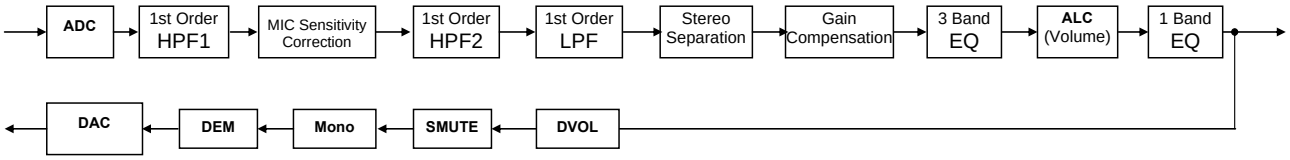


Figure 36. The Path in Loopback Mode

■ Digital Programmable Filter Circuit

(1) High Pass Filter (HPF2)

Normally, this HPF is used for Wind-Noise Reduction. This is composed 1st order HPF. The coefficient of HPF is set by 03H, 04H, 06H (3-wire mode, COEW bit = "1") and 83H, 84H and 86H (I^2C mode). HPF bit controls ON/OFF of the HPF2. When the HPF2 is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when PMPFIL bit = "0". The HPF2 starts operation 2/fs (max) after when HPF bit=PMPFIL bit= "1" is set.

fs: Sampling Frequency
fc: Cutoff Frequency

Register Setting (Register Map 2) (Note 37)
A0: Register Addr = 03H(3-wire mode), 83H(I^2C mode)
A1: Register Addr = 04H(3-wire mode), 84H(I^2C mode)
B1: Register Addr = 06H(3-wire mode), 86H(I^2C mode)

$$A0 = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad A1 = -A0, \quad B1 = \frac{1 / \tan(\pi fc/fs) - 1}{1 / \tan(\pi fc/fs) + 1}$$

Transfer Function

$$H(z) = A0 \frac{1 - z^{-1}}{1 - B1\, z^{-1}}$$

The cut-off frequency must be set as below.
$fc/fs \geq 0.0001$ (fc min = 4.41Hz at 44.1kHz)

Setting Example) When fc=150Hz @ fs=44.1kHz (I^2C mode)
A0 = 0FD4B1 (hex): Addr. 83H
A1 = F02B4F (hex): Addr. 84H
B1 = 0FA963 (hex): Addr. 86H

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. 09H, 0AH, 0CH (3-wire mode, COEW bit = "1") and 89H~8AH and 8CH (I^2C mode) set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when PMPFIL bit = "0". The LPF starts operation 2/fs (max) after when LPF bit =PMPFIL bit= "1" is set.

fs: Sampling Frequency
fc: Cutoff Frequency

Register Setting (Register Map 2) (Note 37)
A0: Register Addr = 09H(3-wire mode), 89H(I^2C mode)
A1: Register Addr = 0AH(3-wire mode), 8AH(I^2C mode)
B1: Register Addr = 0CH(3-wire mode), 8CH(I^2C mode)

$$A0 = A1 = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B1 = \frac{1 / \tan(\pi fc/fs) - 1}{1 / \tan(\pi fc/fs) + 1}$$

Transfer Function

$$H(z) = A0 \frac{1 + z^{-1}}{1 - B1\, z^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.05 (fc min = 2205Hz at 44.1kHz)

Setting Example) When fc=15kHz @ fs=44.1kHz (I^2C mode)
A0 = 0A53F3 (hex): Addr. 89H
A1 = 0A53F3 (hex): Addr. 8AH
B1 = FB581A (hex): Addr. 8CH

(3) Stereo Separation Emphasis Filter (FIL3)

FIL3 is used to emphasize the stereo separation of stereo microphone recording data and playback data. Address 0FH, 10H, 11H, 12H and 13H (3-wire mode, COEW bit = "1"), and address 8FH, 90H, 91H, 92H and 93H (I^2C mode) set the filter coefficients of FIL3. FIL3 bit controls ON/OFF of the FIL3. When the stereo separation emphasis filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when PMPFIL bit = "0". The FIL3 starts operation 2/fs(max) after when FIL3 bit =PMPFIL bit= "1" is set.

1) In case of setting FIL3 as LPF

fs: Sampling Frequency
fc: Cutoff Frequency
κ: Gain ($0.25 \leq \kappa \leq 1$) * κ_{dB} [dB], $\kappa = 10^{\kappa dB/20}$
$\alpha = \sin(2\pi fc / fs) / 2Q$
Gain =20 log (Q)[dB] for fs. Normally Q should be set to 0.7071.

Register Setting (Register Map2) (Note 37)
A0: Register Addr = 0FH(3-wire mode), 8FH(I^2C mode)
A1: Register Addr = 10H(3-wire mode), 90H(I^2C mode)
A2: Register Addr = 11H(3-wire mode), 91H(I^2C mode)
B1: Register Addr = 12H(3-wire mode), 92H(I^2C mode)
B2: Register Addr = 13H(3-wire mode), 93H(I^2C mode)

$$A0 = A2 = \frac{1 - \cos(2\pi fc/fs)}{2} \times \frac{1}{1+\alpha} \times \kappa$$

$$A1 = \frac{1 - \cos(2\pi fc/fs)}{1+\alpha} \times \kappa$$

$$B1 = \frac{2\cos(2\pi fc/fs)}{1+\alpha}$$

$$B2 = \frac{\alpha - 1}{\alpha + 1}$$

Transfer Function

$$H_x(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 - B_1 z^{-1} - B_2 z^{-2}}$$

The cut-off frequency must be set as below.
fc / fs < 0.497

Setting Example) When fc=15kHz @ fs=44.1kHz. (I^2C mode)
A0 = 03D96B (hex): Addr. 8FH
A1 = 07B2D5 (hex): Addr. 90H
A2 = 03D96B (hex): Addr. 91H
B1 = F53F37 (hex): Addr. 92H
B2 = FBF575 (hex): Addr. 93H

(4) Gain Compensation (EQ0)

Gain compensation is used to compensate the frequency response and the gain that is changed by the stereo separation emphasis filter. Gain compensation is composed of the Equalizer (EQ0) and the Gain (0dB/+6dB/+12dB/+24dB). Address 19H ~ 1DH(3-wire mode, COEW bit = "1") and address 99H~9DH (I^2C mode) set the coefficient of EQ0. GN1-0 bits set the gain (Table 26). EQ0 bit controls ON/OFF of EQ0. When EQ is OFF and the gain is 0dB, the audio data passes this block by 0dB gain. The coefficient should be set when EQ0 bit = "0" or PMPFIL bit = "0". The EQ0 starts operation 2/fs(max) after when EQ0 bit =PMPFIL bit= "1" is set.

1) When EQ0 = High boost Filter

fs: Sampling Frequency

fc: Cutoff Frequency

$\beta = \sqrt{A / Q}$

A = boost gain. Example) Boost gain = +12dB ($A = 10^{\text{Gain [dB]} / 40}$) when A=2.

Gain =20 log (Q)[dB] for fs. Normally Q should be set to 0.7071.

Register Setting (Register Map 2) (Note 37)

A0: Register Addr = 19H(3-wire mode), 99H(I^2C mode)
A1: Register Addr = 1AH(3-wire mode), 9AH(I^2C mode)
A2: Register Addr = 1BH(3-wire mode), 9BH(I^2C mode)
B1: Register Addr = 1CH(3-wire mode), 9CH(I^2C mode)
B2: Register Addr = 1DH(3-wire mode), 9DH(I^2C mode)

$$A0 = \frac{A \times ((A+1) + (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs))}{(A+1) - (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs)}$$

$$A1 = \frac{-2A \times ((A-1) + (A+1) \times \cos(2\pi fc/fs))}{(A+1) - (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs)}$$

$$A2 = \frac{A \times ((A+1) - (A-1) \times \cos(2\pi fc/fs) - \beta \times \sin(2\pi fc/fs))}{(A+1) - (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs)}$$

$$B1 = \frac{-2 \times ((A-1) - (A+1) \times \cos(2\pi fc/fs))}{(A+1) - (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs)}$$

$$B2 = -\frac{(A+1) + (A-1) \times \cos(2\pi fc/fs) - \beta \times \sin(2\pi fc/fs))}{(A+1) - (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs)}$$

Transfer Function

$$H_x(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 - B_1 z^{-1} - B_2 z^{-2}}$$

The cut-off frequency must be set as below.

$fc_1 / fs < 0.497$

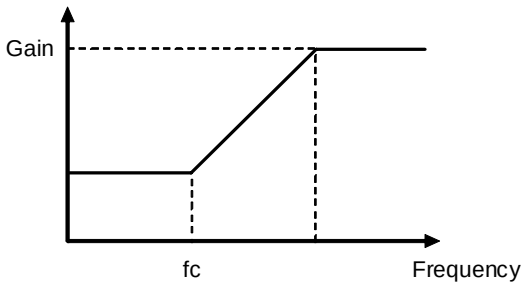


Figure 37. EQ0 Frequency Response (High –boost)

2) When EQ0 = Low boost Filter

fs: Sampling Frequency

fc: Cutoff Frequency

$\beta = \sqrt{A / Q}$

A = boost gain. Example) Boost gain = +12dB ($A = 10^{\text{Gain [dB]} / 40}$) when A=2.

Gain =20 log (Q)[dB] for fs. Normally Q should be set to 0.7071.

Register Setting (Register Map 2) (Note 37)

A0: Register Addr = 19H(3-wire mode), 99H(I^2C mode)

A1: Register Addr = 1AH(3-wire mode), 9AH(I^2C mode)

A2: Register Addr = 1BH(3-wire mode), 9BH(I^2C mode)

B1: Register Addr = 1CH(3-wire mode), 9CH(I^2C mode)

B2: Register Addr = 1DH(3-wire mode), 9DH(I^2C mode)

$$A0 = \frac{A \times ((A+1) + (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs))}{(A+1) + (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs)}$$

$$A1 = \frac{2A \times ((A+1) - (A+1) \times \cos(2\pi fc/fs)}{(A+1) + (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs)}$$

$$A2 = \frac{-A \times ((A+1) - (A-1) \times \cos(2\pi fc/fs) - \beta \times \sin(2\pi fc/fs))}{(A+1) + (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs)}$$

$$B1 = \frac{-2 \times ((A-1) - (A+1) \times \cos(2\pi fc/fs))}{(A+1) + (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs)}$$

$$B2 = \frac{(A+1) + (A-1) \times \cos(2\pi fc/fs) - \beta \times \sin(2\pi fc/fs))}{(A+1) + (A-1) \times \cos(2\pi fc/fs) + \beta \times \sin(2\pi fc/fs)}$$

Transfer Function

$$H_x(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 - B_1 z^{-1} - B_2 z^{-2}}$$

The cut-off frequency must be set as below.

$fc_1 / fs < 0.497$

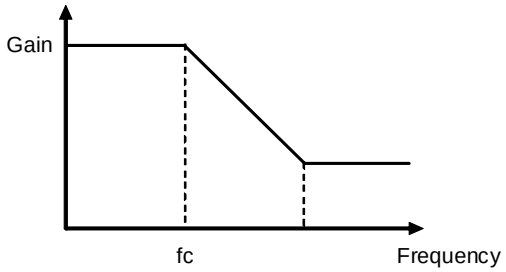


Figure 38. EQ0 Frequency Response (Low –boost)

GN1 bit	GN0 bit	Gain	
0	0	0dB	(default)
0	1	+6dB	
1	0	+12dB	
1	1	+24dB	

Table 26. Gain Select of the Gain Block

Setting Example) Gain Compensation EQ0: High-boost, fs=44.1kHz, fc= 3.5kHz, Q= 0.7071 (Gain =+3dB) (I^2C mode)

A0 =1565F1 (hex): Addr. 99H
A1 =E1A168 (hex): Addr. 9AH
A2 = 0C79DC (hex): Addr. 9BH
B1 = 14FCF9 (hex): Addr. 9CH
B2 = F781D1 (hex): Addr. 9DH

(3) 3-band Equalizer & 1-band Equalizer after ALC

This block can be used as equalizer or Notch Filter. 3-band equalizer (EQ2, EQ3, and EQ4) is switched ON/OFF independently by EQ2, EQ3, and EQ4 bits. ON/OFF switching of the equalizer after ALC (EQ1) is controlled by coefficients. When the equalizer is OFF, the audio data passes this block by 0dB gain. Address 6BH ~ 6FH (3-wire mode, COEW bit = "1") and address EBH~EFH (I^2C mode) set the coefficient of EQ1. Address 20H ~ 26H(3-wire mode, COEW bit = "1") and address A0H~A6H (I^2C mode) set the coefficient of EQ2. Address 29H ~ 2FH(3-wire mode, COEW bit = "1") and address A9H~AFH (I^2C mode) set the coefficient of EQ3. Address 32H ~ 36H(3-wire mode, COEW bit = "1") and address B2~B6H (I^2C mode) set the coefficient of EQ4. The EQx (x=1, 2, 3 or 4) coefficient must be set when PMPFIL bit = "0". EQ1-4 start operation 2/fs(max) after when EQx (x=1, 2, 3 or 4) = PMPFIL bit = "1" is set.

1) When EQ1 ~ EQ4 = Notch Filter
fs: Sampling Frequency
fo: Center Frequency
$\alpha = \sin(2\pi fc/fs) / 2Q$
A = boost gain Example) Boost gain = +12dB ($A = 10^{\text{Gain [dB]} / 40}$) when A=2
Q = fo/BW (BW: Band Width)

$$A0 = A2 = \frac{1}{1 + \alpha}$$

$$A1 = \frac{-2 \cos (2\pi fc/fs)}{1 + \alpha}$$

$$B1 = \frac{2 \cos (2\pi fc/fs)}{1 + \alpha}$$

$$B2 = -\frac{1 - \alpha}{1 + \alpha}$$

The cut-off frequency must be set as below.
EQ1, EQ4: $0.0625 < fo_n / fs < 0.497$
EQ2, EQ3: $fo_n / fs < 0.497$

2) When EQ1 ~ EQ4 = Dip boost Filter

fs: Sampling Frequency
fo: Center Furequency
$\alpha = \sin(2\pi fc/fs) / 2Q$
A = Boost gain Example) Boost gain = +12dB ($A = 10^{\text{Gain [dB]} / 40}$) when A=2.
Q = fo/BW (BW: Band Width)

$$A0 = \frac{A(1+\alpha A)}{A+\alpha}$$

$$A1 = \frac{-2A\cos(2\pi fc/fs)}{A+\alpha}$$

$$A2 = \frac{A(1-\alpha A)}{A+\alpha}$$

$$B1 = \frac{2A\cos(2\pi fc/fs)}{A+\alpha}$$

$$B2 = \frac{A-\alpha}{A+\alpha}$$

The cut-off frequency must be set as below.

EQ1, EQ4: $0.0625 < fo_n / fs < 0.497$
EQ2, EQ3: $fo_n / fs < 0.497$

Setting Example) EQ2 (Notch Filter) fs = 44.1kHz, fo = 8kHz, BW =200Hz (I_2C mode)
A0 = 0FD201 (hex): Addr. A0H
A1 = F2C80F (hex): Addr. A1H
A2 = 0FD201 (hex): Addr. A2H
B1 = 0D37F1 (hex): Addr. A3H, A5H
B2 = F05BFE (hex): Addr. A4H, A6H

Note 37.
[Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]

X = (Real number of filter coefficient calculated by the equations above) x 2^{20}

X should be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block when ALC bit is "1". When ADCPF bit is "1", the ALC circuit operates for recording path. When ADCPF bit is "0", the ALC circuit operates for playback path. ALC bit controls ON/OFF of ALC operation.

Note 38. In this section, VOL means IVL and IVR for recording path, OVL and OVR for playback path.
Note 39. In this section, REF means IREF for recording path, OREF for playback path.

1. ALC Limiter Operation

During ALC limiter operation, when either L or R channel output level exceeds the ALC limiter detection level (Table 27), the VOL value (L/R in common) is attenuated automatically to the level under ALC recovery counter reset level. The attenuate amount is depends on output level (Table 28). The volume is attenuated by the amount (L/R in common) shown in Table 28 in every one sampling. (When ALC limiter operation is executed, this attenuate operation is repeated for 16 times.)

After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds ALC limiter detection level.

LMTH1 bit	LMTH0 bit	ALC Limiter Detection Level (LM LEVEL)	ALC Recovery Counter Reset Level	
0	0	–2.5dBFS	–4.1dBFS	(default)
0	1	–4.1dBFS	–6.0dBFS	
1	0	–6.0dBFS	–8.5dBFS	
1	1	–8.5dBFS	–12dBFS	

Table 27. ALC Limiter Detection Level / Recovery Counter Reset Level

Output level	ATT Amount [dB]
Output Level (*) >= +0.53dBFS	0.38142
–1.16dBFS < Output Level < +0.53dBFS	0.06812
LM LEVEL < Output Level < –1.16dBFS	0.02548

(*) Compare with the next output data

Table 28. ALC Limiter ATT Amount

2. ALC Recovery Operation

ALC recovery operation waits for the time set by WTM1-0 bits (Table 29) after completing ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 27) during the wait time, ALC recovery operation is executed. The VOL value is automatically incremented by the amount set by RGAIN2-0 bits (Table 30) up to the set reference level (Table 31) in every one sampling. When the VOL value exceeds the reference level (REF7-0), the VOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

ALC operations correspond to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to a microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 33).

WTM1 bit	WTM0 bit	Recovery Wait Time
0	0	128/fs
0	1	256/fs
1	0	512/fs
1	1	1024/fs

Table 29. ALC Recovery Operation Waiting Period

RGAIN2 bit	RGAIN1 bit	RGAIN0 bit	GAIN Amount [dB]	
0	0	0	0.0042	(default)
0	0	1	0.0021	
0	1	0	0.0011	
0	1	1	0.0005	
1	0	0	0.0003	
1	0	1	0.0001	
1	1	0	0.00007	
1	1	1	0.00003	

Table 30. ALC Recovery GAIN Amount

IREF7-0 bits	GAIN [dB]	Step	
F0H	+35.625	0.375 dB	
EFH	+35.25		
:	:		
E1H	+30.0		(default)
:	:		
92H	+0.375		
91H	0.0		
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 31. Reference Level of ALC Recovery Operation for Recoding

OREF7-0 bits	GAIN [dB]	Step	
F0H	+35.625	0.375 dB	
EFH	+35.25		
:	:		
E1H	+30.0		(default)
:	:		
92H	+0.375		
91H	0.0		
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 32. Reference Level of ALC Recovery Operation for Playback

RFST1-0 bits	Fast Recovery GAIN Amount [dB]
00	0.0032
01	0.0042
10	0.0064
11	0.0127

Table 33. Fast Recovery Gain Setting

3. The Volume at ALC Operation

The volume value during ALC operation is reflected in VOL7-0 bits. It is possible to check the current volume by reading the register value of VOL7-0 bits.

VOL7-0 bits	GAIN [dB]	VOL7-0 bits	GAIN [dB]
EDH	+34.5 ≤ Gain ≤ +35.625	7DH	–7.5 ≤ Gain < –6.0
E9H	+33.0 ≤ Gain < +34.5	79H	–9.0 ≤ Gain < –7.5
E5H	+31.5 ≤ Gain < +33.0	75H	–10.5 ≤ Gain < –9.0
E1H	+30.0 ≤ Gain < +31.5	71H	–12.0 ≤ Gain < –10.5
DDH	+28.5 ≤ Gain < +30.0	6DH	–13.5 ≤ Gain < –12.0
D9H	+27.0 ≤ Gain < +28.5	69H	–15.0 ≤ Gain < –13.5
D5H	+25.5 ≤ Gain < +27.0	65H	–16.5 ≤ Gain < –15.0
D1H	+24.0 ≤ Gain < +25.5	61H	–18.0 ≤ Gain < –16.5
CDH	+22.5 ≤ Gain < +24.0	5DH	–19.5 ≤ Gain < –18.0
C9H	+21.0 ≤ Gain < +22.5	59H	–21.0 ≤ Gain < –19.5
C5H	+19.5 ≤ Gain < +21.0	55H	–22.5 ≤ Gain < –21.0
C1H	+18 ≤ Gain < +19.5	51H	–24.0 ≤ Gain < –22.5
BDH	+16.5 ≤ Gain < +18	4DH	–25.5 ≤ Gain < –24.0
B9H	+15.0 ≤ Gain < +16.5	49H	–27.0 ≤ Gain < –25.5
B5H	+13.5 ≤ Gain < +15.0	45H	–28.5 ≤ Gain < –27.0
B1H	+12.0 ≤ Gain < +13.5	41H	–30.0 ≤ Gain < –28.5
ADH	+10.5 ≤ Gain < +12.0	3DH	–31.5 ≤ Gain < –30.0
A9H	+9.0 ≤ Gain < +10.5	39H	–33.0 ≤ Gain < –31.5
A5H	+7.5 ≤ Gain < +9.0	35H	–34.5 ≤ Gain < –33.0
A1H	+6.0 ≤ Gain < +7.5	31H	–36.0 ≤ Gain < –34.5
9DH	+4.5 ≤ Gain < +6.0	2DH	–37.5 ≤ Gain < –36.0
99H	+3.0 ≤ Gain < +4.5	29H	–39.0 ≤ Gain < –37.5
95H	+1.5 ≤ Gain < +3.0	25H	–40.5 ≤ Gain < –39.0
91H	0 ≤ Gain < +1.5	21H	–42.0 ≤ Gain < –40.5
8DH	–1.5 ≤ Gain < 0	19H	–45.0 ≤ Gain < –42.0
89H	–3.0 ≤ Gain < –1.5	11H	–48.0 ≤ Gain < –45.0
85H	–4.5 ≤ Gain < –3.0	01H	–54.0 ≤ Gain < –48.0
81H	–6.0 ≤ Gain < –4.5	0H	MUTE

Table 34. Value of VOL7-0 bits

4. Example of ALC Setting

Table 35 and Table 36 show the examples of the ALC setting for recording and playback path.

Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
WTM1-0	Recovery waiting period	01	32ms	11	21.3ms
IREF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
RGAIN2-0	Recovery GAIN	011	0.0005dB	011	0.0005dB
RFST1-0	Fast Recovery GAIN	00	0.0032dB	00	0.0032dB
ALC	ALC enable	1	Enable	1	Enable

Table 35. Example of the ALC Setting (Recording)

Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
WTM1-0	Recovery waiting period	01	32ms	11	21.3ms
OREF7-0	Maximum gain at recovery operation	A1H	+6dB	A1H	+6dB
OVL7-0, OVR7-0	Gain of IVOL	91H	0dB	91H	0dB
RGAIN2-0	Recovery GAIN	011	0.0005dB	011	0.0005dB
RFST1-0	Fast Recovery GAIN	00	0.0032dB	00	0.0032dB
ALC	ALC enable	1	Enable	1	Enable

Table 36. Example of the ALC Setting (Playback)

5. Example of registers set-up sequence of ALC Operation

The following registers must not be changed during ALC operation. These bits must be changed after ALC operation is finished by ALC bit= "0". The volume is changed in soft transition until the AK4950 becomes manual mode after ALC bit is set to "0".

LMTH1-0, WTM1-0, RGAIN 2-0, IREF7-0, OREF7-0, RFST1-0 bits

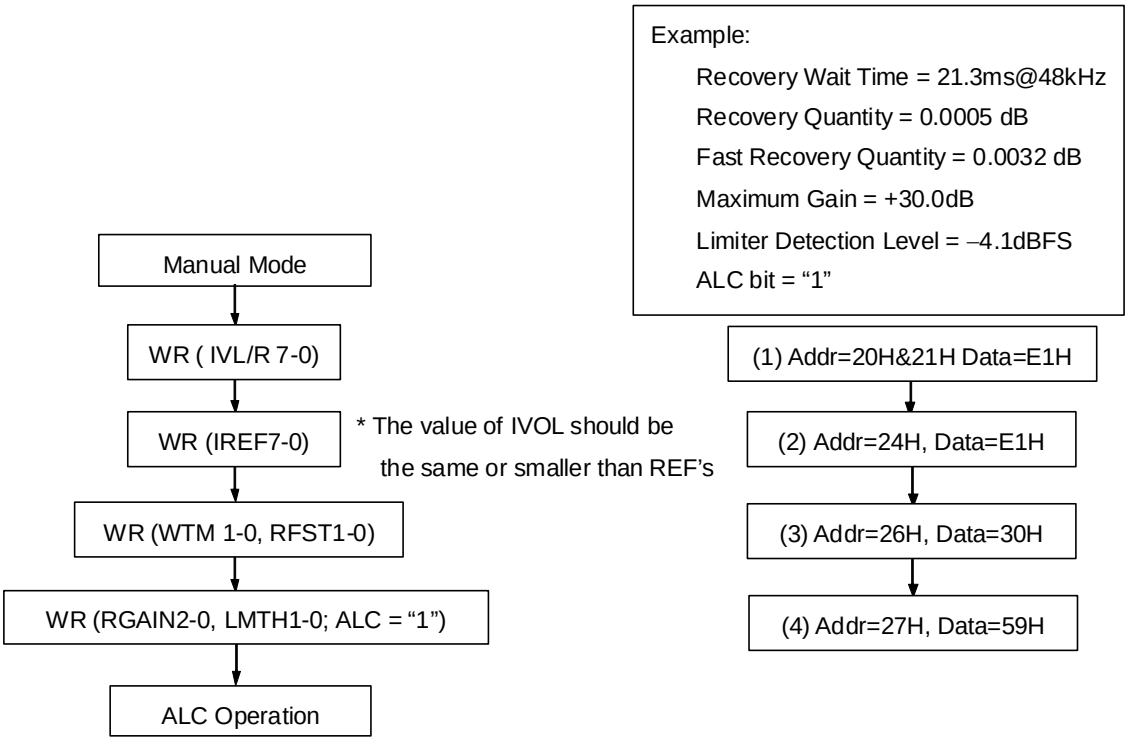


Figure 39. Registers Set-up Sequence at ALC1 Operation (recording path)

■ Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode at ALC bit = "0" when ADCPF bit ="1". This mode is used in the case shown below.

1. After exiting reset state, when setting up the registers for ALC operation (LMTH and etc.)
2. When the registers for ALC operation (Limiter period, Recovery period and etc.) are changed. For example; when the sampling frequency is changed.
3. When IVOL is used as a manual volume control.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 37). When the IVOL value is changed, the transition is executed via soft changes. The transition time between set values is 10ms@fs =44.1kHz. L and R channel volumes are set individually by IVL7-0 and IVR7-0 bits when IVOLC bit = "0". IVL7-0 bits control both L and R channel volumes together when IVOLC bit = "1".

IVL7-0 bits IVR7-0 bits	GAIN [dB]	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		
E0H	+29.625		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54		
00H	MUTE		

Table 37. Input Digital Volume Setting

If IVL7-0 or IVR7-0 bits are written during PMPFIL bit = "0", IVOL operation starts with the written values after PMPFIL bit is changed to "1".

When changing ADCPF bit, the volume value is changed to OVL/R(IVL/R) from IVL/R(OVL/R). The switching noise can be reduced by setting into soft mute sate (SMUTE bit = "1") before changing ADCPF bit.

■ Output Digital Volume (Manual Mode)

The ALC block becomes output digital volume (manual mode) by setting ALC bit to "0" when PMPFIL = PMDAC bits = "1" and ADCPF bit is "0". The output digital volume gain is set by the OVL7-0 bit and the OVR7-0 bit (Table 38). When the OVOLC bit = "1", the OVL7-0 bits control both L and R channel volume levels. When the OVOLC bit = "0", the OVL7-0 bits control L channel volume level and the OVR7-0 bits control R channel volume level. The volume change is executed via soft transition. The transition time between set values is 10ms@fs =44.1kHz. When changing ADCPF bit, the volume value is changed to OVL/R(IVL/R) from IVL/R(OVL/R). The switching noise can be reduced by setting into soft mute sate (SMUTE bit = "1") before changing ADCPF bit.

OVL7-0 bits OVR7-0 bits	GAIN [dB]	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 38. Output Digital Volume Setting

■ Output Digital Volume 2

The volume of both L and R channels are controlled together by the DVL7-0. Setting values are shown in Table 39. The volume change is executed via soft transition. It can be changed during ALC operation. The transition time between set values is 10ms@fs =44.1kHz.

DVOL7-0 bits	GAIN [dB]	Step	
F1H	+18.0	0.375dB	
F0H	+17.625		
EFH	+17.25		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	-0.375		
:	:		
2H	-71.625		
1H	-72.0		
0H	MUTE		

Table 39. Output Digital Volume2 Setting

■ Digital HPF1

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies of the HPF1 are set by HPFC1-0 bits (Table 40). It is proportional to the sampling frequency (fs) and default is 3.4Hz (@fs = 44.1kHz). HPFAD bit controls the ON/OFF of the HPF1 (HPF ON is recommended).

HPFC1 bit	HPFC0 bit	fc			
		fs=44.1kHz	fs=22.05kHz	fs=8kHz	
0	0	3.4Hz	1.7Hz	0.62Hz	(default)
0	1	13.6Hz	6.8Hz	2.47Hz	
1	0	108.8Hz	54.4Hz	19.7Hz	
1	1	217.6Hz	108.8Hz	39.5Hz	

Table 40. HPF1 Cut-off Frequency

■ De-emphasis Filter

The AK4950 includes a digital de-emphasis filter (tc = 50/15μs) which corresponds three kinds frequency (32kHz, 44kHz, 48kHz) by IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter (Table 41).

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 41. De-emphasis Control

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is set "1", the output signal is attenuated to -∞ in 10ms@fs =44.1kHz. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the value set by DVOL7-0 bits from -∞ in 10ms@fs =44.1kHz. If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and the volume returns to the level set by DVOL7-0 bits in the same cycle. The soft mute function is effective for changing signal source without stopping the signal transmission at playback path. SMUTE bit is invalid during an ALC operation.

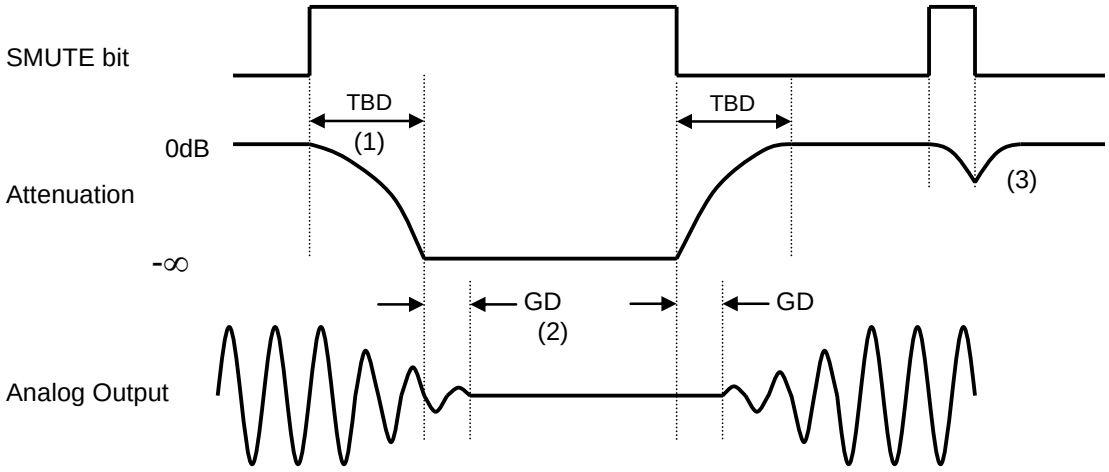


Figure 40. Soft Mute Function

(1) The input signal is attenuated to –∞ ("0") during 10ms@fs =44.1kHz.
(2) Analog output corresponding to digital input has group delay (GD).
(3) If soft mute is cancelled before attenuating to –∞, the attenuation is discounted and returned to the level set by DVOL7-0 bits within the same cycle.

■ Stereo Line Output (LOUT, ROUT pin)

When PMBP bit = "0", PMLO bit= "1" and DACL bit is set to "1", L and R channel signals of DAC are output in single-ended format from the LOUT and ROUT pins. When DACL bit is "0", output signals are muted and LOUT and ROUT pins output common voltage. The load impedance is 10kΩ (min.). When the PMLO bit = LOPS bit = "0", the stereo line output enters power-down mode and the output is pulled-down to VSS1 by 100kΩ(typ). When the LOPS bit is "1", stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO bit when LOPS bit = "1". In this case, output signal line should be pulled-down by 20kΩ after AC coupled as Figure 42. Rise/Fall time is 300ms (max) if C=1μF and R_L=10kΩ. When PMLO bit = "1" and LOPS bit = "0", stereo line output is in normal operation.

LOVL1-0 bits set the gain of stereo line output.

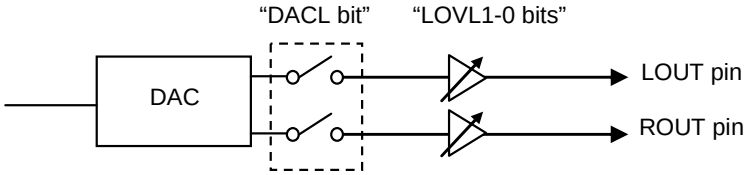


Figure 41. Stereo Line Output

LOPS	PMLO	Mode	LOUT/ROUT pin	
0	0	Power Down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power Save	Fall down to VSS1	
	1	Power Save	Rise up to Common Voltage	

Table 42. Stereo Line Output Mode Select

LOVL1-0 bits	AVDD	Gain	
00	2.7 ~ 3.6 V	0dB	
01	3.0 ~ 3.6 V	+1.34dB	(default)
10	2.7 ~ 3.6 V	+2dB	
11	3.0 ~ 3.6 V	+3.34dB	

Table 43. Stereo Lineout Volume Setting

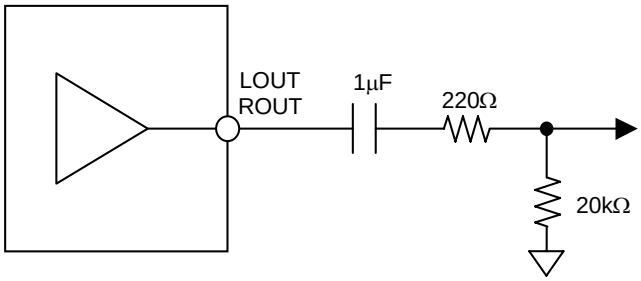


Figure 42. External Circuit for Stereo Line Output (in case of using a Pop Noise Reduction Circuit)

[Stereo Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)]

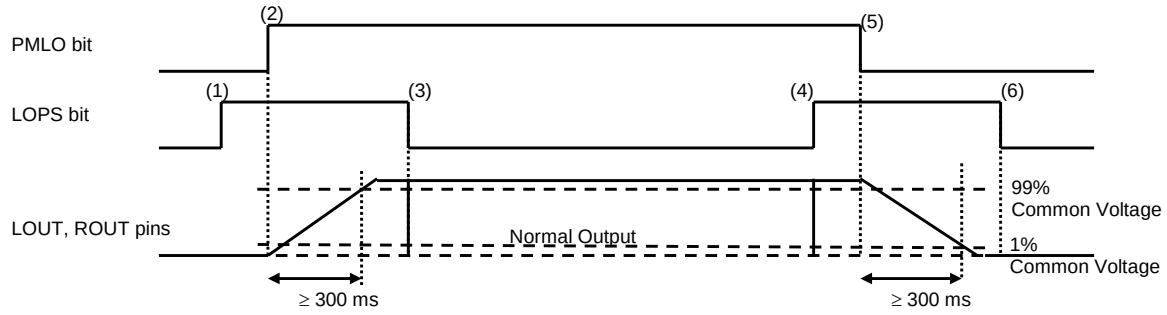


Figure 43. Stereo Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)

(1) Set LOPS bit = "1". Stereo line output enters the power-save mode.
(2) Set PMLO bit = "1". Stereo line output exits the power-down mode.
LOUT and ROUT pins rise up to common voltage. Rise time is 200ms (max 300ms) when C=1μF.
(3) Set LOPS bit = "0" after LOUT and ROUT pins rise up. Stereo line output exits the power-save mode.
Stereo line output is enabled.
(4) Set LOPS bit = "1". Stereo line output enters power-save mode.
(5) Set PMLO bit = "0". Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to 1% of the common voltage. Fall time is 200ms (max 300ms) at C=1μF.
(6) Set LOPS bit = "0" after LOUT and ROUT pins fall down. Stereo line output exits the power-save mode.

< Mono Mixing Output >

Mono mixing outputs are available by setting MONO1-0 bits. Input data from the SDTI pin can be converted to mono signal [(L+R)/2] and are output via LOUT and ROUT pins. (Figure 32)

MONO1 bit	MONO0 bit	LOUT pin	ROUT pin	
0	0	Lch	Rch	(default)
0	1	Lch	Lch	
1	0	Rch	Rch	
1	1	(Lch+Rch)/2	(Lch+Rch)/2	

Table 44. LOUT/ROUT pin Output Data Switch

■ Line Sharing of Mic Input and Stereo Lineout in External Circuit (LIN1/RIN1, LOUT/ROUT pin)

The LIN1 (or RIN1) pin and the LOUT (or ROUT) pin of the AK4950 can share a line in external circuit. When using the LIN1(or RIN1) pin as ADC input, the LOUT(or ROUT) pin is pulled up (typ. 200kΩ) to typ. 1.35V* by setting PMADC= LOPS= EXTC bits= "1". When using the LOUT (or ROUT) pin as DAC output, the LIN1 (or RIN1) pin is pulled up (typ. 100kΩ) to typ. 1.35V* by setting PMADC=LOPS bits = "0" and EXTC bit = "1".

PMADC bit	LOPS bit (PMLO bit = "1")	EXTC bit	LIN1/RIN1 pins	LOUT/ROUT pins	Figure
1	1	1	Normal Operation	Pull-up to typ. 1.35V (*) by 200kΩ (typ)	Figure 44
1	0	1	Normal Operation	Normal Operation	-
0	1	1	Pull-up to typ. 1.35V (*) by 100kΩ (typ)	Pull-up toR typ. 1.35V (*) by 200kΩ (typ)	-
0	0	1	Pull-up to typ. 1.35V (*) by 100kΩ (typ)	Normal Operation	Figure 45
x	x	0	Can Not Share a Line		-

Table 45. LIN1/RIN1 and LOUT/ROUT Mode Setting (x: Don't care)

* When LOVL0 bit = "0". 1.43V (typ) if the LOVL0 bit = "1"

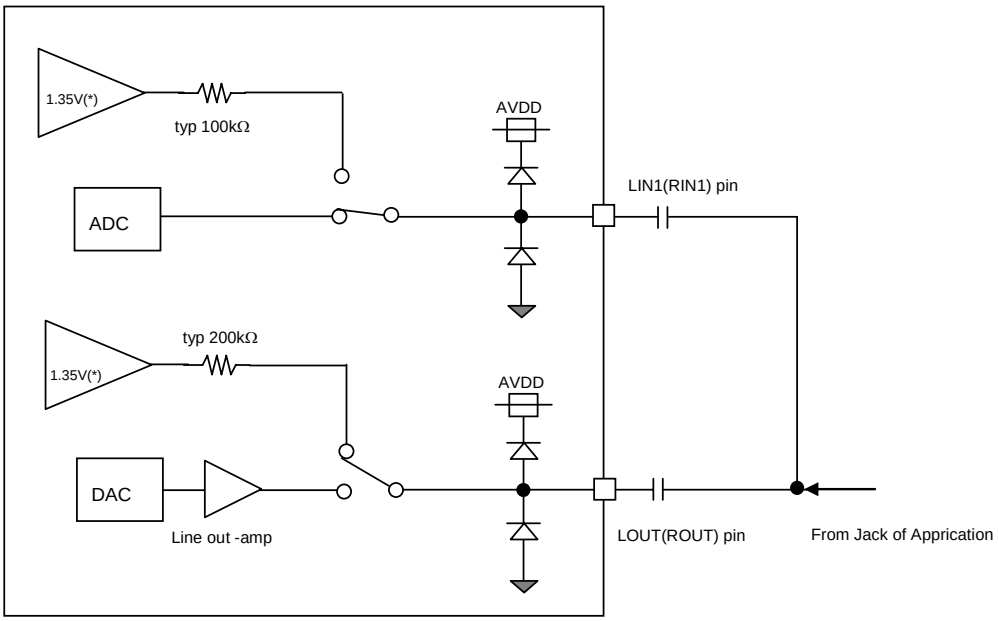


Figure 44. LIN1/RIN1→ADC path: External Line Share
(PMADC = LOPS = EXTC bits = "1")

* When LOVL0 bit = "0". 1.43V (typ) if the LOVL0 bit = "1"

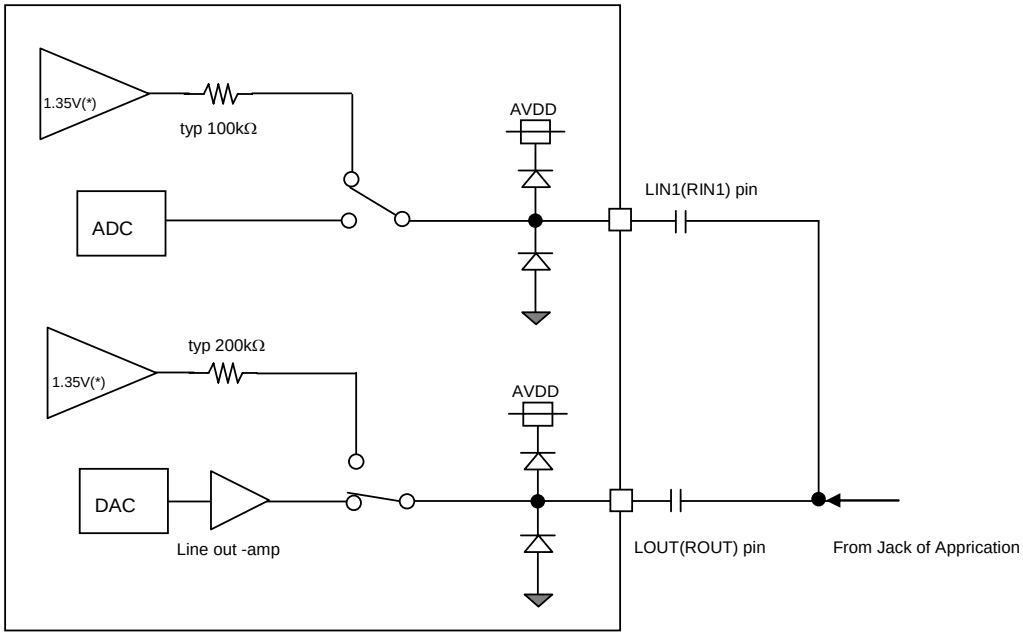


Figure 45. DAC→ LOUT/ROUT path: External Line Share
(PMADC = LOPS bits = "0", EXTC bits = "1")

* When LOVL0 bit = "0". 1.43V (typ) if the LOVL0 bit = "1"

■ Rch Line Output and Analog Mix Mono Input Modes Select

When PMBP bit = "0", the ROUT/MIN pin outputs right channel signal of DAC (ROUT pin mode). When PMBP bit = "1", the ROUT/MIN pin becomes mono input pin (MIN pin mode).

PMLO bit	PMBP bit	ROUT/MIN pin mode	
1	0	ROUT pin mode	(default)
x	1	MIN pin mode	

* MIN pin mode when PMLO = PMBP bits = "1"

Table 46. ROUT/MIN pin Mode Select (x: Don't care)

During PMBP bit = "1", the speaker amplifier outputs input data of the MIN pin by setting BEEPS bit to "1". The lineout amplifier outputs input signal of the MIN pin by setting BEEPL bit to "1". When BPM bit = "1", Ri can control the BEEP signal gain which is in inverse proportion to Ri resister value. Table 48 and Table 49 show the typical gain when R_i = 66kΩ. The external R_i resister is not needed when BPM bit = "0". The total gain is dependent on MIN-Amp gain which is set by BPLVL2-0 bits, speaker amplifier gain (SPKG1-0 bits) and stereo lineout amplifier gain (LOVL1-0 bits).

BPM bit	BEEP Mode	
1	External Resistance Mode	
0	Internal Resistance Mode	(default)

Table 47. BEEP Mode Setting

1. External Resistance Mode (BPM bit = "1")

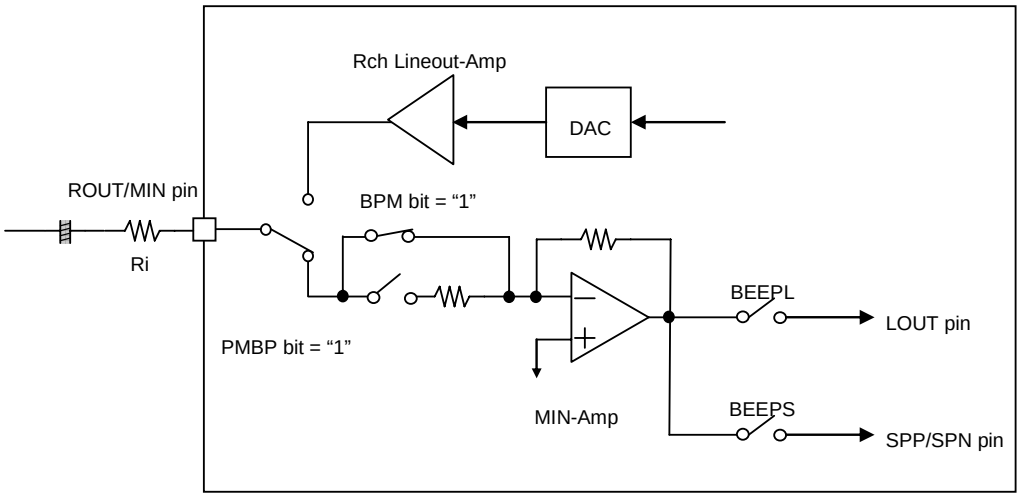


Figure 46. Block Diagram of MIN pin (PMBP bit = "1", BPM bit ="1")

LOVL1-0 bits	MIN → LOUT	
00	0dB	(default)
01	+1.34dB	
10	+2dB	
11	+3.34dB	

Table 48. MIN → LOUT Output Gain

SPKG1-0 bits	MIN → SPP/SPN		
	ALC bit = "0"	ALC bit = "1"	
00	+6.1dB	+8.1dB	(default)
01	+8.1dB	+10.1dB	
10	+10.1dB	+12.1dB	
11	+12.1dB	+14.1dB	

Table 49. MIN → SPK Output Gain

2. Internal Resistance Mode (BPM bit = "0")

BPLVL2	BPLVL1	BPLVL0	BEEP Gain	
0	0	0	0dB	(default)
0	0	1	–6dB	
0	1	0	–12dB	
0	1	1	–24dB	
1	0	0	–28dB	
1	0	1	–32dB	
1	1	0	–36dB	
1	1	1	–40dB	

Table 50. BEEP Output Gain Setting when BPM bit = "0"

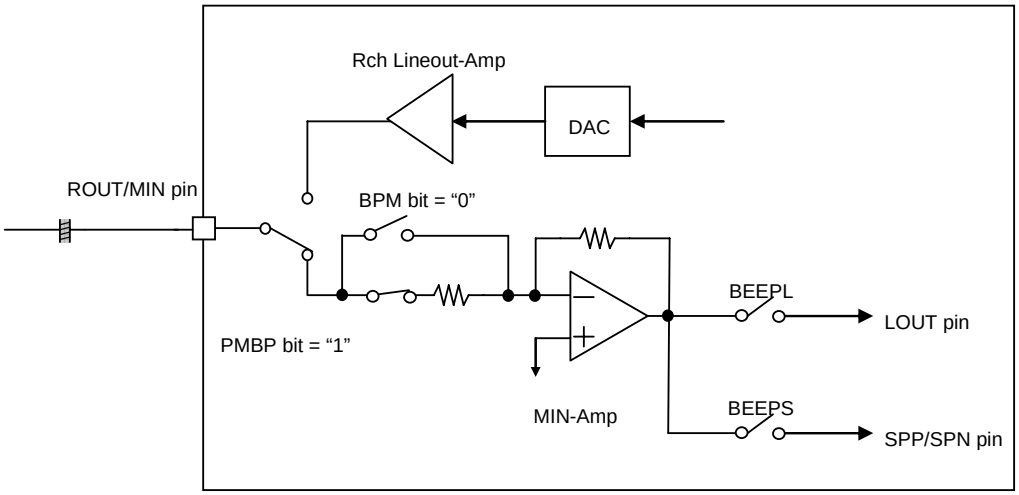


Figure 47. Block Diagram of MIN pin (PMBP bit = "1", BPM bit ="0")

■ Speaker Output

The DAC output signal is input to the speaker amplifier as mono signal [(L+R)/2]. The speaker amplifier has mono output as it is BLT (Bridged Transless) capable. The gain and output level are set by SPKG1-0 bits. The output level is depends on AVDD and SPKG1-0 bits setting.

SPKG1-0 bits	Gain		
	ALC bit = "0"	ALC bit = "1"	
00	+6.1dB	+8.1dB	(default)
01	+8.1dB	+10.1dB	
10	+10.1dB	+12.1dB	
11	+12.1dB	+14.1dB	

Table 51. SPK-Amp Gain

SPKG1-0 bits	SPK-Amp Output (DAC Input=0dBFS, AVDD= 3.3V)		
	ALC bit = "0"	ALC bit = "1" (LMTH1-0 bits = "00")	
00	3.37Vpp	3.17Vpp	(default)
01	4.23Vpp (Note 40)	4.00Vpp	
10	5.33Vpp (Note 40)	5.04Vpp (Note 40)	
11	6.71Vpp (Note 40)	6.33Vpp (Note 40)	

Note 40. The output level is calculated on the assumption that the signal is not clipped. However, in the actual case, the SPK-Amp output signal is clipped when DAC outputs 0dBFS signal. The SPK-Amp output level should be kept under 4.0Vpp (AVDD=3.3V) by adjusting digital volume to prevent clipped noise.

Table 52. SPK-Amp Output Level

< Speaker-Amp Control Sequence >

The speaker amplifier is powered-up/down by PMSPK bit. When PMSPK bit is "0", both SPP and SPN pins are in Hi-Z state. When PMSPK bit is "1" and SPPSN bit is "0", the speaker amplifier enters power-save mode. In this mode, the SPP pin is placed in Hi-Z state and the SPN pin outputs AVDD/2 voltage.

When the PMSPK bit is "1" after the PDN pin is changed from "L" to "H", the SPP and SPN pins rise up in power-save mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to AVDD/2 voltage. Because the SPP and SPN pins rise up in power-save mode, pop noise can be reduced. When the AK4950 is powered-down (PMSPK bit = "0"), pop noise can also be reduced by first entering power-save-mode.

PMSPK	SPPSN	Mode	SPP	SPN	
0	x	Power-down	Hi-Z	Hi-Z	(default)
1	0	Power-save	Hi-Z	AVDD/2	
	1	Normal Operation	Normal Operation	Normal Operation	

Table 53 Speaker-Amp Mode Setting (x: Don't care)

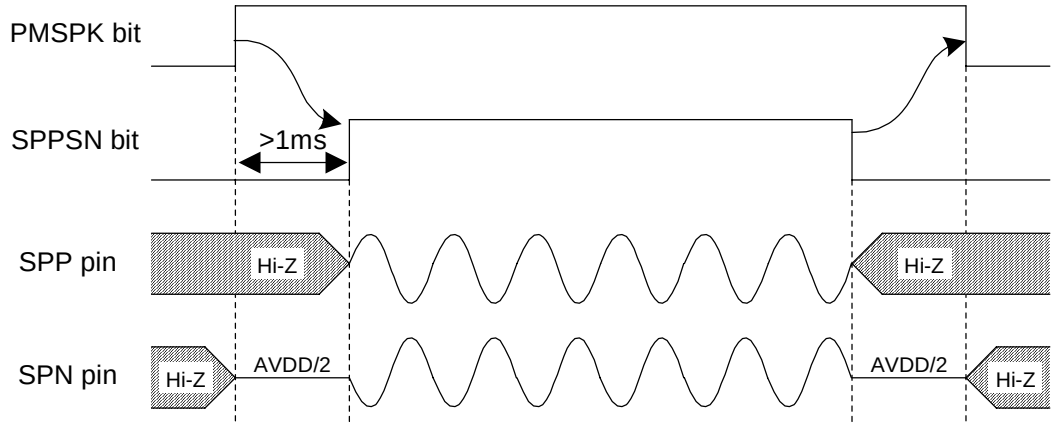


Figure 48. Power-up/Power-down Timing for Speaker-Amp

■ Thermal Shutdown Function

When the internal temperature of the device rises up irregularly (E.g. When output pins are shortened.), the speaker amplifier is automatically powered down and then THDET bit becomes "1"(thermal shutdown). When the thermal shutdown is executed, the speaker amplifier, lineout amplifier, charge pump and video block are powered-down (PMSPK=PMLO=PMCP=PMV bits = "1" → "0"). Writing "1" to these registers can put each circuit in normal operation, but it may be powered down again ("1" → "0") if the internal temperature of the device is still high. The device status can be monitored on THDET bit.

■ Video Block

The integrated cap-less video amplifier with charge pump has drivability for a load resistance of 150Ω (Figure 49). The AK4950 has a composite input and output. A Low Pass Filter (LPF) and Gain Control Amp are integrated, and VG1-0 bits set the gain (+6/+9/+12/16.5 dB) (Table 54). The video signals can be output as pedestal level 0V by supplying negative power to the video amplifier from the charge pump circuit (Figure 50). Therefore AC-coupling capacitor is not needed. And also, the external flying capacitor for charge pump is not needed because it is included. The video amplifier power management is controlled by PMV bit. The charge pump circuit power management is controlled by PMCP bit. When PMV bit = "0", the VOUT pin outputs 0V. The video inputs must be AC-coupled by a 0.1µF capacitor. The video signal source impedance at transmitting side must not over 600Ω.

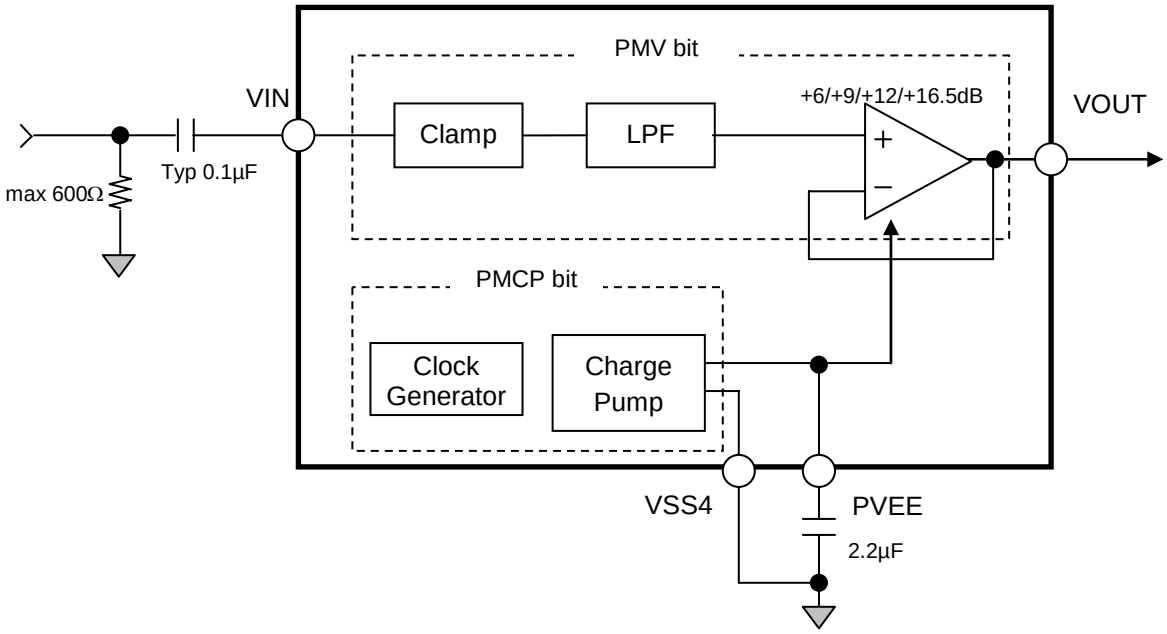


Figure 49. Video Block Diagram

VG1-0 bits	GAIN	
00	+6dB	(default)
01	+9dB	
10	+12dB	
11	+16.5dB	

Table 54. Video Signal Gain Setting

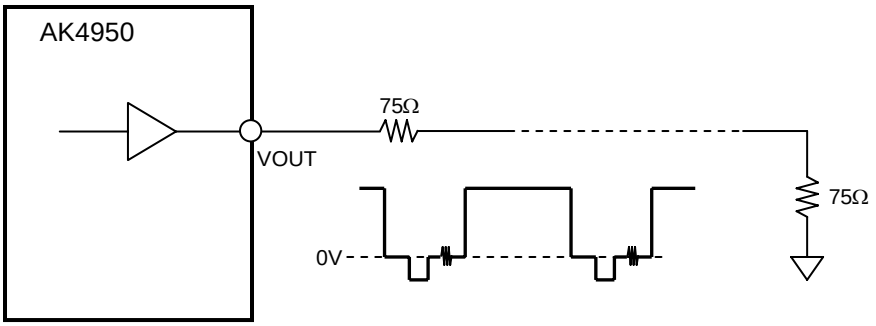


Figure 50. Video Signal Output

■ Regulator Block

The AK4950 integrates two regulators. The 3.3V (typ) power supply voltage from the AVDD pin is converted to 2.3V (typ) by the regulator 1 and supplied to the analog logic (MIC-Amp, ADC, DAC, MIN, Video-Amp input stage, LPF of video block and charge pump). It is also converted to 1.8V (typ) by the regulator 2 and supplied to the digital logic (digital core block). Each regulator is powered up by the PDN pin = "H", and powered down by the PDN pin = "L". Connect a 2.2μF (± 50%) capacitor to the REGFIL1 pin and a 1.0μF (± 50%) capacitor to the REGFIL2 pin to reduce noise on AVDD.

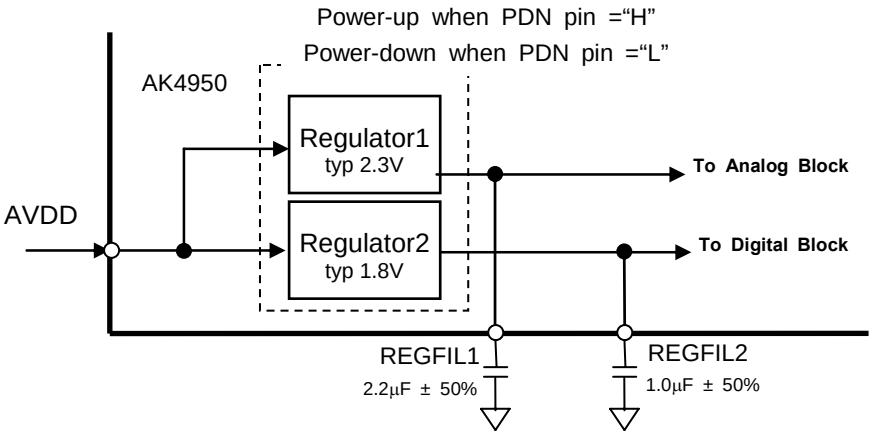


Figure 51 Regulator Block

■ Serial Control Interface

(1) 3-wire Mode

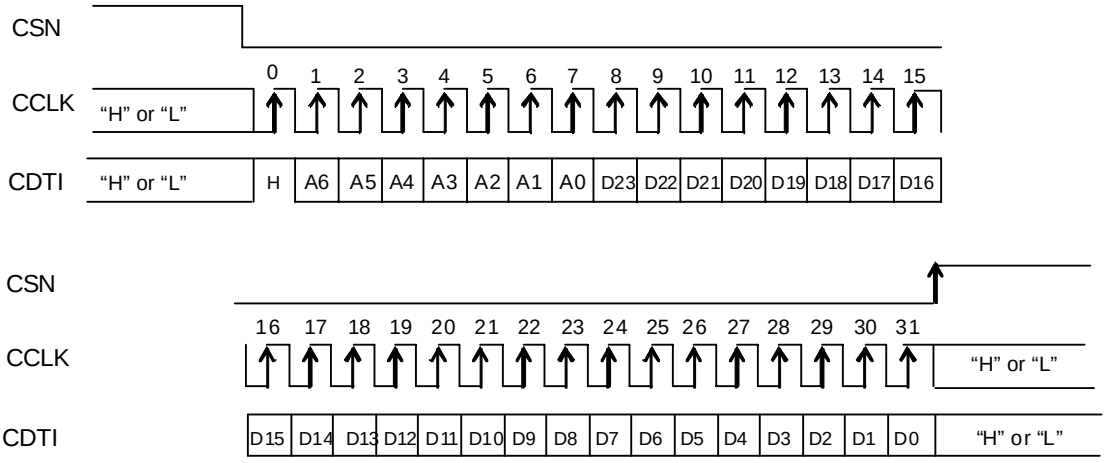
Internal registers may be written by using 3-wire mode interface pins (CSN, CCLK and CDTIO). The data on this interface consists of Read/Write, Register address (MSB first, 7bits) and Control or Output data (MSB first, 24bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge.

Data writings become available on the rising edge of CSN. When reading the data, the CDTIO pin changes to output mode at the falling edge of 8th CCLK and outputs data in D23-D0. However this reading function is available only when READ bit = "1". When READ bit = "0", the CDTIO pin stays as Hi-Z even after the falling edge of 8th CCLK. The data output finishes on the rising edge of CSN. The CDTIO is placed in a Hi-Z state except when outputting the data at read operation mode. Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by the PDN pin = "L".

The registers on the address after 20H are for CRAM of the DSP. Writing data is automatically stored in CRAM when COEW bit is "1" (Figure 53). In this case, PMPFIL bit should be set to "0". Read commands are not valid.

Note 41. Data reading is only available on the following addresses; 00 ~ 0FH and 20H ~ 2FH. When reading the other addresses, the register values are invalid.

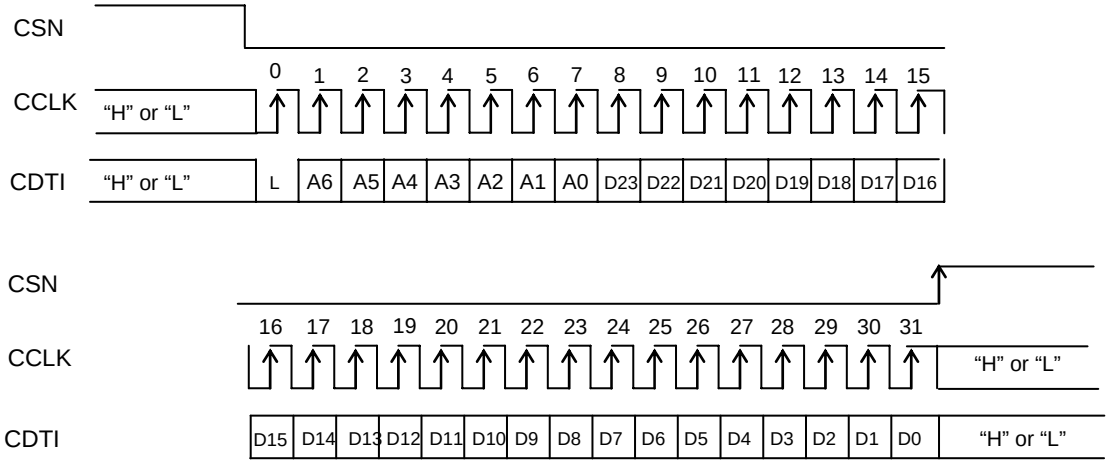
(1)-1. When accessing to the address 00H ~ 2FH (COEW bit = "0")



A6-A0: Register Address
D23-D0: Control data (Input) at Write Command (Write only)

Figure 52. 3-wire Mode Control Interface Timing (COEW bit = "0")

(1)-2. When accessing to filter coefficients (COEW bit = "1")



A6-A0: Register Address
D23-D0: Control data (Input) at Write Command (Write only)

Figure 53. 3-wire Mode Control Interface Timing (COEW bit = "1")

(2) I2C-bus Control Mode (I2C pin = "H")

The AK4950 supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to (TVDD+0.3)V or less voltage.

(2)-1. WRITE Operations

Figure 54 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 62). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001001". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets these device address bits (Figure 56). If the slave address matches that of the AK4950, the AK4950 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 63). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4950 and the format is MSB first. (Figure 57). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 58). The AK4950 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 62).

The AK4950 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4950 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 2FH prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 64) except for the START and STOP conditions.

The data length is different (8bit or 24bit) depending on the data address.

Address	Data length
00H ~ 2FH	8bit
80H ~ FFH	24bit

Table 55. Data Length in I²C-bus Mode

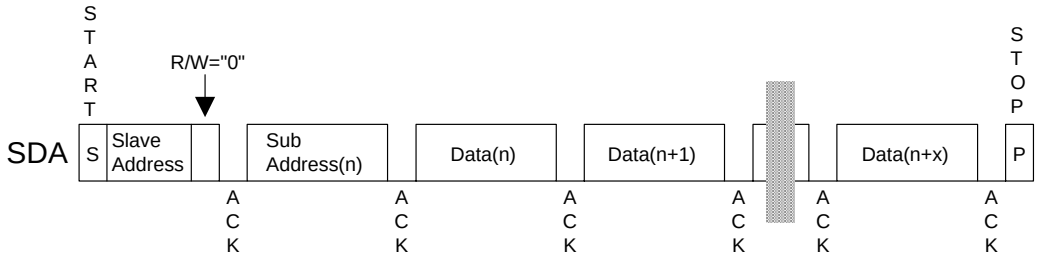


Figure 54. Data Transfer Sequence at I²C Bus Mode (00H ~ 2FH)

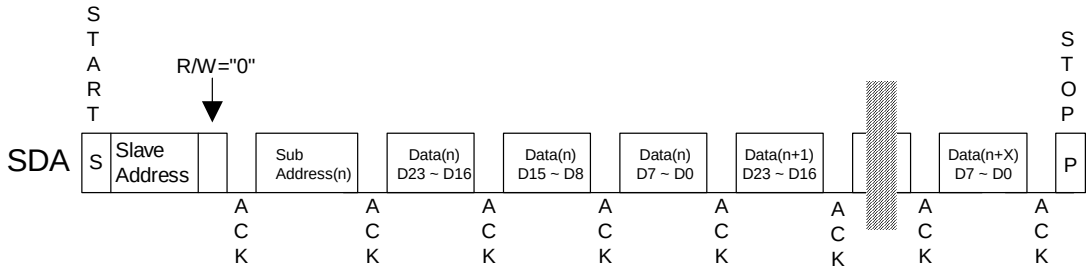


Figure 55. Data Transfer Sequence at I^2C Bus Mode (80H ~ FEH)

0	0	1	0	0	1	CAD0	R/W

Figure 56. The First Byte

A7	A6	A5	A4	A3	A2	A1	A0

Figure 57. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 58. The Third Byte (00H ~ 2FH)

D23	D22	D21	D20	D19	D18	D17	D16
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Figure 59. The Third Byte (80H ~ FEH)

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4950. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 2FH prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4950 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.
However, the AK4950 only supports RANDOM ADDRESS READ in DSP mode.

(2)-2-1. CURRENT ADDRESS READ

The AK4950 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4950 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4950 ceases the transmission.

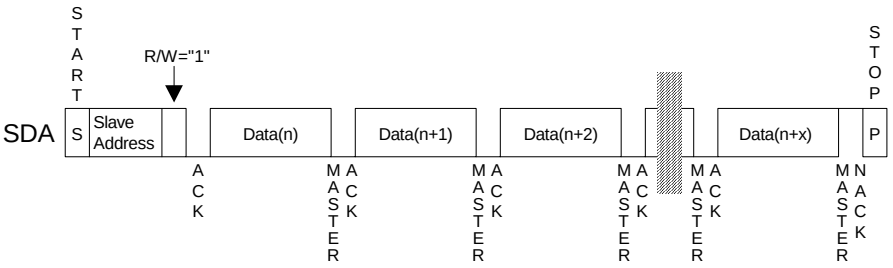


Figure 60. Current Address Read

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4950 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4950 ceases the transmission.

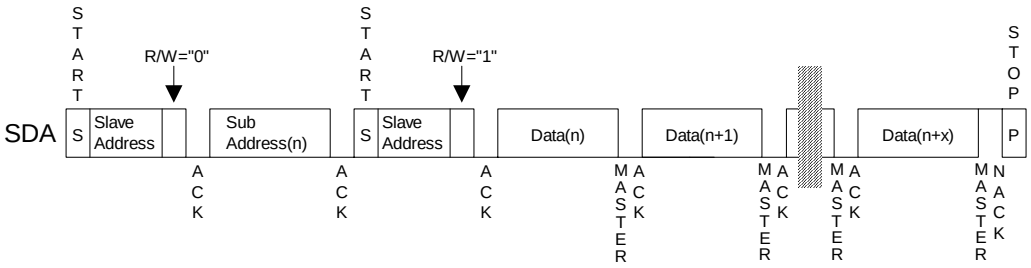


Figure 61. Random Address Read

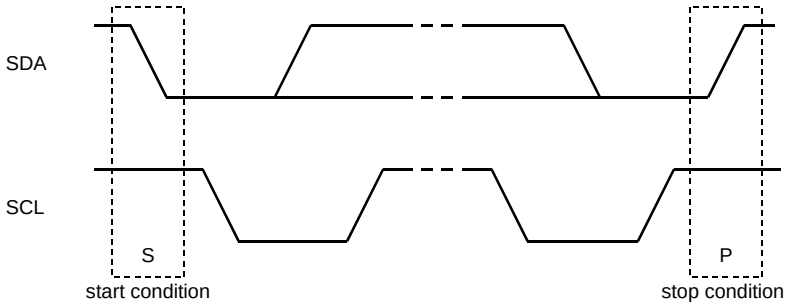


Figure 62. Start Condition and Stop Condition

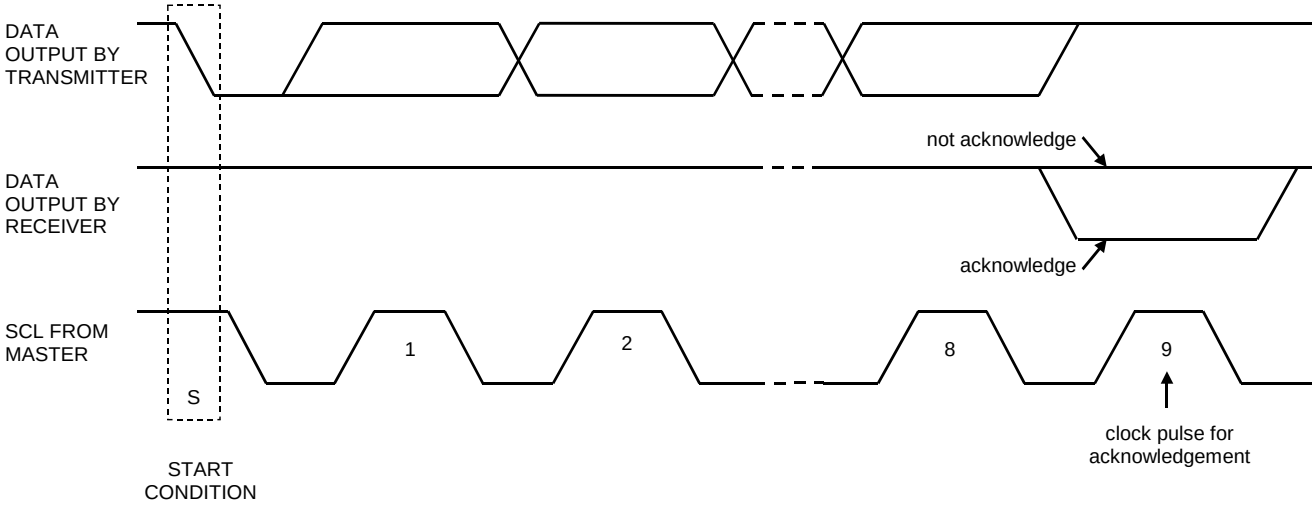


Figure 63. Acknowledge (I^2C Bus)

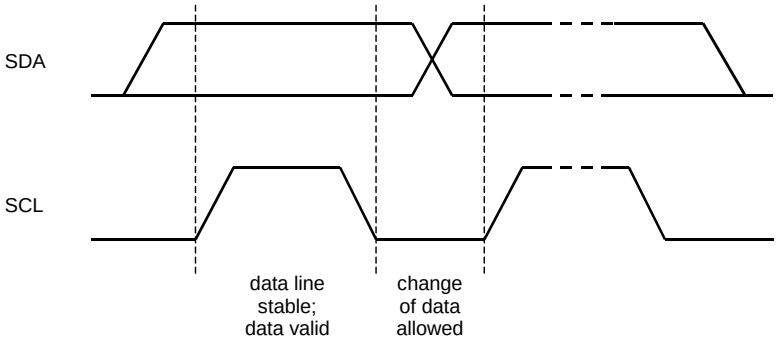


Figure 64. Bit Transfer (I^2C Bus)

■ Register Map 1

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
00H	Power Management 1	PMPFIL	0	PMBP	PMSPK	PMLO	PMDAC	PMADR	PMADL
01H	Power Management 2	ADRST	0	0	0	M/S	PMMP	MCKO	PMPLL
02H	MIC gain Control 1	0	0	0	0	MGAIN3	MGAIN2	MGAIN1	MGAIN0
03H	Gain Control	MICL	0	SPPKG1	SPKG0	0	0	LOVL1	LOVL0
04H	Mode Control 1	SPPSN	LOPS	0	0	BEEPS	BEEPL	DACS	DACL
05H	Mode Control 2	READ	MLOUT	0	0	0	0	INR	INL
06H	Mode Control 3	0	0	EXTC	0	MONO1	MONO0	DEM1	DEM0
07H	PLL Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	0	DIF1	DIF0
08H	PLL Control 2	PS1	PS0	0	0	FS3	FS2	FS1	FS0
09H	Digital MIC	0	0	PMDMR	PMDML	0	DCLKE	DCLKP	DMIC
0AH	BEEP Control	BPM	0	0	BPVCM	0	BPLVL2	BPLVL1	BPLVL0
0BH	HPF Control	0	0	0	0	0	HPFC1	HPFC0	HPFAD
0CH	Video Control	0	0	0	0	VG1	VG0	PMCP	PMV
0DH	Mode Control 4	THDET	0	0	0	0	0	0	COEW
0EH	Mode Control 5	0	0	0	0	0	0	0	INIT
0FH	ALC Level	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
10H	Reserved	0	0	0	0	0	0	0	0
11H	Reserved	0	0	0	0	0	0	0	0
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	0	0	0	0	0
14H	Reserved	0	0	0	0	0	0	0	0
15H	Reserved	0	0	0	0	0	0	0	0
16H	Reserved	0	0	0	0	0	0	0	0
17H	Reserved	0	0	0	0	0	0	0	0
18H	Reserved	0	0	0	0	0	0	0	0
19H	Reserved	0	0	0	0	0	0	0	0
1AH	Reserved	0	0	0	0	0	0	0	0
1BH	Reserved	0	0	0	0	0	0	0	0
1CH	Reserved	0	0	0	0	0	0	0	0
1DH	Reserved	0	0	0	0	0	0	0	0
1EH	Reserved	0	0	0	0	0	0	0	0
1FH	Reserved	0	0	0	0	0	0	0	0
20H	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
21H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
22H	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
23H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
24H	ALC Mode Contorl 1	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
25H	ALC Mode Contorl 2	OREF7	OREF6	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
26H	ALC Mode Contorl 3	0	0	WTM1	WTM0	0	0	RFST1	RFST0
27H	ALC Mode Contorl 4	SMUTE	ALC	RGAIN2	RGAIN1	RGAIN0	0	LMTH1	LMTH0
28H	Reserved	0	0	0	0	0	0	0	0
29H	Reserved	0	0	0	0	0	0	0	0
2AH	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
2BH	MIC Gain Control 2	MSGAINR3	MSGAINR2	MSGAINR1	MSGAINR0	MSGAINL3	MSGAINL2	MSGAINL1	MSGAINL0
2CH	Digital Filter Contorl 1	0	0	0	PFSDO	PFDAC	ADCPF	OVOLC	IVOLC
2DH	Digital Filter Contorl 2	0	0	LPF	HPF	EQ0	GN1	GN0	FIL3
2EH	Digital Filter Contorl 3	0	0	0	0	EQ4	EQ3	EQ2	0
2FH	Reserved	0	0	0	0	0	0	0	0

Note 42. PDN pin = "L" resets the registers to their default values.
Note 43. The bits defined as 0 must contain a "0" value.
Note 44. Address 0FH is a read only register. Writing access to 0FH is ignored and does not effect the operation.
Note 45. D15~D0 registers must contain "0" value.

■ **Register Map 2: Filter Coefficient (COEW bit = "1")**

Control Register Addr		Register Name	Initial
I^2C pin ="L" (3-wire mode)	I^2C pin ="H" (I^2C mode)		
01H	81H	Lch input volume	100000H
02H	82H	Rch input volume	100000H
03H	83H	HPF A0	100000H
04H	84H	HPF A1	000000H
06H	86H	HPF B1	000000H
09H	89H	LPF A0	100000H
0AH	8AH	LPF A1	000000H
0CH	8CH	LPF B1	000000H
0FH	8FH	Stereo Filter A0	100000H
10H	90H	Stereo Filter A1	000000H
11H	91H	Stereo Filter A2	000000H
12H	92H	Stereo Filter B1	000000H
13H	93H	Stereo Filter B2	000000H
19H	99H	EQ0 A0	100000H
1AH	9AH	EQ0 A1	000000H
1BH	9BH	EQ0 A2	000000H
1CH	9CH	EQ0 B1	000000H
1DH	9DH	EQ0 B2	000000H
20H	A0H	EQ2 A0	100000H
21H	A1H	EQ2 A1	000000H
22H	A2H	EQ2 A2	000000H
23H	A3H	EQ2 B1	000000H
24H	A4H	EQ2 B2	000000H
25H	A5H	EQ2 B1	000000H
26H	A6H	EQ2 B2	000000H
29H	A9H	EQ3 A0	100000H
2AH	AAH	EQ3 A1	000000H
2BH	ABH	EQ3 A2	000000H
2CH	ACH	EQ3 B1	000000H
2DH	ADH	EQ3 B2	000000H
2EH	AEH	EQ3 B1	000000H
2FH	AFH	EQ3 B2	000000H
32H	B2H	EQ4 A0	100000H
33H	B3H	EQ4 A1	000000H
34H	B4H	EQ4 A2	000000H
35H	B5H	EQ4 B1	000000H
36H	B6H	EQ4 B2	000000H
6BH	EBH	EQ1 A0	100000H
6CH	ECH	EQ1 A1	000000H
6DH	EDH	EQ1 A2	000000H
6EH	EEH	EQ1 B1	000000H
6FH	EFH	EQ1 B2	000000H

■ Register Definitions

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
00H	Power Management 1	PMPFIL	0	PMBP	PMSPK	PMLO	PMDAC	PMADR	PMADL
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMADL: MIC-Amp Lch and ADC Lch Power Management
0: Power-down (default)
1: Power-up

PMADR: MIC-Amp Rch, ADC Rch Power Management
0: Power down (default)
1: Power up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (1059/fs=24ms @44.1kHz, ADRST bit = "0") starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management
0: Power-down (default)
1: Power-up

PMLO: Stereo Line Output Power Management
0: Power-down (default)
1: Power-up

PMSPK: Speaker-Amp Power Management
0: Power-down (default)
1: Power-up

PMBP: Mono Input Power Management
0: Power-down (default)
1: Power-up
The ROUT/MIN pin performs as MIN pin. BEEPL and BEEPS bits control the path settings of Rch lineout and speaker from the MIN pin respectively.

PMPFIL: Programmable Filter Block (HPF2/LPF/FIL3/EQ/5 Band EQ/ALC) Power Management
(DSP system reset)
0: Power down (default)
1: Power up

All blocks except regulators can be powered-down by writing "0" to the address "00H", PMPLL, PMMP, PMDML, PMDMR, DMPE, PMADR, PMV, PMCP and MCKO bits. In this case, register values are maintained.

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
01H	Power Management 2	ADRST	0	0	0	M/S	PMMP	MCKO	PMPLL
R/W		R/W	R	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power down (default)
1: PLL Mode and Power up

MCKO: Master Clock Output Enable
0: Disable: MCKO pin = "L" (default)
1: Enable: Output frequency is selected by PS1-0 bits.

PMMP: MIC Power Management
0: Power down (default)
1: Power up

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

ADRST: ADC Initializing Cycle Select
0: 1059/fs (default)
1: 267/fs

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
02H	MIC gain Control 1	0	0	0	0	MGAIN3	MGAIN2	MGAIN1	MGAIN0
R/W		R	R	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

MGAIN3-0: MIC-Amp Gain Control (Table 21)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
03H	Gain Control	MICL	0	SPKG1	SPKG0	0	0	LOVL1	LOVL0
R/W		R/W	R	R/W	R/W	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	1

LOVL1-0: Stereo Line Output Gain and Signal Ground Setting (Table 43)

SPKG1-0: Speaker-Amp Output Gain Select (Table 51)

MICL: MIC Power Output Voltage Select
0: typ 2.5V (AVDD=3.0 ~ 3.6V) (default)
1: typ 2.2V (AVDD = 2.7 ~ 3.6V)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
04H	Mode Control 1	SPPSN	LOPS	0	0	BEEPS	BEEPL	DACS	DACL
R/W		R/W	R/W	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACL: DAC Output Signal to Stereo Line Amp Control
0: OFF (default)
1: ON
When PMLO bit = "1", this bit setting is enabled. LOUT and ROUT pins output VSS1 when PMLO bit = "0".

DACS: Signal Switch Control from DAC to Speaker-Amp
0: OFF (default)
1: ON
When DACS bit is "1", DAC output signal is input to Speaker-Amp.

BEEPL: Signal Switch Control from the MIN pin to Lineout
0: OFF (default)
1: ON
This setting is valid when PMBP bit = "1". Set BEEP signal input mode by BPM bit. The signal from the MIN pin is input to lineout by BEEPL bit = "1".

BEEPS: Signal Switch Control from the MIN pin to Speaker-Amp
0: OFF (default)
1: ON
This setting is valid when PMBP bit = "1". Set BEEP signal input mode by BPM bit. The signal from the MIN pin is input to lineout by BEEPS bit = "1".

LOPS: Stereo Line Output Power Save
0: Normal Operation (default)
1: Power Save Mode

SPPSN: Speaker-Amp Power-Save Mode
0: Power-Save Mode (default)
1: Normal Operation
When SPPSN bit is "0", Speaker-Amp is in power-save mode. In this mode, the SPP pin goes to Hi-Z and the SPN pin outputs AVDD/2 voltage. When PMSPK bit = "1", SPPSN bit is enabled. After the PDN pin is set to "L", Speaker-Amp is in power-down mode since PMSPK bit is "0".

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
05H	Mode Control 2	READ	MLOUT	0	0	0	0	INR	INL
R/W		R/W	R/W	R	R	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

INL: ADC Lch Input Source Select
0: LIN1 pin (default)
1: LIN2 pin

INR: ADC Rch Input Source Select
0: RIN1 pin (default)
1: RIN2 pin

MLOUT: Lineout Mono Mode Switch
0: Lineout Stereo mode (default)
Both L and R channel lineout amplifiers are powered-up when PMLO bit = "0".
1: Lineout Mono mode
Only L channel lineout amplifier is powered-up when PMLO bit = "1". R channel lineout amplifier is powered-down.

READ: Read Function Enable
0: Disable (default)
1: Enable

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
06H	Mode Control 3	0	0	EXTC	0	MONO1	MONO0	DEM1	DEM0
R/W		R	R	R/W	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

DEM1-0: De-emphasis Control (Table 41)
Default: "01" (OFF)

MONO1-0: LOUT/ROUT Output Signal Mode Select (Table 44)

EXTC: LIN1/RIN1 and LOUT/ROUT External Connect Mode Switch (Table 45)
0: External Connect Mode Disable (default)
1: External Connect Mode Enable

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
07H	PLL Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	0	DIF1	DIF0
R/W		R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Default		0	1	1	0	0	0	1	0

DIF1-0: Audio Interface Format (Table 17)
Default: "10" (MSB justified)

BCKO: Master Mode BICK Output Frequency Setting (Table 10)

PLL3-0: PLL Reference Clock Select (Table 4)
Default: "0110" (MCKI pin, 12MHz)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
08H	PLL Control 2	PS1	PS0	0	0	FS3	FS2	FS1	FS0
R/W		R/W	R/W	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	1	1

FS3-0: Sampling frequency (Table 5, Table 6) and MCKI frequency (Table 11) Setting
These bits control sampling frequency in PLL mode and control MCKI input frequency in EXT mode.

PS1-0: MCKO Frequency Setting (Table 9)
Default: "00" (256fs)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
09H	Digital MIC	0	0	PMDMR	PMDML	0	DCLKE	DCLKP	DMIC
R/W		R	R	R/W	R/W	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DMIC: Digital Microphone Connection Select
0: Analog Microphone (default)
1: Digital Microphone

DCLKP: Data Latching Edge Select
0: Lch data is latched on the DMCLK rising edge ("↑"). (default)
1: Lch data is latched on the DMCLK falling edge ("↓").

DCLKE: DMCLK pin Output Clock Control
0: "L" Output (default)
1: 64fs Output

PMDML/R: Input Signal Select with Digital Microphone (Table 19)
Default: "00"
ADC digital block is powered-down by PMDML = PMDMR bits = "0" when selecting a digital microphone input (DMIC bit = "1", INL/R bits = "00", "01" or "10").

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
0AH	BEEP Control	BPM	0	0	BPVCM	0	BPLVL2	BPLVL1	BPLVL0
R/W		R/W	R	R	R/W	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPLVL2-0: BEEP Output Level Setting (Table 50)
Default: "0H": 0dB

BPVCM: Common Voltage Setting of MIN Input Amplifier
0: 1.15V (default)
1: 1.65V

BPM: BEEP Mode Setting (Table 47)
Default: "0": Internal Resistance Mode

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
0BH	HPF Control	0	0	0	0	0	HPFC1	HPFC0	HPFAD
R/W		R	R	R	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

HPFAD: HPF1 Control of ADC
0: OFF
1: ON (default)
When HPFAD bit is "1", the settings of HPFC1-0 bits are enabled. When HPFAD bit is "0", HPFAD block is through (0dB).
When PMADL bit = "1" or PMADR bit = "1", set HPFAD bit to "1".

HPFC1-0: Cut-off Frequency Setting of HPF1 (ADC) (Table 40)
Default: "00" (3.4Hz @ fs = 44.1kHz)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
0CH	Video Control	0	0	0	0	VG1	VG0	PMCP	PMV
R/W		R	R	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMV: Composite Video Block Power Management (VIN pin → VOUT pin)
0: Power down (default)
1: Power up

PMCP: Charge Pump Power Management
0: Power down (default)
1: Power up

VG1-0: Video Amp Gain Select

VG1-0 bits	GAIN(dB)	
00	+6dB	(default)
01	+9dB	
10	+12dB	
11	+16.5dB	

Table 54. Video Signal Gain Setting

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
0DH	Mode Control 4	THDET	0	0	0	0	0	0	COEW
R/W		R	R	R	R	R	R	R	R/W
Default		0	0	0	0	0	0	0	0

COEW: Filter Coefficient Write Enable
0: Disable (default)
1: Enable

THDET: Thermal Shutdown Detection (READ only)
This bit becomes "1" when the internal temperature of LSI exceeds 170°C (typ). When THDET bit changes to "1", PMSPK, PMLO, PMV and PMCP bits become "0" forcibly. THDET bit returns to "0" when the internal temperature is down, however, PMSPK, PMLO, PMV and PMCP bits stays "0".

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
0EH	Mode Control 5	0	0	0	0	0	0	0	INIT
R/W		R	R	R	R	R	R	R	R/W
Default		0	0	0	0	0	0	0	0

INIT: Programmable Filter Initializing
Programmable filter coefficients are initialized by INIT bit = "1". INIT bit returns to "0" automatically when the initialization is finished. This initialization must be made after clocks are input following the PDN pin = "L" → "H".

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
0FH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
R/W		R	R	R	R	R	R	R	R
Default		-	-	-	-	-	-	-	-

VOL7-0: Current ALC volume value, Read operation only (Table 34)

(ALC Registers)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
20H	Lch Intput Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
21H	Rch Intput Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IVL7-0, IVR7-0: Input Digital Volume
Default: "E1H" (+30dB)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
22H	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
23H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

OVL7-0, OVR7-0: Output Digital Volume
Default: "91H" (0dB)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
24H	ALC Mode Control 1	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
25H	ALC Mode Control 2	OREF7	OREF6	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IREF7-0: Reference Value of ALC Recovery Operation (Recording). 0.375dB step, 242 Level (Table 31)
OREF7-0: Reference Value of ALC Recovery Operation (Playback). 0.375dB step, 242 Level (Table 32)

Default: "E1H" (+30.0dB)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
26H	ALC Mode Control 3	0	0	WTM1	WTM0	0	0	RFST1	RFST0
R/W		R	R	R/W	R/W	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

RFST1-0: ALC First Recovery Speed (Table 33)
Default: "00"
* Writing to these registers is valid only when PMFIL bit ="0". When PMFIL bit = "1", writings are ignored.

WTM1-0: ALC Recovery Waiting Period (Table 29)
Default: "00"

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
27H	ALC Mode Control 3	SMUTE	ALC	RGAIN2	RGAIN1	RGAIN0	0	LMTH1	LMTH0
R/W		R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 27)
Default: "00"

RGAIN2-0: ALC Recovery GAIN Step (Table 30)
Default: "000"
* Writing to these registers is valid only when PMFIL bit ="0". When PMFIL bit = "1", writings are ignored.

ALC: ALC Enable
0: ALC Disable (default)
1: ALC Enable

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted
* This bit is invalid during an ALC operation.

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
2AH	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	0	0	0	0	0	1

DVOL7-0: Output Digital Volume 2 (Table 39)
Default: "C1H" (0dB)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
2BH	MIC Gain Control 2	MSGAINR3	MSGAI NR2	MSGAINR1	MSGAINR0	MSGAINL3	MSGAINL2	MSGAINL1	MSGAINL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MSGAINL0-3: Lch Mic Sensitivity Compensation (Table 22)

MSGAINR0-3: Rch Mic Sensitivity Compensation (Table 22)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
2CH	Digital Filter Control 1	0	0	0	PFSDO	PFDAC	ADCPF	OVOLC	IVOLC
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	1

IVOLC: IVOL Control
0: Independent
1: Dependent (default)
When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume levels, while register values of IVL7-0 bits are not written to IVR7-0 bits.

OVOLC: Output Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When OVOLC bit = "1", OVL7-0 bits control both Lch and Rch volume levels, while register values of OVL7-0 bits are not written to OVR7-0 bits.

ADCPF: Programmable Filter / ALC Input Signal Select
0: SDTI
1: ALC Output (default)

PFDAC: DAC Input Signal Select
0: SDTI (default)
1: Programmable Filter / ALC Output

PFSDO: SDTO Output Signal Select
0: ADC (+ 1st HPF) Output
1: Programmable Filter / ALC Output (default)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
2DH	Digital Filter Control 2	0	0	LPF	HPF	EQ0	GN1	GN0	FIL3
R/W		R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FIL3: Stereo Emphasis Filter Control
0: OFF (default)
1: ON
When FIL3 bit = "1", the settings of 8FH ~ 93H are enabled.

GN1-0: Gain Block Gain Setting (Table 26)
Default: "00" (0dB)

EQ0: Gain Compensation Filter (EQ0) Control
0: OFF (default)
1: ON
When EQ0 bit = "1", the settings of 99H ~ 9DH are enabled. When EQ0 bit = "0", EQ0 block is through (0dB).

HPF: HPF2 Coefficient Setting Enable
0: OFF (default)
1: ON
When HPF bit is "1", the settings of 83H ~ 87H are enabled. When HPF bit is "0", HPF2 block is through (0dB).

LPF: LPF Coefficient Setting Enable
0: OFF (default)
1: ON
When LPF bit is "1", the settings of 89H ~ 8DH are enabled. When LPF bit is "0", LPF block is through (0dB).

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
2EH	Digital Filter Control 3	0	0	0	0	EQ4	EQ3	EQ2	0
R/W		R	R	R	R	R/W	R/W	R/W	R
Default		0	0	0	0	0	0	0	0

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit is "1", the settings of A0H ~ A6H are enabled. When EQ2 bit is "0", EQ2 block is through (0dB).

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit is "1", the settings of A9H ~ AFH are enabled. When EQ3 bit is "0", EQ3 block is through (0dB).

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit is "1", the settings of B2 ~ B6H are enabled. When EQ4 bit is "0", EQ4 block is through (0dB).

Register Map 2

MIC Sensitivity Compensation Coefficient

Addr	Register Name	D23 ~ D20	D19 ~ D16	D15 ~ D12	D11 ~ D8	D7 ~ D4	D3 ~ D0
		Default					
01H (3-wire) 81H (I^2C)	Lch input volume	0001	0000	0000	0000	0000	0000
02H (3-wire) 82H (I^2C)	Rch input volume	0001	0000	0000	0000	0000	0000
R/W		W	W	W	W	W	W

* MIC sensitivity compensation gain can be written to the DSP directly without setting register 2BH.

HPF2 Coefficient

Addr	Register Name	D23 ~ D20	D19 ~ D16	D15 ~ D12	D11 ~ D8	D7 ~ D4	D3 ~ D0
		Default					
03H (3-wire) 83H (I^2C)	HPF A0	0001	0000	0000	0000	0000	0000
04H (3-wire) 84H (I^2C)	HPF A1	0000	0000	0000	0000	0000	0000
06H (3-wire) 86H (I^2C)	HPF B1	0000	0000	0000	0000	0000	0000
R/W		W	W	W	W	W	W

* When the coefficients are in default setting, audio data passes through this block by 0dB gain even if HPF bit = "1".

LPF Coefficient

Addr	Register Name	D23 ~ D20	D19 ~ D16	D15 ~ D12	D11 ~ D8	D7 ~ D4	D3 ~ D0
		Default					
09H (3-wire) 89H (I^2C)	LPF A0	0001	0000	0000	0000	0000	0000
0AH (3-wire) 8AH (I^2C)	LPF A1	0000	0000	0000	0000	0000	0000
0CH (3-wire) 8CH (I^2C)	LPF B1	0000	0000	0000	0000	0000	0000
R/W		W	W	W	W	W	W

* When the coefficients are in default setting, audio data passes through this block by 0dB gain even if LPF bit = "1".

Stereo Emphasis FIL3 Coefficient

Addr	Register Name	D23 ~ D20	D19 ~ D16	D15 ~ D12	D11 ~ D8	D7 ~ D4	D3 ~ D0
		Default					
0FH (3-wire) 8FH (I^2C)	Stereo Filter A0	0001	0000	0000	0000	0000	0000
10H (3-wire) 90H (I^2C)	Stereo Filter A1	0000	0000	0000	0000	0000	0000
11H (3-wire) 91H (I^2C)	Stereo Filter A2	0000	0000	0000	0000	0000	0000
12H (3-wire) 92H (I^2C)	Stereo Filter B1	0000	0000	0000	0000	0000	0000
13H (3-wire) 93H (I^2C)	Stereo Filter B2	0000	0000	0000	0000	0000	0000
R/W		W	W	W	W	W	W

* When the coefficients are in default setting, audio data passes through this block by 0dB gain even if FIL3 bit = "1".

Stereo Emphasis EQ0 (Gain compensation) Coefficient

Addr	Register Name	D23 ~ D20	D19 ~ D16	D15 ~ D12	D11 ~ D8	D7 ~ D4	D3 ~ D0
		Default					
19H (3-wire) 99H (I^2C)	EQ0 A0	0001	0000	0000	0000	0000	0000
1AH (3-wire) 9AH (I^2C)	EQ0 A1	0000	0000	0000	0000	0000	0000
1BH (3-wire) 9BH (I^2C)	EQ0 A2	0000	0000	0000	0000	0000	0000
1CH (3-wire) 9CH (I^2C)	EQ0 B1	0000	0000	0000	0000	0000	0000
1DH (3-wire) 9DH (I^2C)	EQ0 B2	0000	0000	0000	0000	0000	0000
R/W		W	W	W	W	W	W

* When the coefficients are in default setting, audio data passes through this block by 0dB gain even if EQ0 bit = "1".

EQ2 Coefficient

Addr	Register Name	D23 ~ D20	D19 ~ D16	D15 ~ D12	D11 ~ D8	D7 ~ D4	D3 ~ D0
		Default					
20H (3-wire) A0H (I^2C)	EQ2 A0	0001	0000	0000	0000	0000	0000
21H (3-wire) A1H (I^2C)	EQ2 A1	0000	0000	0000	0000	0000	0000
22H (3-wire) A2H (I^2C)	EQ2 A2	0000	0000	0000	0000	0000	0000
23H (3-wire) A3H (I^2C)	EQ2 B1	0000	0000	0000	0000	0000	0000
24H (3-wire) A4H (I^2C)	EQ2 B2	0000	0000	0000	0000	0000	0000
25H (3-wire) A5H (I^2C)	EQ2 B1	0000	0000	0000	0000	0000	0000
26H (3-wire) A6H (I^2C)	EQ2 B2	0000	0000	0000	0000	0000	0000
R/W		W	W	W	W	W	W

* When the coefficients are in default setting, audio data passes through this block by 0dB gain even if EQ2 bit = "1".

EQ3 Coefficient

Addr	Register Name	D23 ~ D20	D19 ~ D16	D15 ~ D12	D11 ~ D8	D7 ~ D4	D3 ~ D0
		Default					
29H (3-wire) A9H (I^2C)	EQ3 A0	0001	0000	0000	0000	0000	0000
2AH (3-wire) AAH (I^2C)	EQ3 A1	0000	0000	0000	0000	0000	0000
2BH (3-wire) ABH (I^2C)	EQ3 A2	0000	0000	0000	0000	0000	0000
2CH (3-wire) ACH (I^2C)	EQ3 B1	0000	0000	0000	0000	0000	0000
2DH (3-wire) ADH (I^2C)	EQ3 B2	0000	0000	0000	0000	0000	0000
2EH (3-wire) AEH (I^2C)	EQ3 B1	0000	0000	0000	0000	0000	0000
2FH (3-wire) AFH (I^2C)	EQ3 B2	0000	0000	0000	0000	0000	0000
R/W		W	W	W	W	W	W

* When the coefficients are in default setting, audio data passes through this block by 0dB gain even if EQ3 bit = "1".

EQ4 Coefficient

Addr	Register Name	D23 ~ D20	D19 ~ D16	D15 ~ D12	D11 ~ D8	D7 ~ D4	D3 ~ D0
		Default					
32H (3-wire) B2H (I^2C)	EQ4 A0	0001	0000	0000	0000	0000	0000
33H (3-wire) B3H (I^2C)	EQ4 A1	0000	0000	0000	0000	0000	0000
34H (3-wire) B4H (I^2C)	EQ4 A2	0000	0000	0000	0000	0000	0000
35H (3-wire) B5H (I^2C)	EQ4 B1	0000	0000	0000	0000	0000	0000
36H (3-wire) B6H (I^2C)	EQ4 B2	0000	0000	0000	0000	0000	0000
R/W		W	W	W	W	W	W

* When the coefficients are in default setting, audio data passes through this block by 0dB gain even if EQ4 bit = "1".

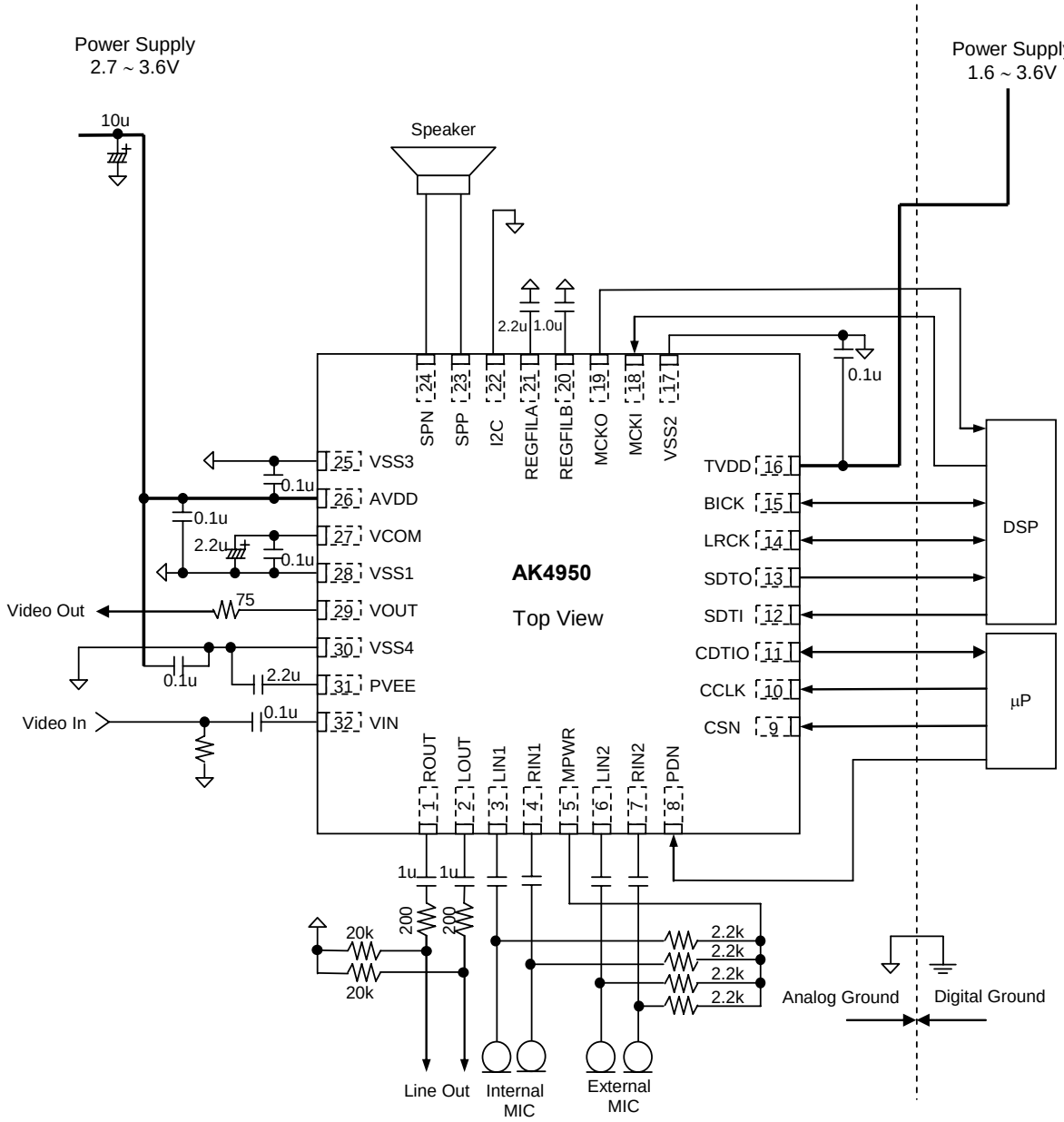
EQ1 Coefficient

Addr	Register Name	D23 ~ D20	D19 ~ D16	D15 ~ D12	D11 ~ D8	D7 ~ D4	D3 ~ D0
		Default					
6BH (3-wire) EBH (I^2C)	EQ1A0	0001	0000	0000	0000	0000	0000
6CH (3-wire) ECH (I^2C)	EQ1 A1	0000	0000	0000	0000	0000	0000
6DH (3-wire) EDH (I^2C)	EQ1 A2	0000	0000	0000	0000	0000	0000
6EH (3-wire) EEH (I^2C)	EQ1 B1	0000	0000	0000	0000	0000	0000
6FH (3-wire) EFH (I^2C)	EQ1 B2	0000	0000	0000	0000	0000	0000
R/W		W	W	W	W	W	W

* When the coefficients are in default setting, audio data passes through this block by 0dB gain even if EQ1 bit = "1".

SYSTEM DESIGN

Figure 65 shows the system connection diagram. An evaluation board (AKD4950) is available for fast evaluation as well as suggestions for peripheral circuitry.



Notes:

- VSS1, VSS2, VSS3 and VSS4 of the AK4950 must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- When the AK4950 is used in master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, around 100kΩ pull-up resistor must be connected to LRCK and BICK pins of the AK4950.

Figure 65. System Connection Diagram (3-wire Mode, Stereo Lineout PMBP bit = "0")

1. Grounding and Power Supply Decoupling

The AK4950 requires careful attention to power supply and grounding arrangements. A ceramic capacitor of 0.1μF or more should be connected to between AVDD and VSS1/3/4. If AVDD and TVDD are supplied separately, the power-up sequence is not critical. VSS1, VSS2, VSS3 and VSS4 of the AK4950 must be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors must be as near to the AK4950 as possible, with the small value ceramic capacitor being the nearest.

2. Internal Regulated Voltage Power Supply

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4950.

3. Analog Inputs

The Mic and Line inputs supports single-ended. The input signal range scales with nominally at typ. 0.9 x 2.3Vpp (@ MGAIN = 0dB), centered around the internal signal ground (typ. 1.15V). Usually the input signal is AC coupled with a capacitor. The cut-off frequency is $fc = 1/(2\pi RC)$. The AK4950 can accept input voltages from VSS1 to AVDD.

6. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage for 000000H (@24bit data). The common voltage of stereo lineout is 1.35V or 1.43V (typ) and the speaker output is centered on AVDD/2 (typ).

CONTROL SEQUENCE

■ Clock Set up

When ADC, DAC, Digital Microphone and Programmable Filter are used, the clocks must be supplied.

1. PLL Master Mode

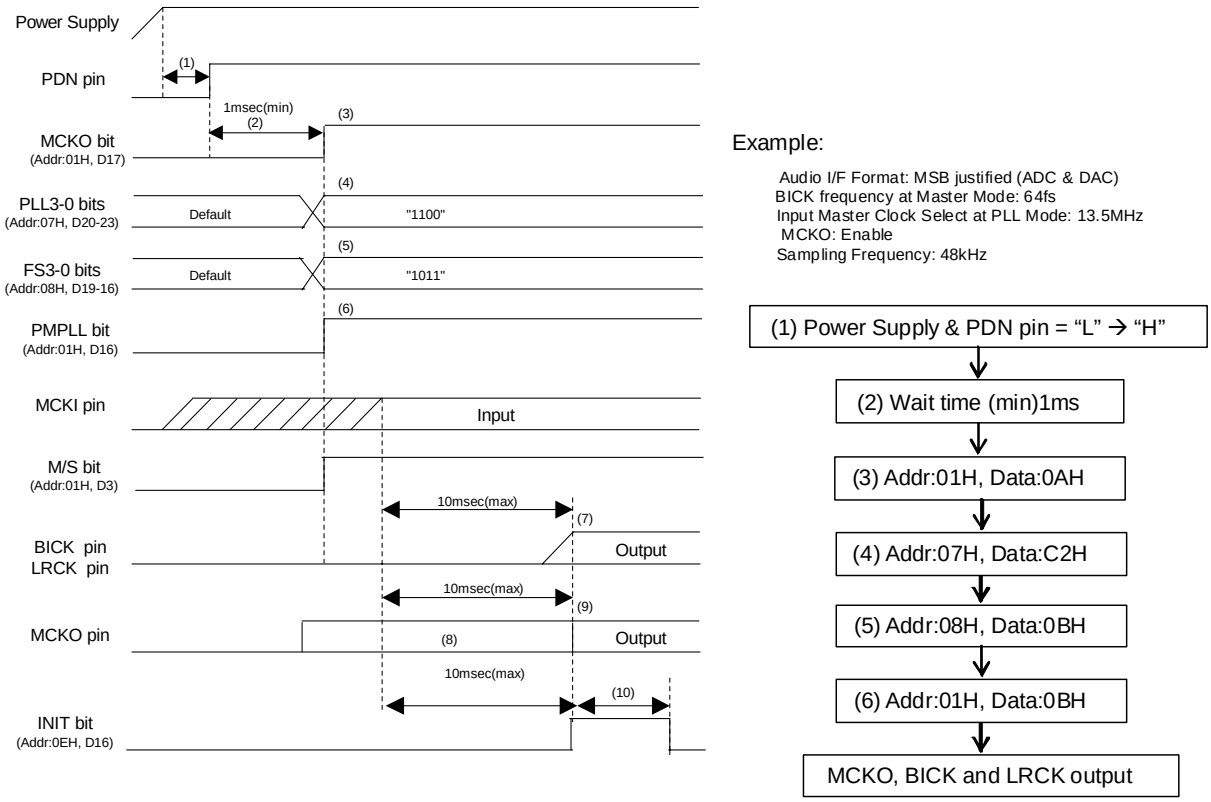


Figure 66. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin = "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4950.

(2) PDN pin reset release waiting time
Wait time of 1ms or more is needed for the internal VCOM voltage rising.

(3) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"

(4) PLL mode setting. (When the reference clock is MCKI = 13.5MHz, PLL3-0 bits = "1100")

(5) Sampling frequency setting. (In case of fs = 48kHz, FS3-0 bits = "1011")

(6) PLL lock time is 10ms (max) after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.

(7) The AK4950 starts outputting the LRCK and BICK clocks after the PLL becomes stable and the normal operation starts.

(8) Invalid clock is output from MCKO pin during this period when MCKO bit = "1".

(9) Normal clock is output from the MCKO pin after PLL is locked when MCKO bit = "1".

(10) Digital Function Initializing
Digital functions can be initialized by setting INIT bit = "0" → "1" after normal clock is output from the MCKO pin. The initializing time is 1/512fs x 18,000 [s]. INIT bit returns to "0" automatically when the initialization is finished. This initialization must be executed when using ALC and Programmable Filter.

2. When the external clock (BICK pin) is used in PLL Slave mode.

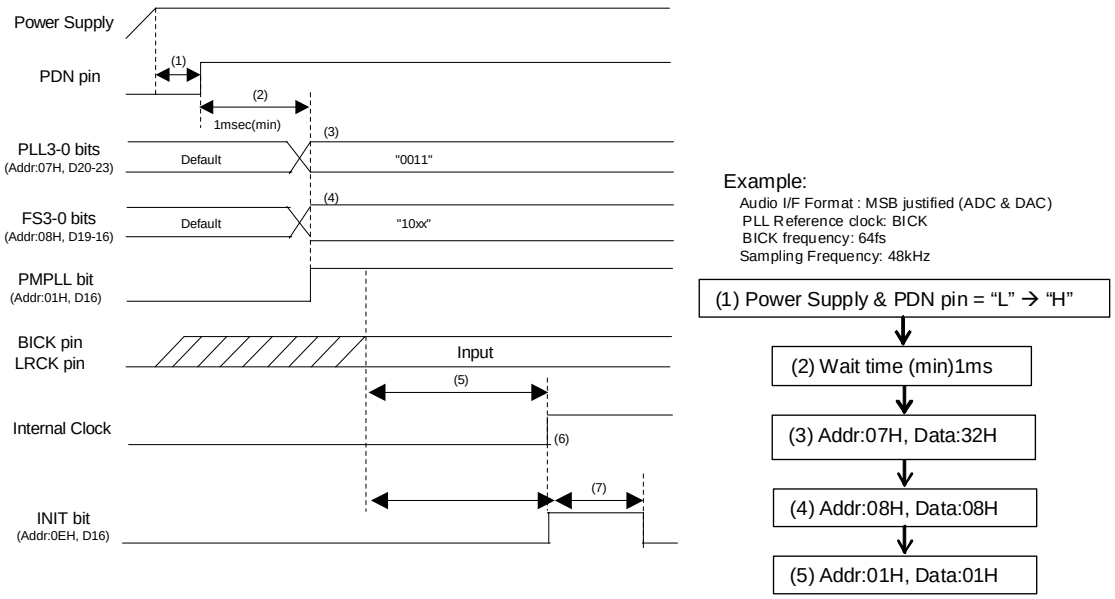


Figure 67. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4950.

(2) PDN pin reset release waiting time
Wait time of 1ms or more is needed for the internal VCOM voltage rising.

(3) PLL mode setting. (When the reference clock is BICK = 64fs, PLL3-0 bits = "0011")

(4) Sampling frequency setting. (In case of fs = 48kHz, FS3-0 bits = "10xx")

(5) PLL lock time is 2ms (max) after the PMPLL bit changes from "0" to "1" and PLL reference clock (BICK pin) is supplied.

(6) Normal operation starts after the PLL is locked.

(7) Digital Function Initializing
Digital functions can be initialized by setting INIT bit = "0" → "1" after normal clock is output. The initializing time is 1/512fs x 18,000 [s]. INIT bit returns to "0" automatically when the initialization is finished. This initialization must be executed when using ALC and Programmable Filter.

3. When the external clock (MCKI pin) is used in PLL Slave mode.

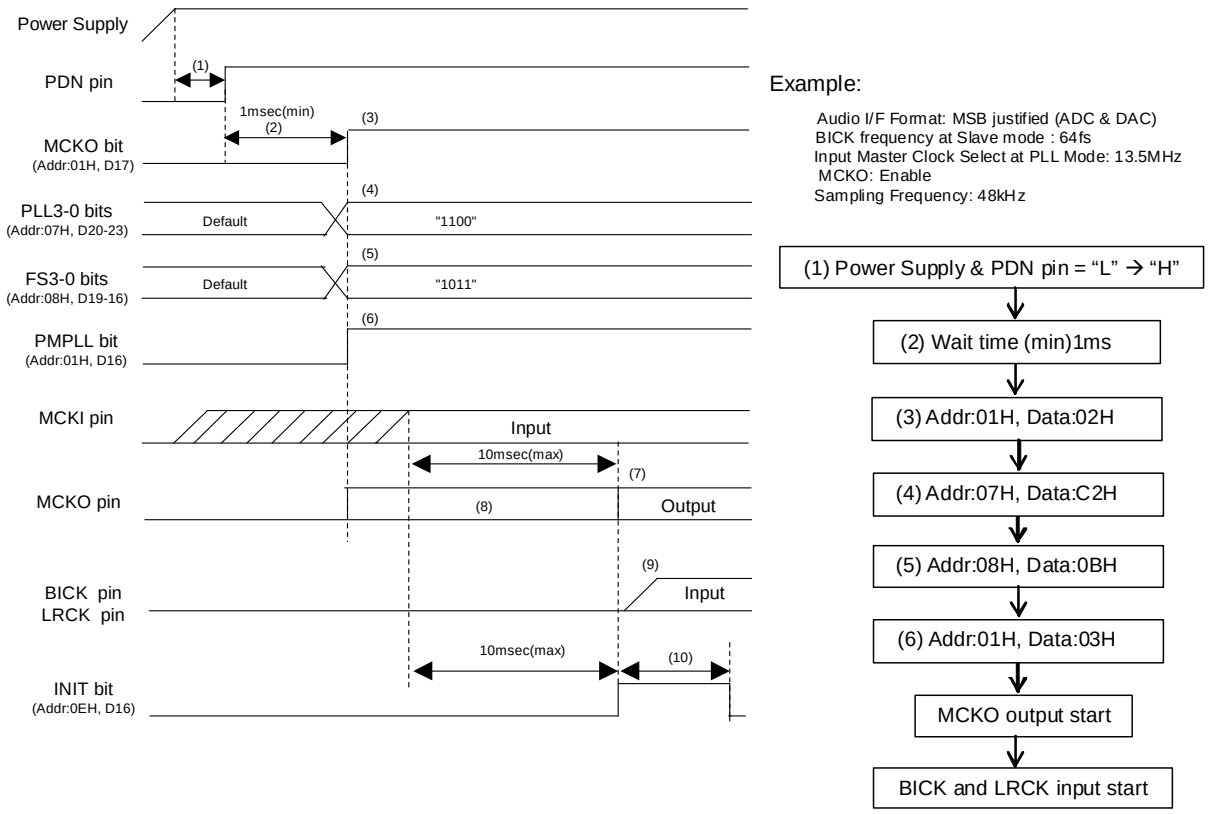


Figure 68. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4950.

(2) PDN pin reset release waiting time
Wait time of 1ms or more is needed for the internal VCOM voltage rising.

(3) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"

(4) PLL mode setting. (When the reference clock is MCKI = 13.5MHz, PLL3-0 bits = "1100")

(5) Sampling frequency setting. (In case of fs = 48kHz, FS3-0 bits = "1011")

(6) PLL lock time is 10ms (max) after the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied.

(7) Normal clock is output from the MCKO pin after PLL is locked.

(8) Invalid clock is output from MCKO pin during this period.

(9) BICK and LRCK clocks should be synchronized with MCKO clock.

(10) Digital Function Initializing
Digital functions can be initialized by setting INIT bit = "0" → "1" after normal clock is output. The initializing time is 1/512fs x 18,000 [s]. INIT bit returns to "0" automatically when the initialization is finished. This initialization must be executed when using ALC and Programmable Filter.

4. EXT Slave Mode

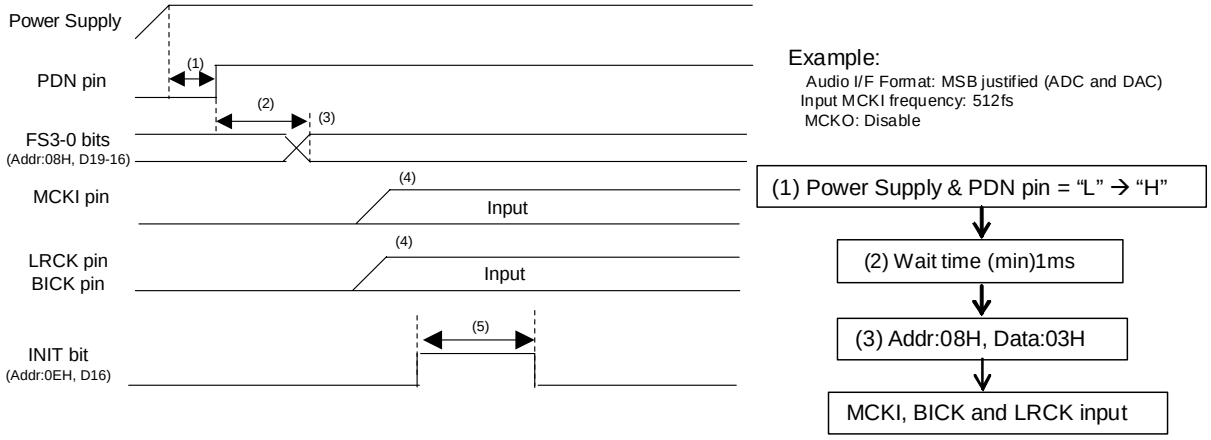


Figure 69. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4950.

(2) PDN pin reset release waiting time
Wait time of 1ms or more is needed for the internal VCOM voltage rising.

(3) Sampling frequency setting. (In case of fs = 48kHz, FS3-0 bits = "xx11")

(4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

(5) Digital Function Initializing
Digital functions can be initialized by setting INIT bit = "0" → "1" after normal clock is supplied. The initializing time is 1/512fs x 18,000 [s]. INIT bit returns to "0" automatically when the initialization is finished. This initialization must be executed when using ALC and Programmable Filter.

■ MIC Input Recording (Stereo)

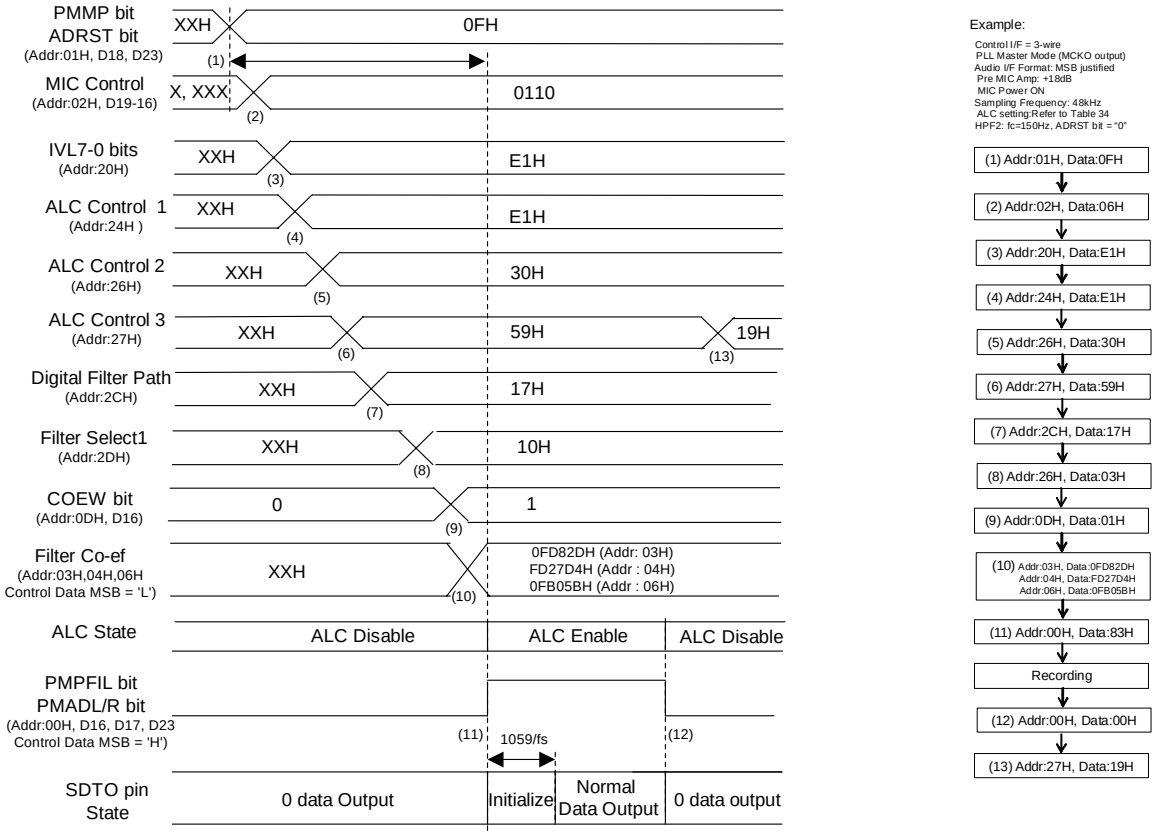


Figure 70. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs=48kHz. If the parameter of the ALC1 is changed, please refer to the Figure 39. At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Power Up MIC Power: PMMP bit = "0" → "1", ADRST bit (initializing cycle) setting (Addr = 01H)
(2) Set up gain for microphone by MGAIN3-0 bits (Addr = 02H)
(3) Set up ALC starting IVOL value. (Addr = 20H)
(4) Set up IREF value. (Addr = 24H)
(5) Set up RFST1-0 and WTM1-0 bits for ALC (Addr= 26H)
(6) Set up LMTH1-0, RGAIN2-0 bits and ALC bit. (Addr=27H)
(7) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr=2CH)
(8) Switch ON/OFF of the Programmable Filter: HPF bit = "1" (Addr= 2DH)
(9) Set up COEW bit = "1" (Addr = 0DH)
When COEW bit = "1", registers on the register map 1 and 2 can be accessed. Set the most significant bit (MSB) of the control data to "1" (Figure 52) to access registers on the register map 1, and set "0" to access registers on the register map 2 (Figure 53).
(10) Set up Coefficient of the Programmable Filter (Addr=03H, 04H, 06H: Control data MDB = "L")
(11) Power up of the ADC and Programmable Filter: (PMADL=PMADR=PMPFIL bits = "0" → "1")
The initialization cycle of the ADC is 1059/fs=22.06ms@fs=48kHz when ADRST bit = "0". ADC outputs "0" during the initialization. ALC starts operation at the value set by IVOL (3).
(12) Power down of the microphone, ADC and Programmable Filter: (PMADL=PMADR=PMPFIL bits = "1" → "0")
(13) ALC Disable: ALC bit "1" → "0"

■ Digital MIC Input (Stereo)

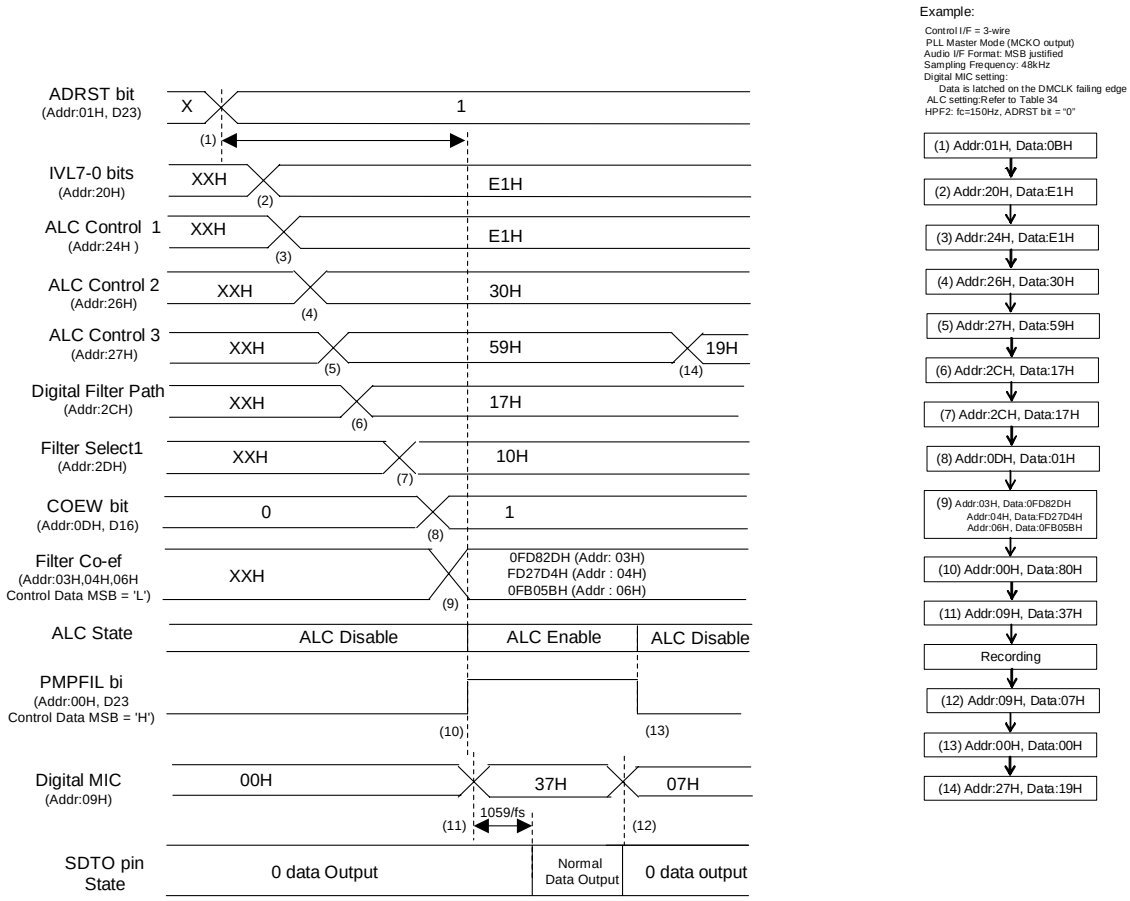


Figure 71. Digital MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs=48kHz. If the parameter of the ALC1 is changed, please refer to the Figure 39. At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up ADRST bit (initializing cycle) setting (Addr = 01H)
(2) Set up ALC starting IVOL value. (Addr = 20H)
(3) Set up IREF value. (Addr = 24H)
(4) Set up RFST1-0 and WTM1-0 bits for ALC (Addr= 26H)
(5) Set up LMTH1-0, RGAIN2-0 bits and ALC bit. (Addr=27H)
(6) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr=2CH)
(7) Switch ON/OFF of the Programmable Filter: HPF bit = "1" (Addr= 2DH)
(8) Set up COEW bit = "1" (Addr = 0DH)
When COEW bit = "1", registers on the register map 1 and 2 can be accessed. Set the most significant bit (MSB) of the control data to "1" (Figure 52) to access registers on the register map 1, and set "0" to access registers on the register map 2 (Figure 53).
(9) Set up Coefficient of the Programmable Filter (Addr=03H, 04H, 06H: Control data MSB = "L")
(10) Power up of the Programmable Filter: (PMADL=PMADR=PMPFIL bits = "0" → "1")
(11) Power up and set the digital MIC: (PMDMR=PMDML bits = "0" → "1")
The initialization cycle of the ADC is 1059/fs=22.06ms@fs=48kHz when ADRST bit = "0". ADC outputs "0" during the initialization. ALC starts operation at the value set by IVOL (4).
(12) Power-down the digital MIC. PMDMR=PMDML bits "1" → "0"
(13) Programmable Filter Power-down ALC Disable: PMPFIL bit "1" → "0"
(14) ALC1 Disable: ALC1 bit = "1" → "0"

■ Speaker-Amp Output

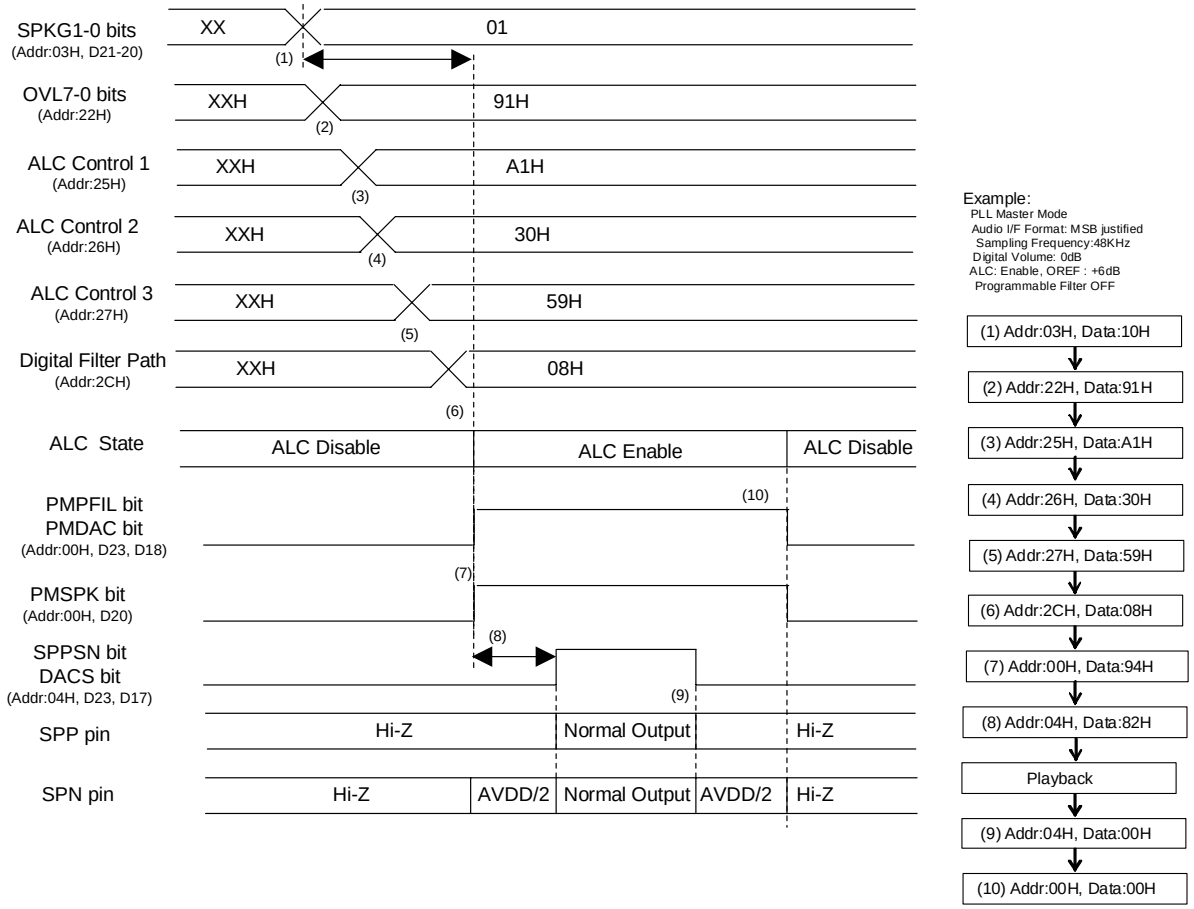


Figure 72. Speaker-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up SPK-Amp gain: SPKG1-0 bits = "00" → "01" (Addr = 03H)

(2) Set up OVOL value for output digital volume. (Addr = 22H)

This is the ALC stating OVOL value. When OVOLC bit = "1", OVL7-0 bits (Addr= 22H) controls Lch and Rch volumes. After the digital block is powered-up, the volume changes to the set value set from the default value (0dB) in soft transition. When ALC bit is "0", this volume can be used as a digital volume.

(3) Set up OREF value. (Addr = 25H)

(4) Set up RFST1-0 bits and WTM1-0 bits. (Addr= 26H)

(5) Set up LMTH-0 bits, RGAIN2-0 bits and ALC bit. (Addr=27H)

(6) Set up Programmable Filter Path: PESDO = ADCPF = PFDAC bits = "1" (Addr = 2CH)

(7) Power up DAC, Programmable Filter and Speaker-Amp: PMPFIL = PMSPK = PMDAC bits = "0" → "1"

(8) Exit power-save mode of Speaker-Amp: SPPSN bit = "1" → "0"

DAC → SPK-Amp Path setting: DACS bit = "0" → "1"

(9) Enter Speaker-Amp power save mode: SPPSN bit = "0" → "1"

Disables DAC → SPK-Amp path: DACS bit = "1" → "0"

(10) Power down DAC, MIN-Amp, Programmable Filter and Speaker-Amp.

PMPFIL = PMSPK = PMDAC bits = "1" → "0"

■ Stereo Line Output

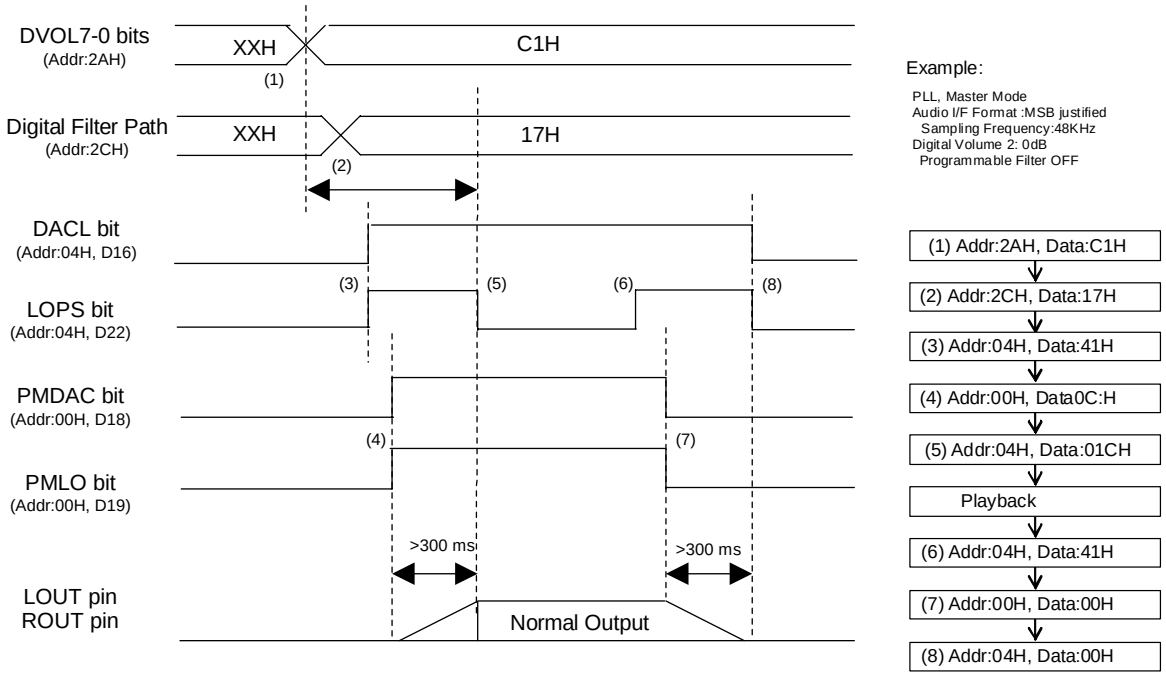


Figure 73. Stereo Lineout Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up output digital volume 2 (Addr = 2AH)

(2) Set up Programmable Filter Path (PFDAC, ADCPF and PFSDO bits). (Addr = 2CH)

(3) Set up the path of "DAC → Stereo Lime-Amp": DACL bit = "0" → "1" (Addr = 04H)
Set stereo lime amp to power save mode. LOPS bit = "0" → "1"

(4) Power up DAC and Stereo Line-Amp: PMDAC = PMLO bits = "0" → "1" (Addr = 00H)
LOUT and ROUT pins rise up to VCOM voltage after PMLO bit is changed to "1". Rise time is 300ms(max.) at C=1μF and AVDD=1.8V.

(5) Exit power-save mode of Stereo Line-Amp: LOPS bit = "1" → "0" (Addr=04H)
LOPS bit should be set to "0" after LOUT and ROUT pins rise up. Stereo Line-Amp goes to normal operation by setting LOPS bit to "0".

(6) Enter power save mode of Stereo Line-Amp: LOPS bit = "0" → "1" (Addr = 04H)

(7) Power down DAC and Stereo Line-Amp: PMDAC=PMLO= "1" → "0". (Addr=00H)
LOUT and ROUT pins fall down to VSS1. Fall time is 300ms (max.) at C=1μF and AVDD=1.8V.

(8) Disable the path of "DAC → Stereo Line-Amp": DACL bit = "1" → "0" (Addr=04H)
Exit power-save mode of the Stereo-Line Amp: LOPS bit = "1" → "0"
LOPS bit should be set to "0" after LOUT and ROUT pins fall down.

■ Mono Output Signal from Speaker

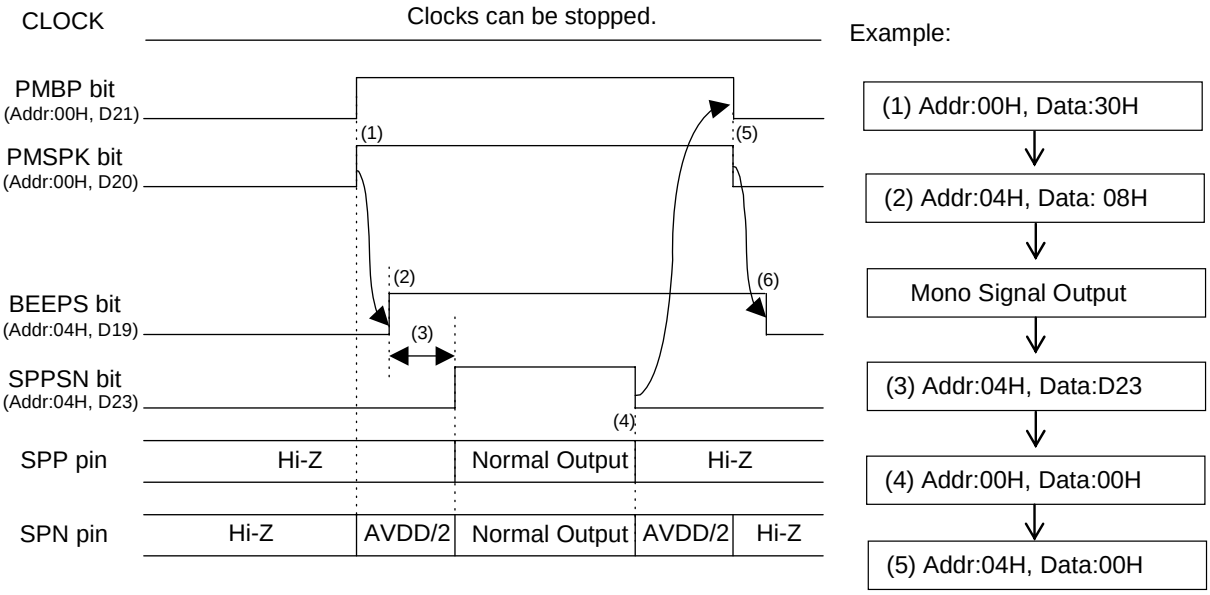


Figure 74. "MIN-Amp → Speaker-Amp" Output Sequence

<Example>

When only the path of "MIN-Amp → SRK-Amp" is in operation, the clocks are not needed.

(1) Power up MIN-Amp and Speaker-Amp: PMBP = PMSPK bits = "0" → "1"

(2) Disable the path of "DAC → SPK-Amp": DACS bit = "0"
Enable the path of "MIN → SPK-Amp": BEEPS bit = "0" → "1"

(3) Exit power-save mode of SPK-Amp: SPPSN bit = "0" → "1"
This period should be set in accordance with the time constant of the capacitor (C) and resistor (R) connected to the MIN pin. Pop noise may occur if the SPK-Amp output is enabled before the MIN-Amp input is stabilized. e.g. R=33kΩ, C=0.1μF: Recommended waiting time is 5τ = 16.5ms or more.

(4) Enter power-save mode of the SPK-Amp: SPPSN bit = "1" → "0"

(5) Power down MIN-Amp and SPK-Amp: PMBP = PMSPK bits = "1" → "0"

(6) Disable the path of "MIN → SPK-Amp": BEEPS bit = "1" → "0"

■ Video Input/Output

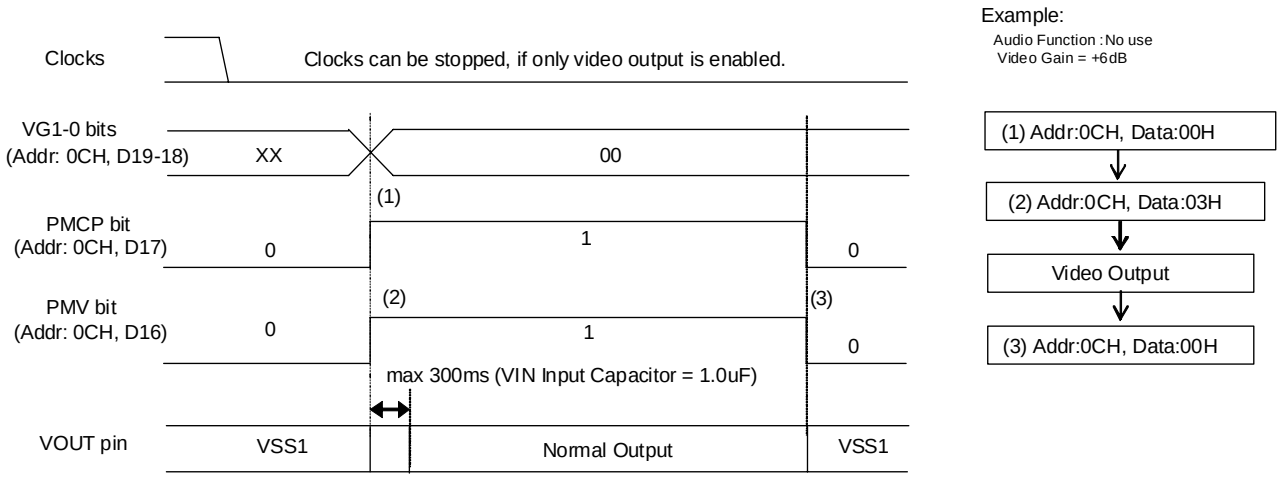


Figure 75. Video Output Sequence

<Example>

When only the video block is in operation, the clocks are not needed.

(1) Set up the video gain (VG1-0 bits).

(2) Power up Video Amp and Charge Pump: PMV, PMCP bits = "0" → "1"

It takes maximum 300ms to a stable operation of clamp circuit. (input capacitor at the VIN pin = 1.0uF)

(3) Power down Video Amp: PMV, PMCP bits = "0" → "1"

The VOUT pin output is stopped and becomes 0V.

■ Stop of Clock

Master clock can be stopped when ADC, DAC, Digital MIC and Programmable Filter are not in operation.

1. PLL Master Mode

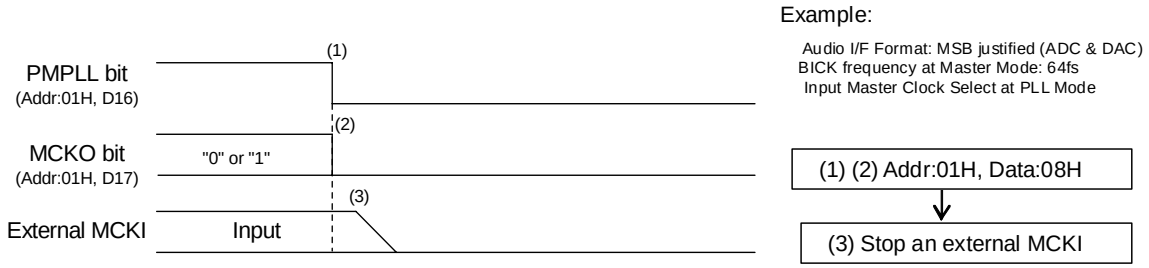


Figure 76. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop the external master clock.

2. PLL Slave Mode (BICK pin)

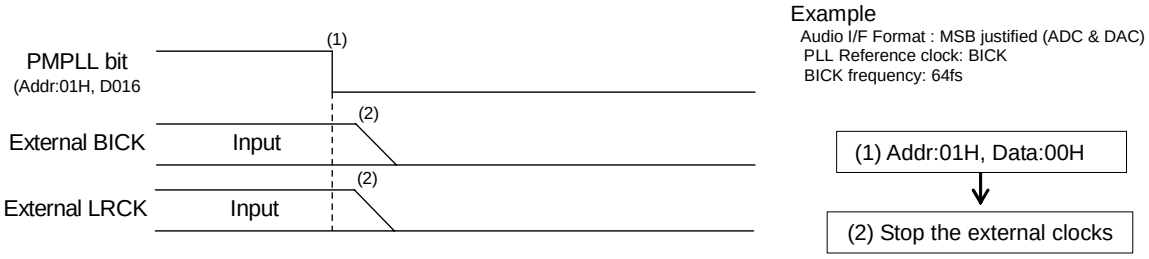


Figure 77. Clock Stopping Sequence (2)

<Example>
(1) Power down of the PLL: PMPLL bit = "1" → "0"
(2) Stop the external master clock.

3. PLL Slave Mode (MCKI pin)

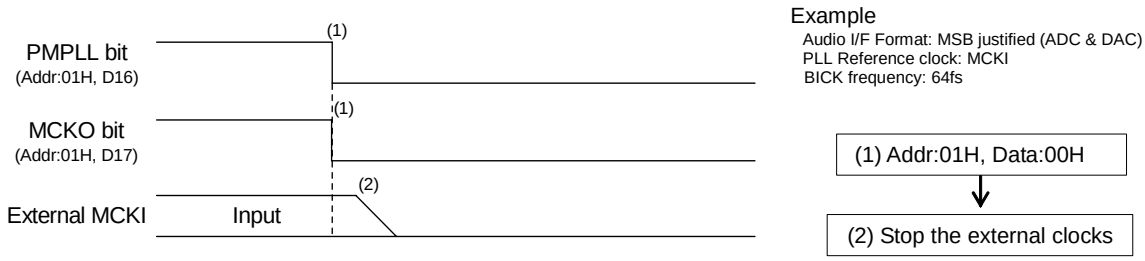


Figure 78. Clock Stopping Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
Stop the MCKO output: MCKO bit = "1" → "0"
(2) Stop the external master clock.

4. External Clock Mode

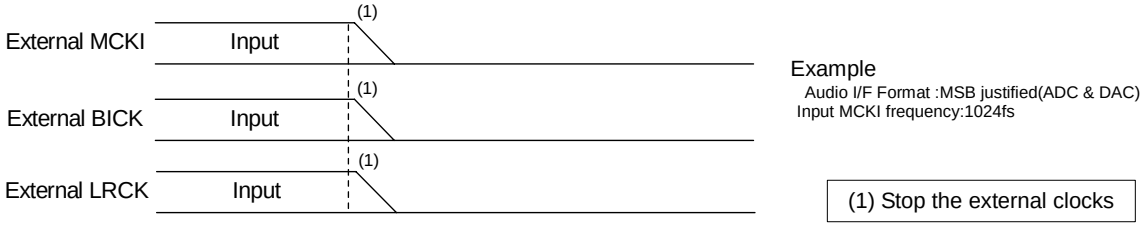


Figure 79. Clock Stopping Sequence (4)

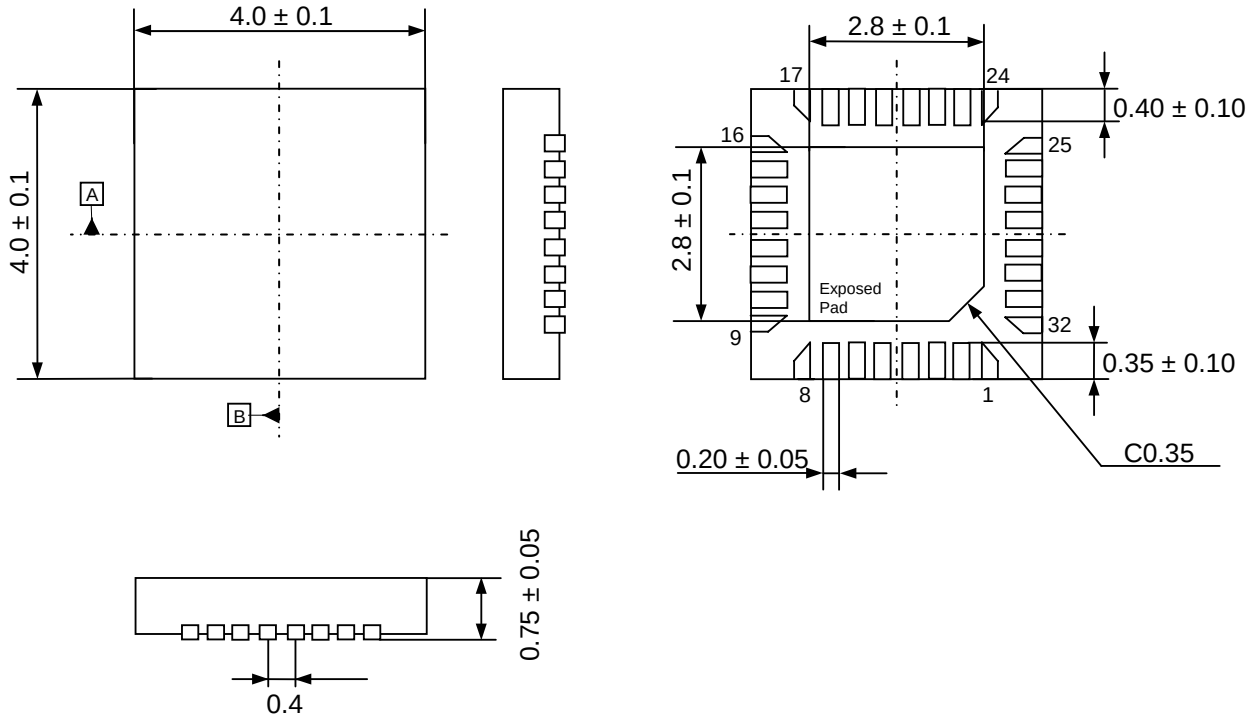
<Example>
(1) Stop the external MCKI, BICK and LRCK clocks.

■ Power Down

Power supply current can be shut down (typ. 1μA) by stopping clocks and setting PDN pin = "L". When the PDN pin = "L", the registers are initialized.

PACKAGE

32pin QFN (Unit: mm)

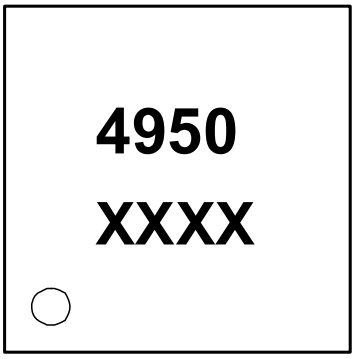


Note: The exposed pad on the bottom surface of the package must be connected to the ground.

■ Material & Lead Finish

Package molding compound: Epoxy resin, Halogen (Br and Cl) free
Lead frame material: Cu alloy
Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXX: Date code (4 digit)
Pin #1 indication

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
11/10/13	00	First Edition		

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