= Target Spec =

AK4704

2ch 24bit DAC with AV SCART switch

GENERAL DESCRIPTION

The AK4704 offers the ideal features for digital set-top-box systems. Using AKM's multi-bit architecture for its modulator, the AK4704 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4704 integrates a combination of SCF and CTF filters, removing the need for high cost external filters and increasing performance for systems with excessive clock jitter. The AK4704 also including the audio switches, volumes, video switches, video filters, etc. designed primarily for digital set-top-box systems. The AK4704 is offered in a space saving 48-pin LQFP package.

FEATURES

DAC
- ☐ Sampling Rates Ranging from 8kHz to 50kHz
- ☐ 64dB High Attenuation 8x FIR Digital Filter
- ☐ 2nd order Analog LPF
- ☐ On chip Buffer with Single-ended Output
- ☐ Digital de-emphasis for 32k, 44.1k and 48kHz sampling
- ☐ I/F format: 24bit MSB justified, I^2S, 18/16bit LSB justified
- ☐ Master clock: 256fs, 384fs
- ☐ High Tolerance to Clock Jitter

Analog switches for SCART

Audio section
- ☐ THD+N: -86dB (@2Vrms)
- ☐ Dynamic Range: 96dB (@2Vrms)
- ☐ Stereo Analog Volume with Zero-cross Detection Circuit (+6dB to –60dB & Mute)
- ☐ Six Analog Inputs
  - Two Stereo Input (TV&VCR SCART)
  - One Stereo Input (changeover to internal DAC)
- ☐ Five Analog Outputs
  - Two Stereo Outputs (TV, VCR SCART)
  - One Mono Output (Modulator)
- ☐ Pop Noise Free Circuit for Power on/off

Video section
- ☐ Integrated LPF: -40dB@27MHz
- ☐ 75ohm driver
- ☐ 6dB Gain for Outputs
- ☐ Adjustable gain
- ☐ Four CVBS/Y inputs (ENCx2, TV, VCR), Three CVBS/Y output (RF, TV, VCR)
- ☐ Three R/C inputs (ENCx2, VCR), Two R/C output (TV, VCR)
- ☐ Bi-directional control for VCR-Chroma/Red
- ☐ Two G and B inputs (ENC, VCR), One G and B outputs (TV)
- ☐ Y/C Mixer for RF output
- ☐ VCR input monitor

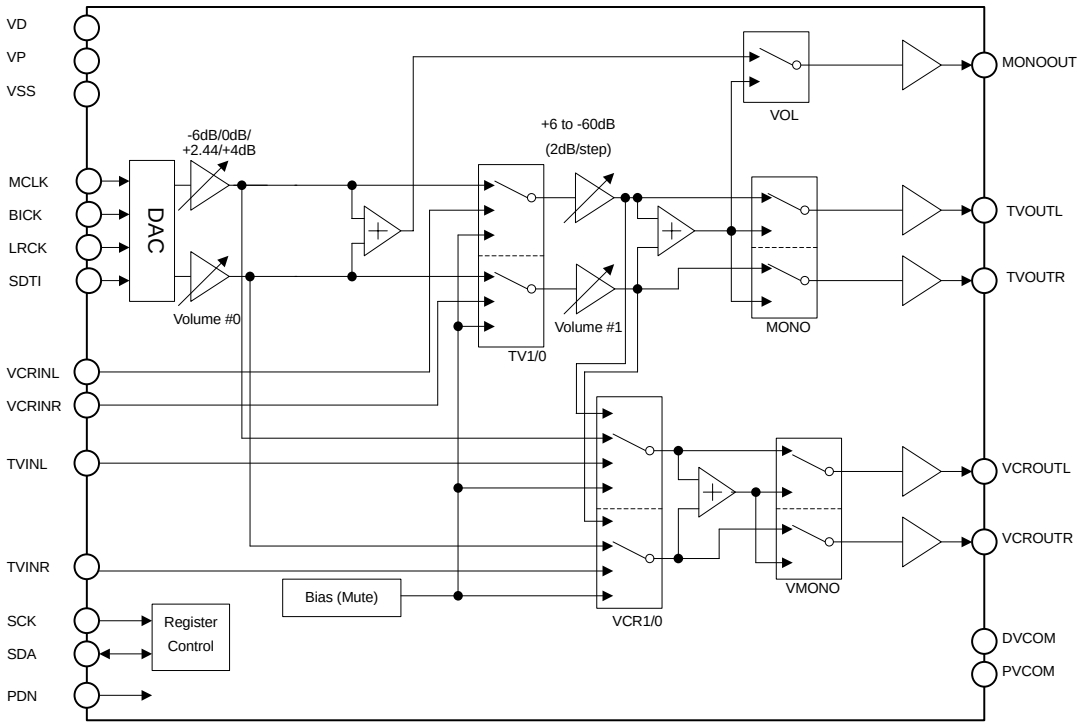
Loop-through Mode for standby

Auto-Startup Mode for power saving

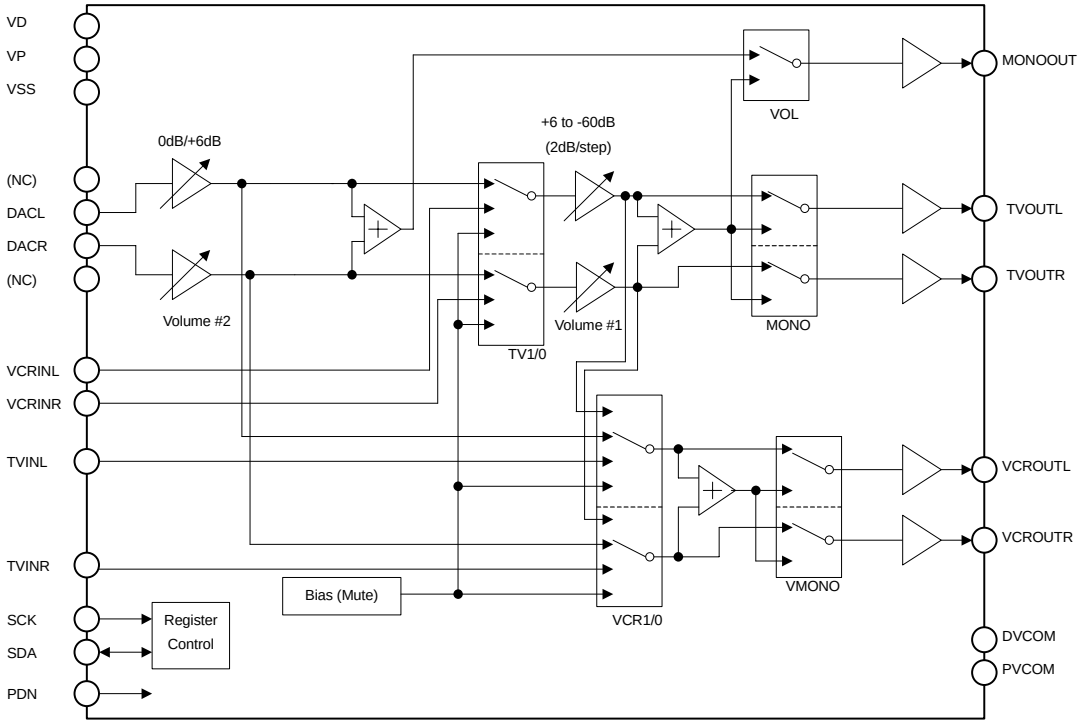
SCART pin#16(Fast Blanking), pin#8(Slow Blanking) Control

Power supply
- ☐ 5V+/-5% and 12V+/-5%
- ☐ Low Power Dissipation / Low Power Standby Mode

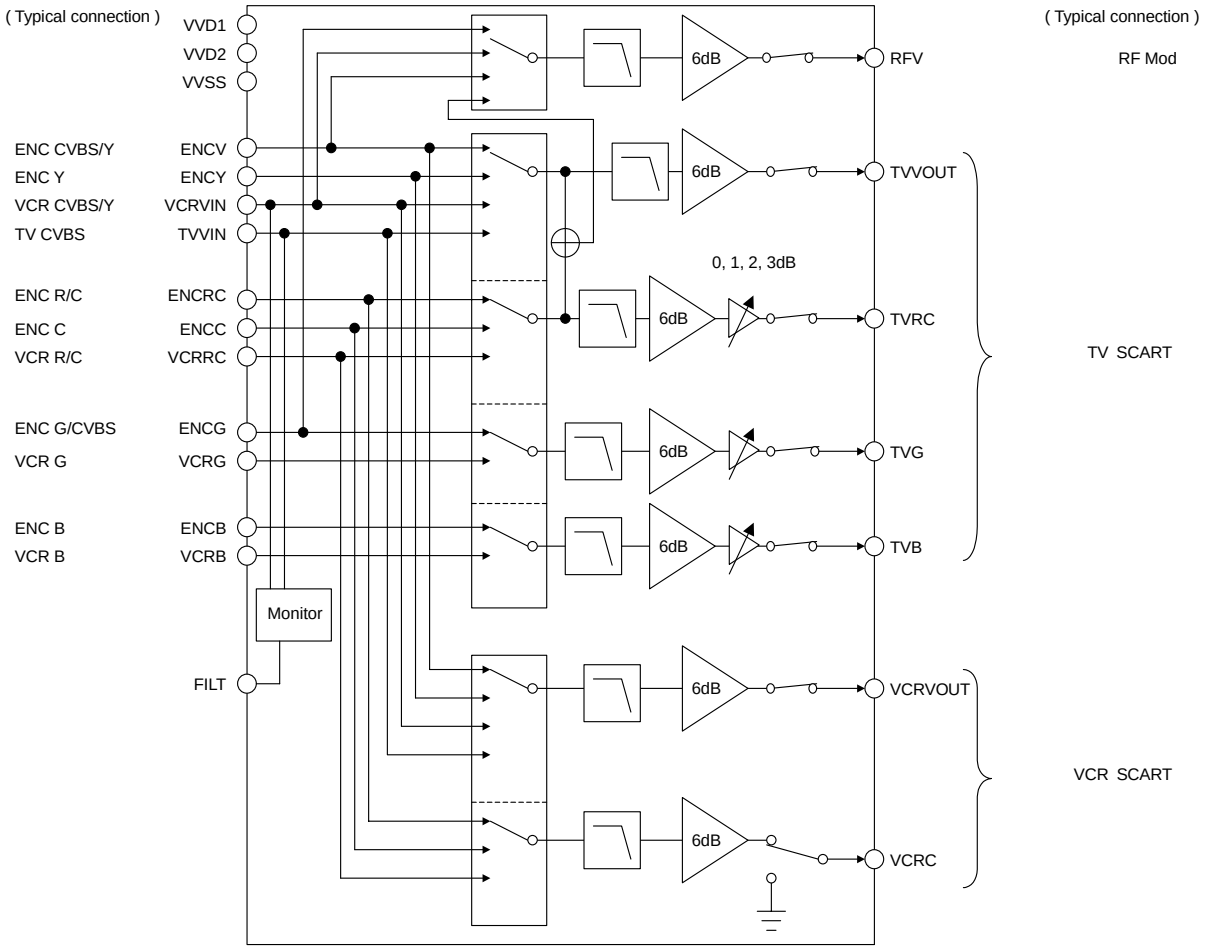
Package
- ☐ Small 48pin LQFP



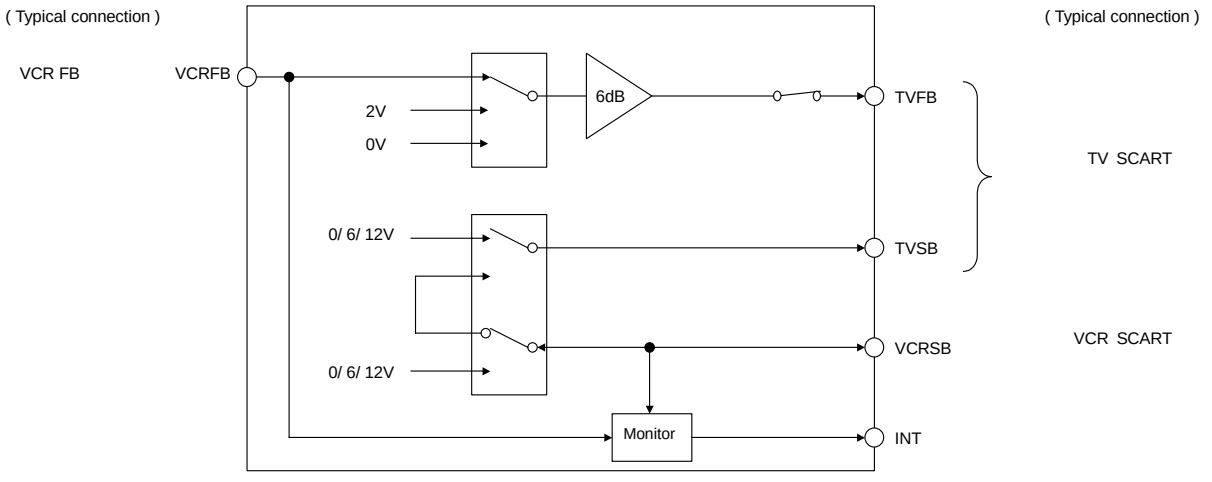
Audio Block(DAPD="0")



Audio Block(DAPD="1")



Video Block

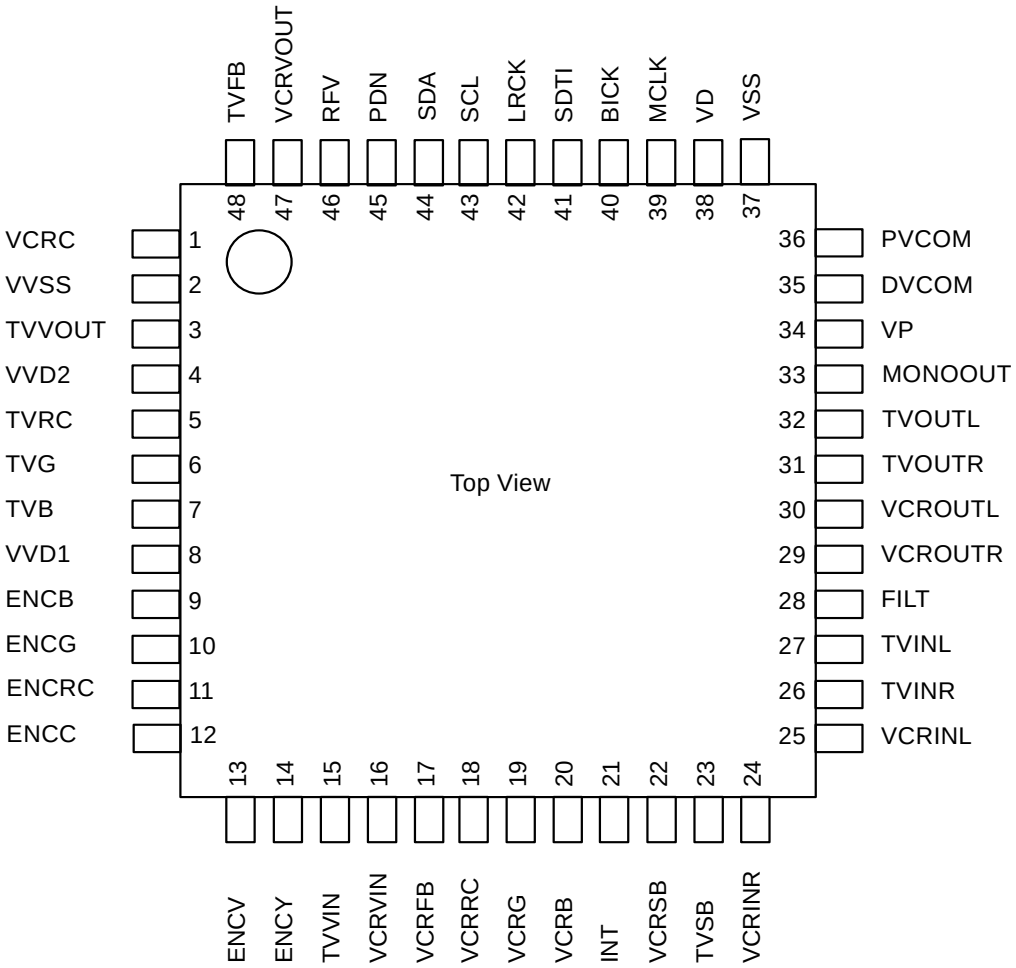


Video Blanking Block

■ Ordering Guide

AK4704	-10 ~ +70°C	48pin LQFP (0.5mm pitch)

■ Pin Layout



■ Main difference between AK4702 and AK4704

Items		AK4702	AK4704
Audio	Audio bits	18bit	24bit
	Digital filter attenuation level	54dB	64dB
	+4dB gain at DAC volume#0 (total: +10dB max)	-	X
	DAC power-down/analog input mode	-	X
	Volume#1 output for VCROUTL/R switch matrix	-	X
	MONO mixing for VCROUTL/R	-	X
	MONO input	X	-
Video	Video filter	-	X
	150ohm video driver for modulator	-	X
	Y/C mixer for modulator	-	X
	VCR video input monitor	-	X
	VCR Slow Blanking monitor in output mode.	enabled	disabled
	TV/VCR CVBS input detection & Power Save Mode	-	X
Others	I^2C speed (max)	100kHz	400kHz
	Mask bits for INT function (09H)	-	X

-: NOT available. X: Available

PIN/FUNCTION

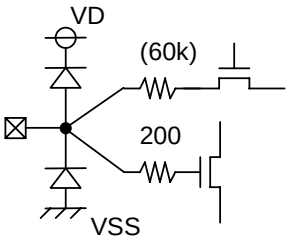
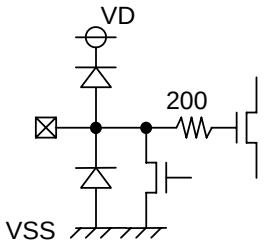
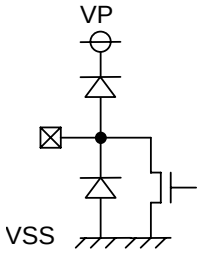
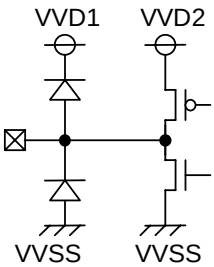
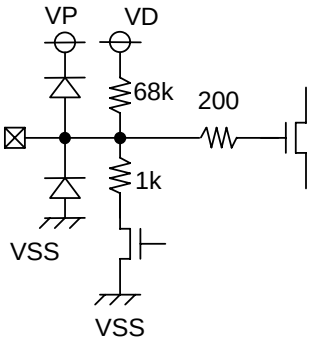
No.	Pin Name	I/O	Function
1	VCRC	O	Chrominance Output Pin for VCR
2	VVSS	-	Video Ground Pin. 0V.
3	TVVOUT	O	Composite/Luminance Output Pin for TV
4	VVD2	-	Video Power Supply Pin #2. 5V. Normally connected to VVSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
5	TVRC	O	Red/Chrominance Output Pin for TV
6	TVG	O	Green Output Pin for TV
7	TVB	O	Blue Output Pin for TV
8	VVD1	-	Video Power Supply Pin #1. 5V. Normally connected to VVSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
9	ENCB	I	Blue Input Pin for Encoder
10	ENCG	I	Green Input Pin for Encoder
11	ENCRC	I	Red/Chrominance Input Pin1 for Encoder
12	ENCC	I	Chrominance Input Pin2 for Encoder
13	ENCV	I	Composite/Luminance Input Pin1 for Encoder
14	ENCY	I	Composite/Luminance Input Pin2 for Encoder
15	TVVIN	I	Composite/Luminance Input Pin for TV
16	VCRVIN	I	Composite/Luminance Input Pin for VCR
17	VCRFB	I	Fast Blanking Input Pin for VCR
18	VCRRC	I	Red/Chrominance Input Pin for VCR
19	VCRG	I	Green Input Pin for VCR
20	VCRB	I	Blue Input Pin for VCR
21	INT	O	Interrupt Pin for Video Blanking
22	VCRSB	I/O	Slow Blanking Input/Output Pin for VCR
23	TVSB	O	Slow Blanking Output Pin for TV
24	VCRINR	I	Rch VCR Audio Input Pin
25	VCRINL	I	Lch VCR Audio Input Pin
26	TVINR	I	Rch TV Audio Input Pin
27	TVINL	I	Lch TV Audio Input Pin
28	FILT	O	Filter Pin Normally connected to VVSS with a 0.1μF ceramic capacitor.
29	VCROUTR	O	Rch Analog Output Pin1
30	VCROUTL	O	Lch Analog Output Pin1
31	TVOUTR	O	Rch Analog Output Pin2
32	TVOUTL	O	Lch Analog Output Pin2
33	MONOOUT	O	MONO Analog Output Pin
34	VP	-	Power Supply Pin. 12V. Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
35	DVCOM	O	DAC Common Voltage Pin Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
36	PVCOM	O	Audio Common Voltage Pin Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap. The caps affect the settling time of audio bias level.

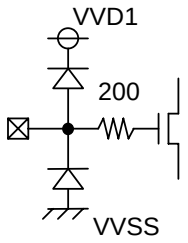
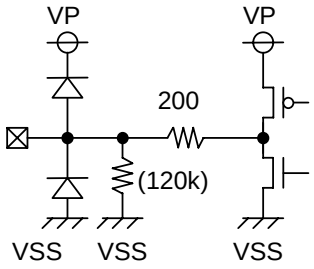
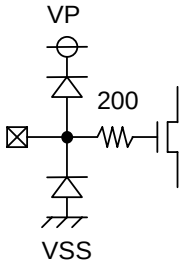
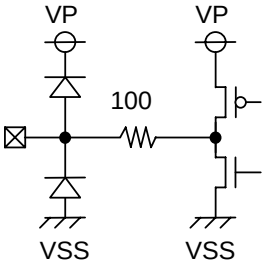
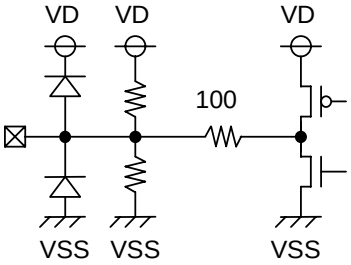
PIN/FUNCTION (Continued)

37	VSS	-	Ground Pin. 0V.
38	VD	-	DAC Power Supply Pin. 5V. Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
39	MCLK (NC)	I -	Master Clock Input Pin at DAPD="0". NC (No Connection) pin at DAPD="1".
40	BICK DACR	I -	Audio Serial Data Clock Pin at DAPD="0". Rch Analog Audio Input Pin at DAPD="1".
41	SDTI (NC)	I I	Audio Serial Data Input Pin at DAPD="0". NC (No Connection) pin at DAPD="1".
42	LRCK DACL	I I	L/R Clock Pin at DAPD="0". Lch Analog Audio Input Pin at DAPD="1".
43	SCL	I	Control Data Clock Pin
44	SDA	I/O	Control Data Pin
45	PDN	I	Power-Down Mode Pin When at "L", the AK4704 is in the power-down mode and is held in reset. The AK4704 should always be reset upon power-up.
46	RFV	O	Composite Output Pin for RF modulator
47	VCRVOUT	O	Composite/Luminance Output Pin for VCR
48	TVFB	O	Fast Blanking Output Pin for TV

Note: All input pins should not be left floating.

Internal Equivalent Circuits

Pin No.	Pin Name	Type	Equivalent Circuit	Description
39 40 41 42 43 45	MCLK BICK SDTI LRCK SCL PDN	Digital IN (DAPD="0") Analog IN (DAPD="1")		The 60kohm is attached only for BICK and LRCK.
44	SDA	Digital I/O		I2C Bus voltage must not exceed VD.
21	INT	Digital OUT		Normally connected to VD(5V) through 10kohm resistor externally.
46 47 48 1 3 5 6 7	RFV VCROUT TVFB VCRC TVVOUT TVRC TVG TVB	Video OUT		
28	FILT	Filter OUT		Normally connected to VVSS (0V) through 0.1µF capacitor externally.

Pin No.	Pin Name	Type	Equivalent Circuit	Description
9 10 11 12 13 14 15 16 17 18 19 20	ENCB ENCG ENCRC ENCC ENCV ENCY TVVIN VCRVIN VCRFB VCRRC VCRG VCRB	Video IN		
22 23	VCRSB TVSB	Video SB		The 120kohm is not attached for TVSB.
24 25 26 27	VCRINR VCRINL TVINR TVINL	Audio IN		
29 30 31 32 33	VCROUTR VCROUTL TVOUTR TVOUTL MONOOUT	Audio OUT		
35 36	DVCOM PVCOM	VCOM OUT		

ABSOLUTE MAXIMUM RATINGS

(VSS=VVSS=0V;Note: 1)

Parameter	Symbol	min	max	Units
Power Supply	VD	-0.3	6.0	V
	VVD1	-0.3	6.0	V
	VVD2	-0.3	6.0	V
	VP	-0.3	14	V
	|VSS-VVSS| (Note: 2)	-	0.3	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VD+0.3	V
Video Input Voltage	VINV	-0.3	VVD1+0.3	V
Audio Input Voltage (except DACL/R pins)	VINA	-0.3	VP+0.3	V
Audio Input Voltage (DACL/R pins)	VINA	-0.3	VD+0.3	V
Ambient Operating Temperature	Ta	-10	70	°C
Storage Temperature	Tstg	-65	150	°C

Note: 1. All voltages with respect to ground.
Note: 2. VSS and VVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=VVSS=0V; Note: 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VD	4.75	5.0	5.25	V
	VVD1=VVD2	4.75	5.0	5.25	V
	VP	11.4	12	12.6	V

Note: 3. Analog output voltage scales with the voltage of VD.
AOUT (typ@0dB) = 2Vrms × VD/5.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C; VP=12V, VD = 5V; VVD1=VVD2 = 5V; fs = 48kHz; BICK = 64fs)

Power Supplies				
Power Supply Current				
Normal Operation (PDN = "H"; Note: 4)				
VD		TBD	TBD	mA
VVD1+VVD2		TBD	TBD	mA
VP		TBD	TBD	mA
Power-Down Mode (PDN = "L"; Note: 5)				
VD		10	100	μA
VVD1+VVD2		10	100	μA
VP		10	100	μA

Note: 4. STBY bit ="L", All video outputs active.
No signal, no load for A/V switches. fs=48kHz "0"data input for DAC.
Note: 5. All digital inputs including clock pins (MCLK, BICK and LRCK) are held at VD or VSS.

DIGITAL CHARACTERISTICS

(Ta = 25°C; VD = 4.75 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.0	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
Low-Level Output Voltage (SDA pin: Iout= 3mA, INT pin: Iout= 1mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	± 100	μA

ANALOG CHARACTERISTICS (AUDIO)

(Ta = 25°C; VP=12V, VD = 5V; VVD1=VVD2 = 5V; fs = 48kHz; BICK = 64fs; Signal Frequency = 1kHz; 24bit Input Data; Measurement frequency = 20Hz ~ 20kHz; R_L ≥4.5kΩ; Volume #0=Volume #1=0dB, 0dB=2Vrms output; unless otherwise specified)

Parameter	min	typ	max	Units
DAC Resolution			24	bit
Analog Input: (TVINL/TVINR/VCRINL/VCRINR pins)				
Analog Input Characteristics				
Input Voltage			2	Vrms
Input Resistance	100	150	-	kΩ
Analog Input: (DACL/DACR pin)				
Analog Input Characteristics				
Input Voltage			1	Vrms
Input Resistance	TBD	TBD	-	kΩ
Stereo/Mono Output: (TVOUTL/TVOUTR/VCROUTL/VCROUTR/MONOOUT pins; Note: 6)				
Analog Output Characteristics				
Volume#0 Gain (DVOL1-0 = "00")		0		dB
(DVOL1-0 = "01")		-6		dB
(DVOL1-0 = "10")		+2.44		dB
(DVOL1-0 = "11". Note: 7)		+4		dB
Volume#1 Step Width (+6dB to –12dB)	1.6	2	2.4	dB
(-12dB to –40dB)	0.5	2	3.5	dB
(-40dB to –60dB)	0.1	2	3.9	dB
THD+N (at 2Vrms output. Note: 8)		-86	-80	dB
(at 3Vrms output. Note: 8, Note: 9)		-60	-	dB
Dynamic Range (-60dB Output, A-weighted. Note: 8)	92	96		dB
S/N (A-weighted. Note: 8)	92	96		dB
Interchannel Isolation (Note: 8, Note: 10)	80	90		dB
Interchannel Gain Mismatch (Note: 8, Note: 10)	-	0.3	-	dB
Gain Drift	-	200	-	ppm/°C
Load Resistance (AC-Lord; Note: 11) TVOUTL/R, VCROUTL/R, MONOOUT	4.5			kΩ
Output Voltage (Note: 11, Note: 12)	1.85	2	2.15	Vrms
Power Supply Rejection (PSR. Note: 13)	-	50		dB

Note: 6. Measured by Audio Precision System Two Cascade.
Note: 7. Output clips over –2.5dBFS digital input.
Note: 8. DAC to TVOUT
Note: 9. Except VCROUTL/VCROUTL pins.
Note: 10. Between TVOUTL and TVOUTR with digital inputs 1kHz/0dBFS.
Note: 11. THD+N : -80dB(min. at 2Vrms), -60dB(typ. at 3Vrms).
Note: 12. Full-scale output voltage by DAC (0dBFS). Output voltage of DAC scales with the voltage of VD, Stereo output (typ@0dBFS) = 2Vrms × VD/5 when volume#0=volume#1=0dB. Do not output signals over 3Vrms.
Note: 13. The PSR is applied to VD with 1kHz, 100mV.

FILTER CHARACTERISTICS

(Ta = 25°C; VP=11.4~12.6V, VD = 4.75~5.25V, VVD1=VVD2 = 4.75~5.25V; fs = 48kHz; DEM0 = "1", DEM1 = "0")

Parameter	Symbol	min	typ	max	Units
Digital filter					
Passband ±0.05dB (Note: 14)	PB	0		21.77	kHz
-6.0dB		-	24.0	-	kHz
Stopband (Note: 14)	SB	26.23			kHz
Passband Ripple	PR			± 0.01	dB
Stopband Attenuation	SA	64			dB
Group Delay (Note: 15)	GD	-	24	-	1/fs
Digital Filter + LPF					
Frequency Response 0 ~ 20.0kHz	FR	-	± 0.5	-	dB

Note: 14. The passband and stopband frequencies scale with fs (system sampling rate).
e.g.) PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note: 15. The calculating delay time which occurred by digital filtering. This time is from setting the 16/18/24bit data of both channels to input register to the output of analog signal.

ANALOG CHARACTERISTICS (VIDEO)

(Ta = 25°C; VP=12V, VD = 5V; VVD1=VVD2 = 5V; VVOL1/0= "00", YC="0" unless specified.)

Parameter	Conditions		min	typ	max	Units
Sync Tip Clamp Voltage	at output pin.			0.7		V
Chrominance Bias Voltage	at output pin.			2.2		V
Gain	Input=0.3Vp-p, 100kHz		5.5	6	6.5	dB
RGB Gain	Input=0.3Vp-p, 100kHz	VVOL1/0= "00"	5.5	6	6.5	dB
		VVOL1/0= "01"	6.7	7.2	7.7	dB
		VVOL1/0= "10"	7.7	8.2	8.7	dB
		VVOL1/0= "11"	8.6	9.1	9.6	dB
Interchannel Gain Mismatch	TVRC, TVG, TVB. Input=0.3Vp-p, 100kHz.		-0.3	-	0.3	dB
Frequency Response	Input=0.3Vp-p, C1=C2=0pF. 100kHz to 6MHz.		-1.0		0.5	dB
	at 12MHz.			-3		dB
	at 27MHz.			-40	-35	dB
Group Delay Distortion	At 4.43MHz with respect to 1MHz.				15	ns
Input Impedance	Chrominance input (internally biased)		40	60	-	kohm
Input Signal	f=100kHz, maximum with distortion < 1.0%, gain=6dB.		-	-	1.5	Vpp
Load Resistance	(Note: 16)		150	-	-	ohm
Load Capacitance	C1 (Note: 16)				400	pF
	C2 (Note: 16)				15	pF
Dynamic Output Signal	f=100kHz, maximum with distortion < 1.0%		-	-	3	Vpp
Y/C Crosstalk	f=4.43MHz, 1Vp-p input. Among TVVOUT, TVRC, VCRVOUT and VCRC outputs.		-	-50	-	dB
S/N	Reference Level = 0.7Vp-p, CCIR 567 weighting. BW= 15kHz to 5MHz.		-	74	-	dB
Differential Gain	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.		-	TBD	-	%
Differential Phase	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.		-	TBD	-	Degree

Note: 16. Refer the Figure 1.

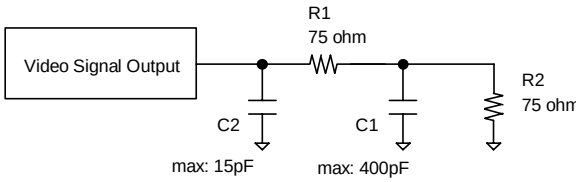


Figure 1. Load Resistance R1+R2 and Load Capacitance C1/C2.

SWITCHING CHARACTERISTICS

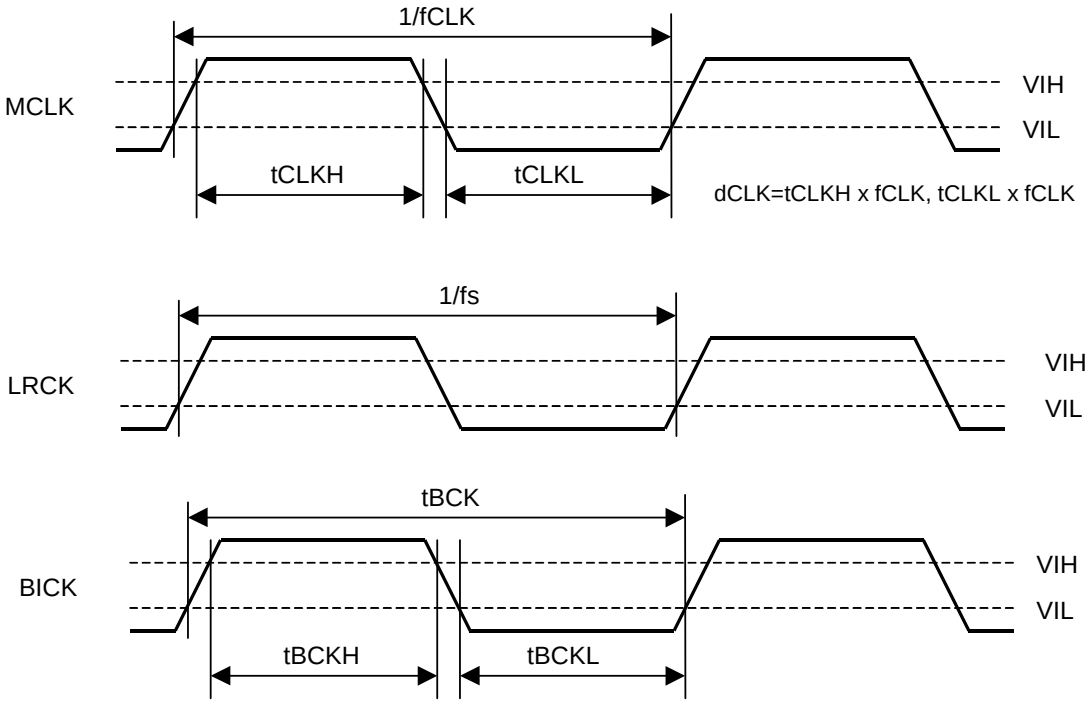
(Ta = 25°C; VP=11.4 ~ 12.6V, VD = 4.75 ~ 5.25V, VVD1=VVD2 = 4.75 ~ 5.25V; C_L = 20pF)

Parameter	Symbol	Min	typ	max	Units
Master Clock Frequency 256fs:	fCLK	2.048		12.8	MHz
Duty Cycle	dCLK	40		60	%
384fs:	fCLK	3.072		19.2	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency	fs	8		50	kHz
Duty Cycle	Duty	45		55	%
Audio Interface Timing					
BICK Period	tBCK	312.5			ns
BICK Pulse Width Low	tBCKL	100			ns
Pulse Width High	tBCKH	100			ns
BICK "↑" to LRCK Edge (Note: 17)	tBLR	50			ns
LRCK Edge to BICK "↑" (Note: 17)	tLRB	50			ns
SDTI Hold Time	tSDH	50			ns
SDTI Setup Time	tSDS	50			ns
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note: 18)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Reset Timing					
PDN Pulse Width (Note: 19)	tPD	150			ns

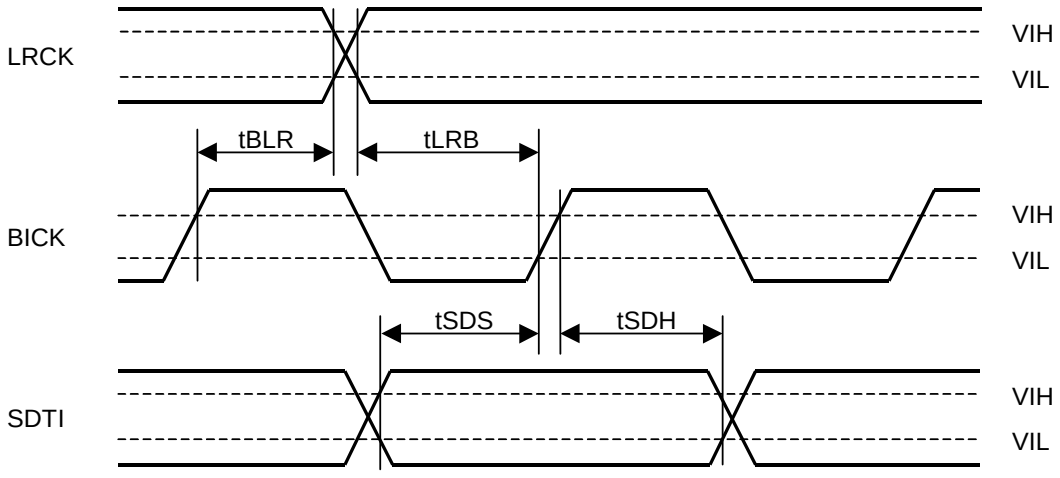
Note: 17. BICK rising edge must not occur at the same time as LRCK edge.
Note: 18. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note: 19. The AK4704 should be reset by PDN= "L" upon power up.
Note: 20. I^2C is a registered trademark of Philips Semiconductors.

Purchase of Asahi Kasei Microsystems Co., Ltd I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conform to the I^2C specifications defined by Philips.

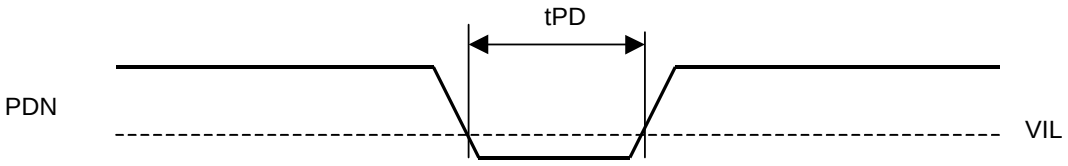
■ Timing Diagram



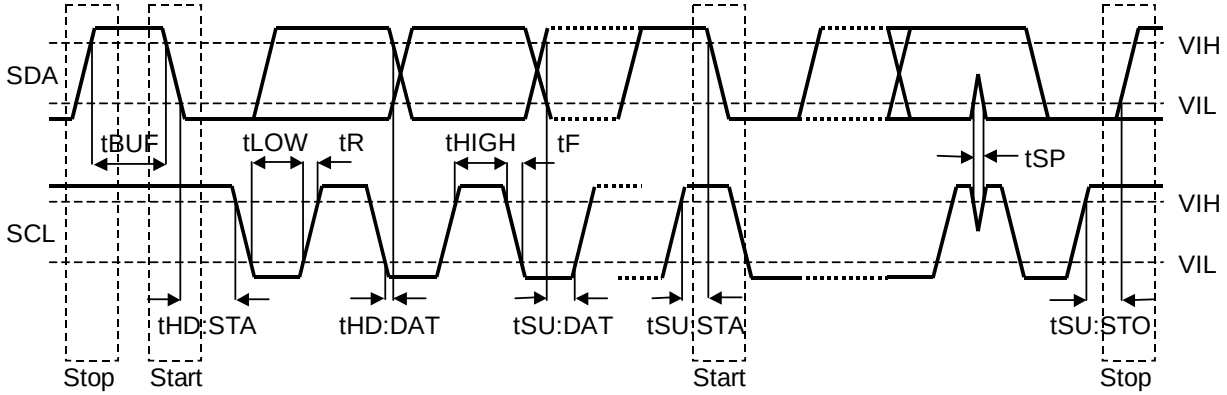
Clock Timing



Serial Interface Timing



Power-down Timing



I^2C Bus mode Timing

OPERATION OVERVIEW

1. System Reset and Power-down options

The AK4704 should be reset once by bringing PDN pin = "L" upon power-up. The AK4704 has several operation modes. The PDN pin, AUTO bit, DAPD bit, MUTE bit and STBY bit control operation modes as shown in Table 1 and Table 2.

Mode	PDN pin	AUTO bit	STBY bit	MUTE bit	DAPD bit	Mode
0	"L"	*	*	*	*	Full Power-down
1	"H"	1	*	*	*	Auto Startup mode (power-on default)
2	"H"	0	1	1	*	Standby & mute
3	"H"	0	1	0	*	Standby
4	"H"	0	0	1	1	Mute (DAC power down)
5	"H"	0	0	1	0	Mute (DAC operation)
6	"H"	0	0	0	1	Normal operation (DAC power down & Analog input)
7	"H"	0	0	0	0	Normal operation (DAC operation)

*: Don't Care

Table 1. Operation Mode Settings

Mode			Register Control	MCLK, BICK, LRCK	Audio Bias Level	Video Output	TVFB, TVSB	VCRSB
0	Full Power-down		NOT available	Not needed	Power down	Hi-Z	Hi-Z	Pull-Down (**)
1	Auto Startup mode (power-on default)	No video input	Available					
		Video input (***)			Active	Active (****)	Active	Active
2	Standby & mute				Power down	Hi-Z/ Active		
3	Standby				Active			
4	Mute (DAC power down)				Power down			
5	Mute (DAC operation)			Needed				
6	Normal operation (DAC power down & Analog input)			Not needed	Active (*)			
7	Normal operation (DAC operation)			Needed				

(*): TVOUTL/R are muted by VMUTE bit in the default state.
(**): Internally pulled down by 120kohm(typ) resister.
(***): Video input to TVVIN or VCRVIN.
(****): VCRC outputs 0V for termination.

Table 2. Status of each operation modes

■ Full Power-down Mode

The AK4704 should be reset once by bringing PDN= ”L” upon power-up.

PDN pin: Power down pin
- “H”: Normal operation
- “L”: Device power down.

■ Auto Startup Mode

After when the PDN pin is set to “H”, the AK4704 is in the auto startup mode. In this mode, all blocks except for the video detection circuit are powered down. Once the video detection circuit detects video signal from TVVIN pin or VCRVIN pin, the AK4704 goes to the stand-by mode automatically and sends “H” pulse via INT pin. To exit the auto startup mode, set the AUTO bit to “0”.

AUTO bit (00H D3): Auto startup bit
- “1”: Auto startup enable (default).
- “0”: Auto startup disable (Manual startup).

■ DAC Power-down Mode

The internal DAC block can be powered-down and switched to 1Vrms analog input mode. When DAPD bit =“1”, the zero-cross detection and offset calibration does not work.

DAPD bit (00H D2): DAC power-down bit.
- “1”: DAC power-down. Analog-input mode.
  - #39 pin: MCLK -> (NC)
  - #40 pin: BICK -> DACR. Rch analog input.
  - #41 pin: SDTI -> (NC)
  - #42 pin: LRCK -> DACL. Lch analog input.
- “0”: DAC operation. (default)

■ Standby Mode

When the AUTO bit = MUTE bit = “0” and the STBY bit = “1”, the AK4704 is forced into TV-VCR loop through mode. In this mode, the sources of TVOUTL/R and MONOOUT pins are fixed to VCRINL/R pins; the sources of VCROUTL/R are fixed to TVINL/R pins respectively. The gain of volume#1 is fixed to 0dB. All register values themselves are NOT changed by STBY bit = “1”.

STBY bit (00H D0): Standby bit.
- “1”: Standby mode. (default)
- “0”: Normal operation.

■ Mute Mode (Bias-off Mode. 00H: D1)

When the MUTE bit = “1”, the bias voltage on the audio output goes to GND level. Bringing MUTE bit to “0” changes this bias voltage smoothly from GND to VP/2 by 2sec(typ.). This removes the huge click noise related the sudden change of bias voltage at power-on. The change of MUTE bit from “1” to “0” also makes smooth transient from VP/2 to GND by 2sec(typ). This removes the huge click noise related the sudden change of bias voltage at power-off.

MUTE bit: Bias-off bit.
- “1”: Set the audio bias to GND. (default)
- “0”: Normal operation

■ Normal Operation Mode

To use the DAC or change analog switches, set the AUTO bit, DAPD bit, MUTE bit and STBY bit to “0”. The DAC is in power-down mode until MCLK and LRCK are input. The AK4704 is in power-down mode until MCLK and LRCK are input. The Figure 2 shows an example of the system timing at the power-down and power-up by PDN pin.

■ Typical Operation Sequence (auto setup mode)

The Figure 2 shows an example of the system timing at auto setup mode.

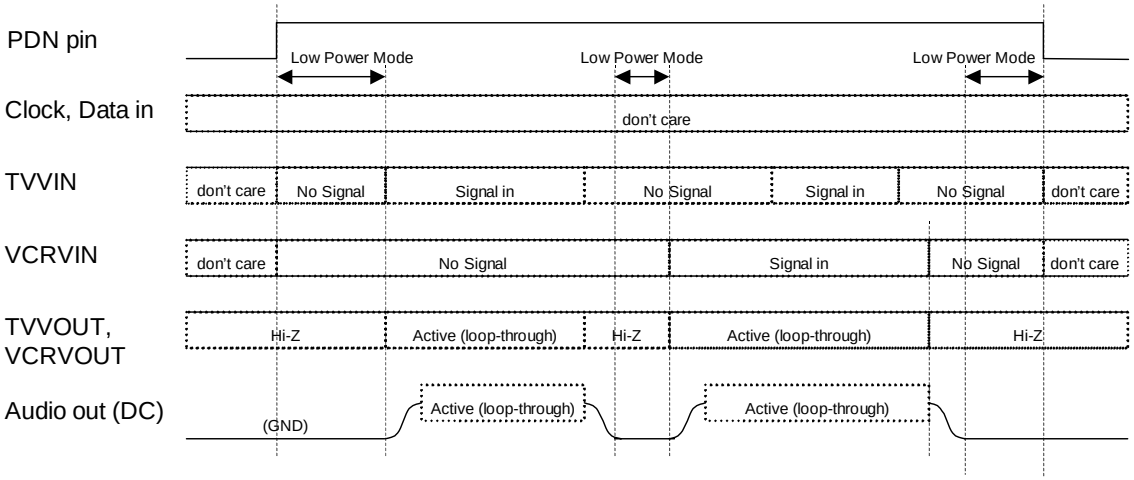
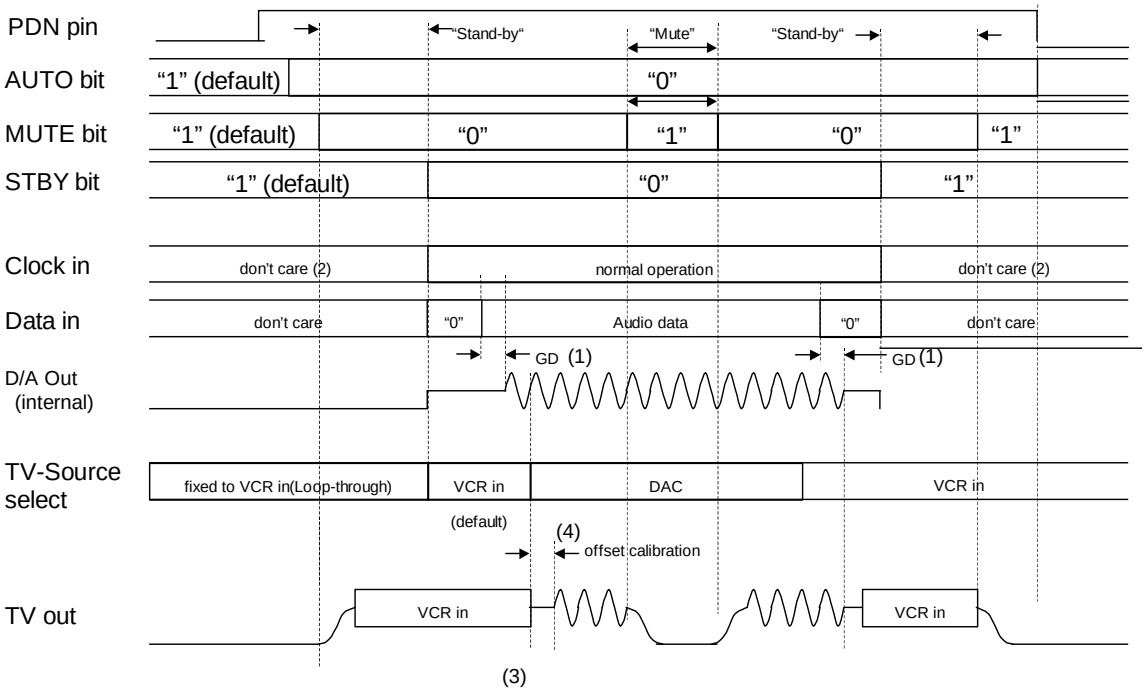


Figure 2. Typical operating sequence (auto setup mode)

■ Typical Operation Sequence (except auto setup mode)

The Figure 3 shows an example of the system timing at auto setup mode.



Notes:

(1) The analog output corresponding to the digital input has a group delay, GD.
(2) The external clocks (MCLK, BICK and LRCK) can be stopped in standby mode.
(3) Mute the analog outputs externally if click noise(3) adversely affects the system.
(4) In case of the CAL bit = "1", the offset calibration is always executed when the source of TVOUTL/R pins are switched to DAC after the STBY bit is changed to "0". To disable this function, set the CAL bit = "0".

Figure 3. Typical operating sequence (except auto setup mode)

2. Audio Block

■ System Clock

The external clocks required to operate the DAC section of AK4704 are MCLK, LRCK and BICK. The master clock (MCLK) corresponds to 256fs or 384fs. MCLK frequency is automatically detected, and the internal master clock becomes 256fs. The MCLK should be synchronized with LRCK but the phase is not critical. Table 3 illustrates corresponding clock frequencies. All external clocks (MCLK, BICK and LRCK) should always be present whenever the DAC section of AK4704 is in the normal operating mode (STBY bit = "0" and DAPD bit = "0"). If these clocks are not provided, the AK4704 may draw excess current because the device utilizes dynamically refreshed logic internally. The DAC section of AK4704 should be reset by STBY bit = "0" after three clocks are provided. If the external clocks are not present, place the AK4704 in power-down mode (STBY bit = "1"). After exiting reset at power-up etc., the AK4704 remains in power-down mode until MCLK and LRCK are input.

LRCK	MCLK		BICK
fs	256fs	384fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	3.0720MHz

Table 3. System clock example

■ Audio Serial Interface Format (00H: D5-D4)

Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF0 and DIF1 bits can select four formats in serial mode as shown in Table 4. In all modes, the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can also be used for 16 MSB justified formats by zeroing the unused two LSBs.

Mode	DIF1	DIF0	SDTI Format	BICK	Figure	
0	0	0	16bit LSB Justified	≥32fs	Figure 4	
1	0	1	18bit LSB Justified	≥36fs	Figure 4	
2	1	0	24bit MSB Justified	≥48fs	Figure 5	
3	1	1	24bit I^2S Compatible	≥48fs or 32fs	Figure 6	Default

Table 4. Audio Data Formats

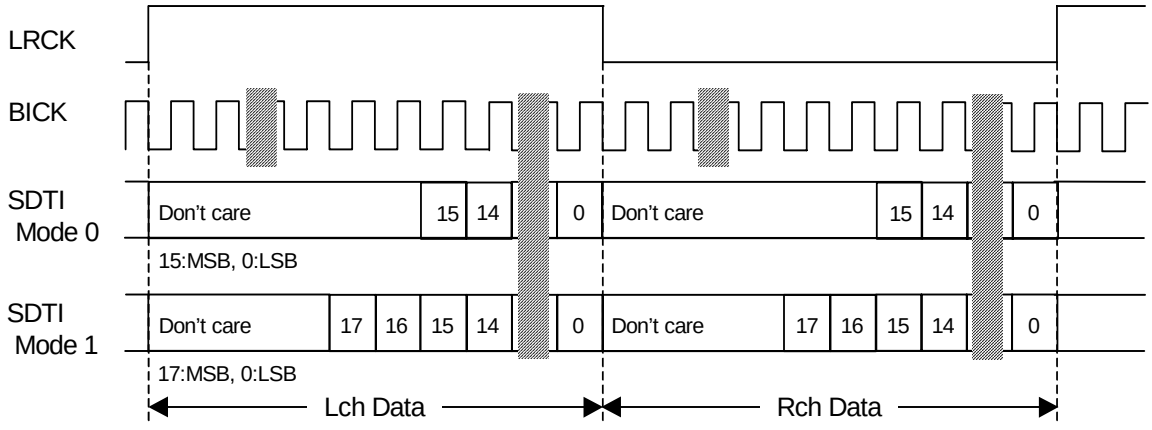


Figure 4. Mode 0,1 Timing

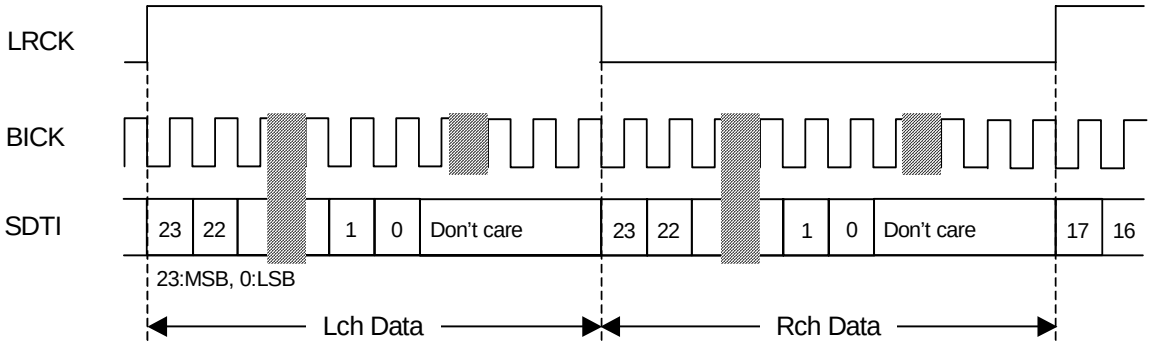


Figure 5. Mode 2 Timing

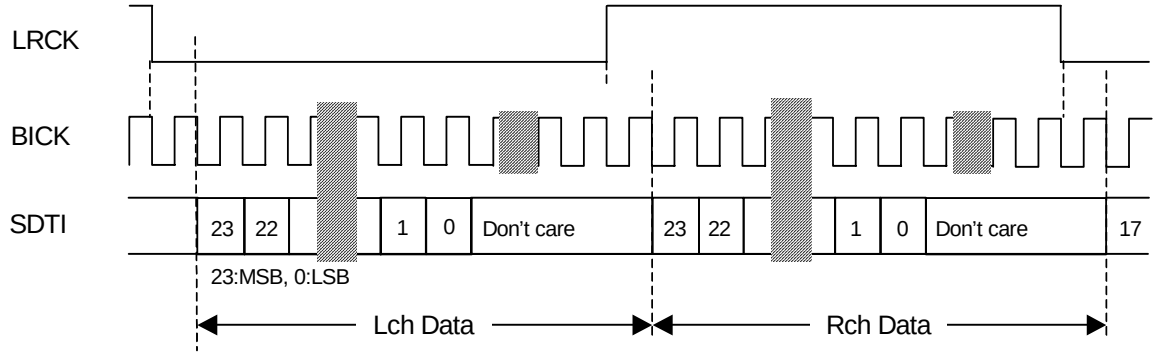


Figure 6. Mode 3 Timing

■ De-emphasis filter (00H: D7-D6)

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc = 50/15μs) and is controlled by the DEM0 and DEM1 bits.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 5. De-emphasis filter control

■ Volume/Switch Control

The AK4704 has analog volume controls and switch matrixes designed primarily for SCART routing. Those are controlled via the control register as shown in, Table 6, Table 8, Table 10 and Table 11 (Please refer to the block diagram in figure 1).

(03H: D4-D3)

DVOL1	DVOL0	Volume #0 Gain	Output Level
0	0	0dB	2Vrms (with 0dBFS input & volume #1=0dB.)
0	1	-6dB	1Vrms (with 0dBFS input & volume #1=0dB.)
1	0	+2.44dB	2.65Vrms (with 0dBFS input & volume #1=0dB.)
1	1	+4dB	2Vrms (with –10dBFS input & volume #1=+6dB. Clips over –2.5dBFS digital input.)

Table 6. Volume #0 (at DAPD bit =”0”. DAC mode)

(03H: D4-D3)

DVOL1	DVOL0	Volume #2 Gain	Output Level
0	0	+6dB	2Vrms (with 1Vrms input & volume #1=0dB.)
0	1	0dB	1Vrms (with 1Vrms input & volume #1=0dB.)
1	0	(reserved)	-
1	1	(reserved)	-

Table 7. Volume #2 (at DAPD bit =”1”. analog input mode.)

(02H: D5-D0)

L5	L4	L3	L2	L1	L0	Gain
1	0	0	0	1	0	+6dB
1	0	0	0	0	1	+4dB
1	0	0	0	0	0	+2dB
0	1	1	1	1	1	0dB (default)
…	…	…	…	…	…	…
0	0	0	0	0	1	-60dB
0	0	0	0	0	0	Mute

Note: Do not exceed 3Vrms at analog output.

Table 8. Volume #1 (Analog Volume)

(01H: D1-D0)

TV1	TV0	Source of TVOUTL/R
0	0	DAC
0	1	VCRIN (default)
1	0	Mute
1	1	(Reserved)

Table 9. TVOUT Switch Configuration

(01H: D2-D0)

VOL	TV1	TV0	Source of MONOOUT	
0	0	0	DAC (L+R)/2	Bypass the volume #1
0	0	1	DAC (L+R)/2	
0	1	0	DAC (L+R)/2	
0	1	1	(Reserved)	
1	0	0	DAC (L+R)/2	Through the volume #1
1	0	1	VCRIN (L+R)/2	
1	1	0	Mute	
1	1	1	(Reserved)	

Table 10. MONOOUT Switch Configuration

(01H: D5-D4)

VCR1	VCR0	Source of VCROUTL/R
0	0	DAC
0	1	TVIN (default)
1	0	Mute
1	1	Output of volume #1

Table 11. VCROUT Switch Configuration

■ Zero-cross Detection and Offset Calibration

To minimize the click noise at changing the gain of volume #1, the AK4704 has a zero-cross detection and an offset calibration function. When DAPD bit =”1”, the zero-cross detection and offset calibration does not work.

1. Zero-cross detection function (03H: D2-D0)

When the ZERO bit = “1”, the zero-cross detection function is enabled. The gain of volume #1 changes at the first zero-cross point from the acknowledgement of a volume changing command or when the zero-cross is not detected within the time set by ZTM1-0 bits (256/fs to 2048/fs). The zero-cross counter is initialized whenever a gain is issued. The zero-cross is detected on L/R channels independently. To disable this function, set the ZERO bit to “0”.

ZERO: Zero-cross detection enable for volume #1

0 : Disable. The volume value changes immediately without zero-cross.

1 : Enable (default). The volume value changes at a zero-crossing point or when timeout (ZTM1-0 bit setting) occurs.

The internal comparator for zero-cross detection has a small offset. Therefore, the gain of volume #1 may change due to a zero-cross timeout before the comparator-based zero-cross detection occurs.

When the new gain value 1EH(-2dB) is written while the gain of both Lch and Rch are 1FH(0dB), if the Lch detects the zero-cross prior to Rch, only the gain of Lch changes to 1EH(-2dB) while Rch waits for a zero-cross. After that, if the gain is set to 1DH(-4dB) before either a zero-cross or zero-cross timeout, the Rch keeps the same value and changes from 1FH to 1DH at next zero-cross or timeout.

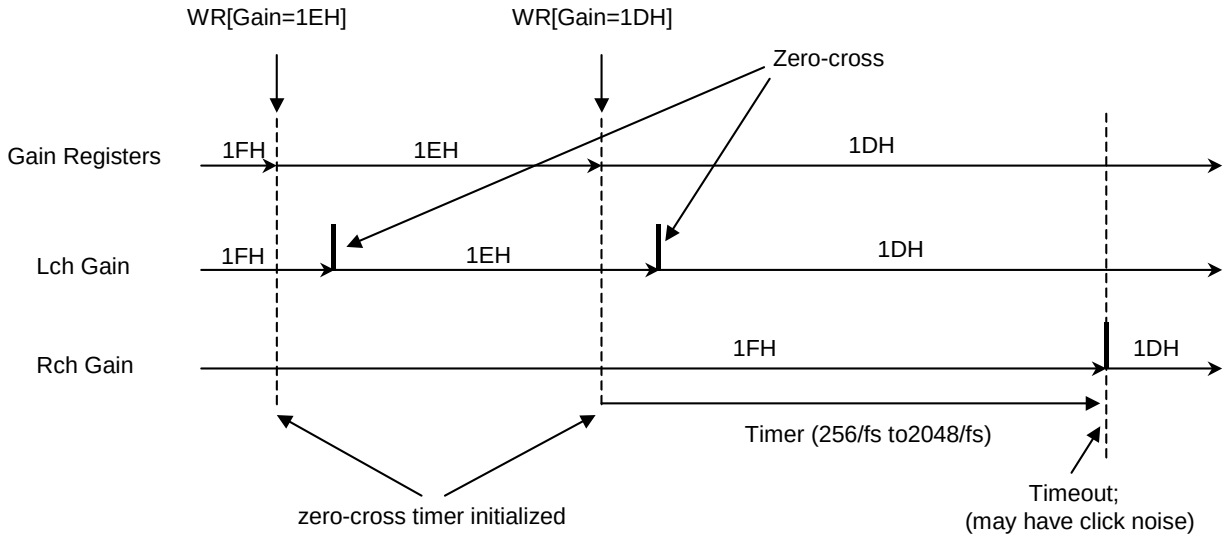


Figure 7. Zero-cross Operation (ZERO= “1”)

2. Offset calibration function (03H: D5)

Offset calibration is enabled when the CAL bit = “1”. This function begins when the TVOUT source is switched to DAC after the STBY bit is changed to “0”. It takes 1664/fs to execute the offset calibration cycle. During the offset calibration cycle, the analog outputs are muted. Once the offset calibration is executed, the calibration memory is held until PDN pin = “L” or the new calibration is executed. When the switch is changed from DAC to VCR during calibration, the calibration is discontinued, and resumed when TVOUT is switched back to DAC. If volume #1 gain is changed during calibration, the change takes place after calibration is complete.

3. Video Block

■ Video Switch Control

The AK4704 has switches for TV, VCR and RF modulator. Each switches can be controlled via registers independently. When AUTO bit = "1" or STBY bit = "1", these switch setting are ignored and set to fixed configuration (loop-through mode). Please refer the auto setup mode and standby mode.

(04H: D2-D0)

Mode	VTV2-0 bit	Source of TVVOUT pin	Source of TVRC pin	Source of TVG pin	Source of TVB pin
Shutdown	000	(Hi-Z)	(Hi-Z)	(Hi-Z)	(Hi-Z)
Encoder CVBS /RGB	001	ENCV pin	ENCRC pin	ENCG pin	ENCB pin
Encoder Y/C 1	010	ENCV pin	ENCRC pin	Hi-Z	(Hi-Z)
Encoder Y/C 2	011	ENCY pin	ENCC pin	Hi-Z	(Hi-Z)
VCR (default)	100	VCRVIN pin	VCRRC pin	VCRG pin	VCRB pin
TV CVBS	101	TVVIN pin	(Hi-Z)	(Hi-Z)	(Hi-Z)
(reserved)	110	-	-	-	-
(reserved)	111	-	-	-	-

(please refer notes)

Table 12. TV video output

(04H: D5-D3)

Mode	VVCR2-0 bit	Source of VCRVOUT pin	Source of VCRC pin
Shutdown	000	(Hi-Z)	(Hi-Z)
Encoder CVBS or Y/C 1	001	ENCV pin	ENCRC pin
Encoder CVBS or Y/C 2	010	ENCY pin	ENCC pin
TV CVBS (default)	011	TVVIN pin	(Hi-Z)
VCR	100	VCRVIN pin	VCRRC pin
(reserved)	101	-	-
(reserved)	110	-	-
(reserved)	111	-	-

(please refer notes)

Table 13. VCR video output

(04H: D7-D6)

Mode	VRF1-0 bit	Source of RFV pin
Encoder CVBS1	00	ENCV pin
Encoder CVBS2	01	ENCG pin (Note: 22)
VCR (default)	10	VCRVIN pin
Shutdown	11	(Hi-Z)

(when YC bit=0. please refer notes)

Table 14. RF video output

Note: 21: When input the video signal via ENCRC pin or VCRRC pin, set CLAMP1-0 bits respectively.
Note: 22 When VTV2-0 bit ="001", TVG bit ="1" and VRF1-0 bit ="01", RFV pin output is same as TVG pin output (Encoder G).

■ Video Output Control (05H: D6-D0)

Each video outputs can be set to Hi-Z individually via control registers. These setting are ignored when the AUTO bit = "1". When the CIO bit = "1", the VCRC pin outputs 0V even if the VCRC bit = "0". When the CIO bit = "0", the VCRC pin follows the setting of VCRC bit. Please refer the "Red/Chroma Bi-directional Control for VCR SCART"

TVV: TVVOUT output control
TVR: TVRCOUT output control
TVG: TVGOUT output control
TVB: TVBOUT output control
VCRV: VCRVOUT output control
VCRC: VCRC output control
TVFB: TVFB output control

0: Hi-Z (default)
1: Active.

■ Red/Chroma Bi-directional Control for VCR SCART (05H: D7, D5)

The 4704 supports the bi-directional Red/Chroma signal on the VCR SCART.

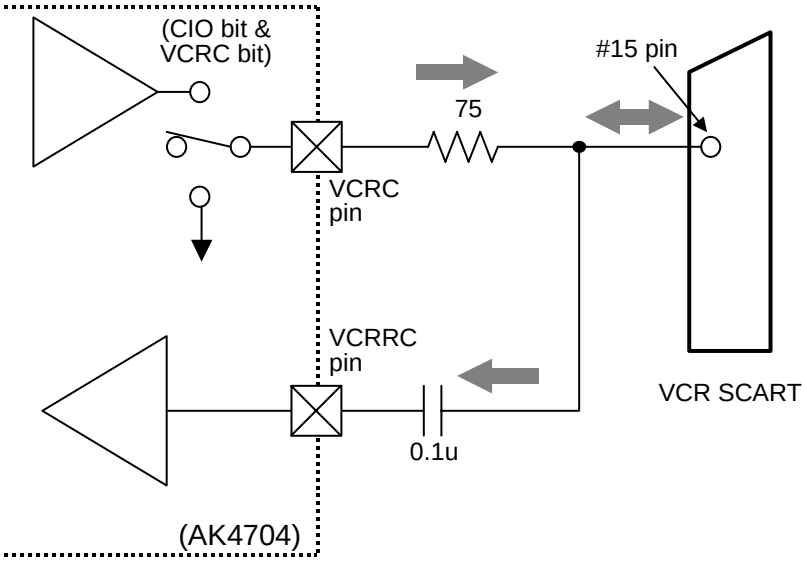


Figure 8. Red/Chroma Bi-directional Control

CIO	VCRC	State of VCRC pin
0	0	Hi-z (default)
0	1	Active
1	0	Connected to GND
1	1	Connected to GND

Table 15 Red/Chroma Bi-directional Control

■ RGB Video Gain Control (06H: D1-D0)

VVOL1-0 bits set the RGB video gain.

VVOL1	VVOL0	Gain	Output level (Typ. @Input=0.7Vpp)
0	0	+6dB	1.4Vpp (default)
0	1	+7.2dB	1.6Vpp
1	0	+8.2dB	1.8Vpp
1	1	+9.1dB	2.0Vpp

Table 16. RGB video gain control

■ Clamp and DC-restore circuit control (06H: D6-D5, D3-D2)

Each CVBS and Y input has the sync tip clamp circuit. The sync tip voltage at each output is 0.7V(typ). This corresponds 0.35V(typ) at the SCART connector when matched by 75ohm resisters. The CLAMP1 and CLAMP0 bits select the input circuit for ENCRC pin (Encoder Red/Chroma) and VCRRC pin (VCR Red/Chroma) respectively. VCLP1-0 bits select the source of DC- restore circuit.

CLAMP1 : Encoder Red/Chroma (ENCRC pin)input clamp control
- 0 : DC restore clamp active (for RED signal. default)
- 1 : Biased (for Chroma signal.)

CLAMP0 : VCR R/C (VCRRC pin)input clamp control
- 0 : DC restore clamp active (for RED signal)
- 1 : Biased (for Chroma signal. default.)

VCLP1-0 : DC restore source control

VCLP1	VCLP0	Sync Source of DC Restore
0	0	ENCV (default)
0	1	ENCY
1	0	VCRVIN
1	1	(Reserved)

When the AUTO bit = “1”, the source is fixed to VCRVIN.

Table 17. DC restore source control

■ Y/C Mixer for RF modulator (06H: D4)

When the YC bit = “1”, the RFV pin outputs Y/C mixed signal from TVVOUT pin and TVRC pin.

YC : Y/C mixing output control for RFV pin
- 0 : Follow VRF1-0 bits (default)
- 1 : Y/C mixing from TVVOUT and TVRC.

4. Blanking Control

The AK4704 supports Fast Blanking signals and Slow Blanking (Function Switching) signals for TV/VCR SCART.

■ Input/Output Control for Fast/Slow Blanking

FB1-0: TV Fast Blanking output control (07H: D1-D0)

FB1	FB0	TVFB pin Output Level
0	0	0V (default)
0	1	4V
1	0	Same as VCR FB input (4V/0V)
1	1	(Reserved)

(note: minimum load is 150ohm)

Table 18. TV Fast Blanking output

SBT1-0: TV Slow Blanking output control (07H: D3-D2)

SBT1	SBT0	TVSB pin Output Level
0	0	<2V (default)
0	1	5V<, <7V
1	0	(Reserved)
1	1	10V<

(note: minimum load is 10kohm)

Table 19. TV Slow Blanking output

SBV1-0: VCR Slow Blanking output control (07H: D5-D4)

SBV1	SBV0	VCRSB pin Output Level
0	0	<2V (default)
0	1	5V<, <7V
1	0	(Reserved)
1	1	10V<

(note: minimum load is 10kohm)

Table 20. VCR Slow Blanking output

SBIO1-0: TV/VCR Slow Blanking I/O control (07H: D7-D6)

SBIO1	SBIO0	VCRSB pin Direction	TVSB pin Direction	
0	0	Output (Controlled by SBV1,0)	Output (Controlled by SBT1,0)	(default)
0	1	(Reserved)	(Reserved)	
1	0	Input (Stored in SVCR1,0)	Output (Controlled by SBT1,0)	
1	1	Input (Stored in SVCR1,0)	Output (Same output as VCR SB)	

Table 21. TV/VCR Slow Blanking I/O control

5. Monitor Options and INT function

■ Monitor Options (08H: D3-D0)

The AK4704 has several monitors for the input DC level of VCR slow blanking, the input DC level of VCR fast blanking and signals input to TVVIN or VCRVIN pins. SVCR1-0 bits, FVCR bit and VMON bit are reflected to these values.

SVCR1-0: VCR Slow blanking status monitor
SVCR1-0 reflect the voltage at VCRSB pin only when the VCRSB is in the input mode.
When the VCRSB is in the output mode, SVCR1-0 hold previous value.

VCRSB pin input level	SVCR1	SVCR0
< 2V	0	0
4.5 to 7V	0	1
(Reserved)	1	0
9.5<	1	1

Table 22. VCR Slow Blanking monitor

FVCR: VCR Fast blanking input level monitor
This bit is enabled when TVFB bit = "1".

VCRFB pin input level	FVCR
<0.4V	0
1 V<	1

Table 23. VCR Fast Blanking monitor (Typical threshold is 0.7V)

VMON : Video input monitor
0 : No video signal detected via TVVIN pin and VCRVIN pin.
1 : Detects video signal via TVVIN pin OR VCRVIN pin.

■ INT Function and Mask Options (09H: D3-D1)

Changes of the 08H status can be monitored via the INT pin. The INT pin is the open drain output and goes "L" for 2usec(typ.) when the status of 08H is changed. This pin should be connected to VD (typ. 5V) through 10kohm resister. MVMON bit, MFVCR bit and MSVCR bit control the reflection of the status change of these monitors onto the INT pin from report to prevent to masks each monitor

MVMON: Video input monitor mask.

AUTO	MVMON	Reflection of the change of VMON bit to INT pin	
0	0	Reflect	
0	1	NOT reflect (e.g. masked)	
1	0	Reflect	
1	1	Reflect	(default)

Table 24. Reflection of VMON change

MFVCR: FVCR Monitor mask.
0 : Change of MFVCR is reflected to INT pin. (default)
1 : Change of MFVCR is NOT reflected to INT pin.

MSVCR: SVCR1-0 Monitor mask.
0 : Change of SVCR1-0 is reflected to INT pin. (default)
1 : Change of SVCR1-0 is NOT reflected to INT pin.

6. Control Interface

I²C-bus Control Mode

1. WRITE Operations

Figure 9 shows the data transfer sequence in I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 15). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010001". If the slave address match that of the AK4704, the AK4704 generates the acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 16). A "1" for R/W bit indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed. The second byte consists of the address for control registers of the AK4704. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 11). The data after the second byte contain control data. The format is MSB first, 8bits (Figure 12). The AK4704 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 15).

The AK4704 can execute multiple one byte write operations in a sequence. After receipt of the third byte, the AK4704 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 09H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 17) except for the START and the STOP condition.

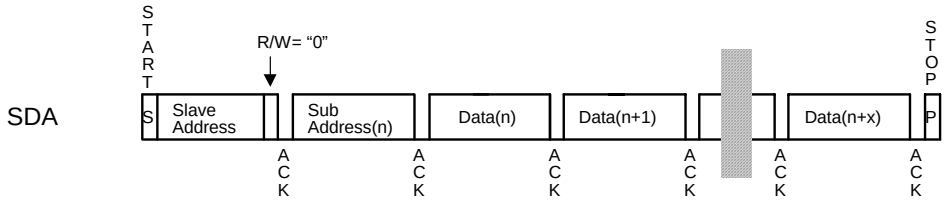


Figure 9. Data transfer sequence at the I²C-bus mode

0	0	1	0	0	0	1	R/W

Figure 10. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 11. The second byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 12. Byte structure after the second byte

2. READ Operations

Set R/W bit = "1" for READ operations. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 09H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4704 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

2-1. CURRENT ADDRESS READ

The AK4704 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4704 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4704 discontinues transmission

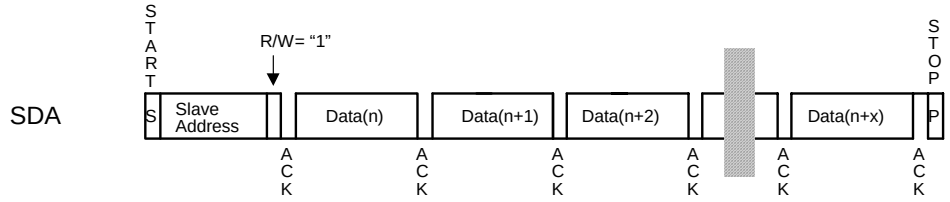


Figure 13. CURRENT ADDRESS READ

2-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address(R/W="0") and then the register address to read. After the register's address is acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4704 generates an acknowledge, 1-byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4704 discontinues transmission.

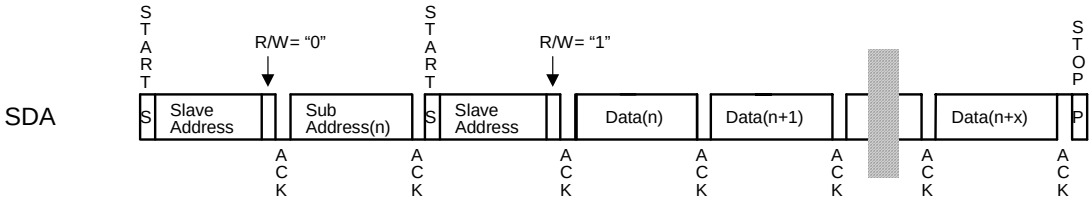


Figure 14. RANDOM ADDRESS READ

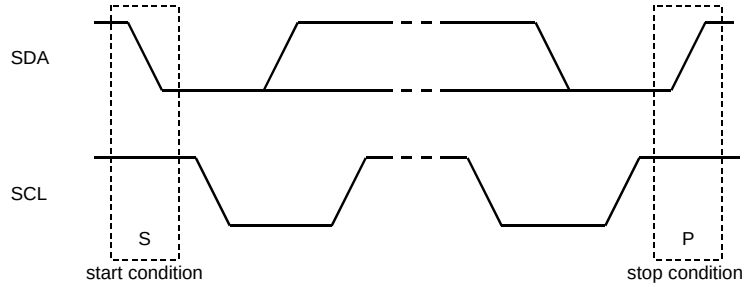


Figure 15. START and STOP conditions

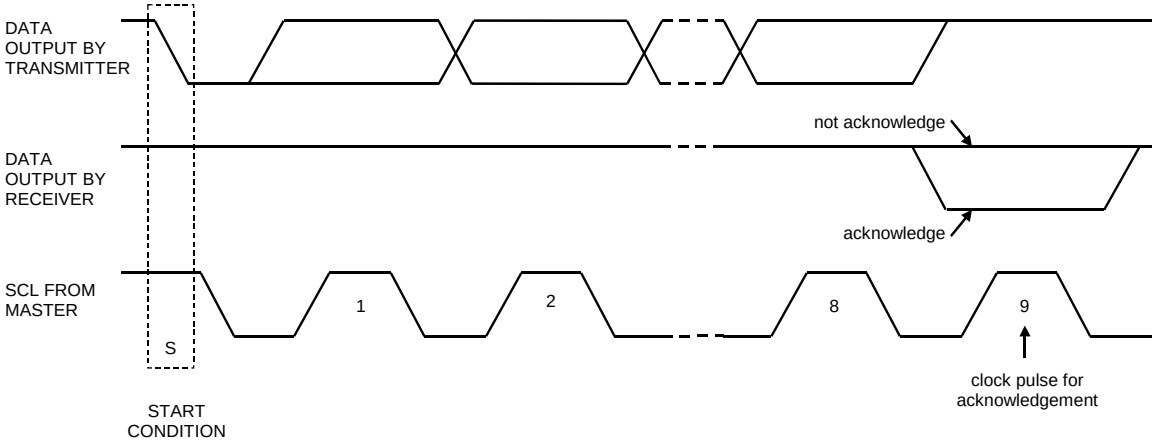


Figure 16. Acknowledge on the I^2C-bus

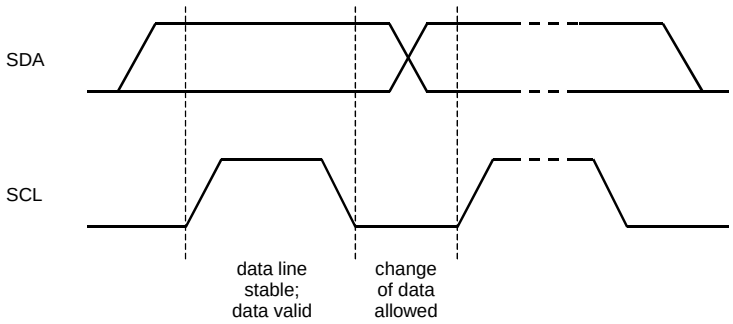


Figure 17. Bit transfer on the I^2C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	DEM1	DEM0	DIF1	DIF0	AUTO	DAPD	MUTE	STBY
01H	Switch	VMUTE	0	VCR1	VCR0	MONO	VOL	TV1	TV0
02H	Main volume	0	0	L5	L4	L3	L2	L1	L0
03H	Zerocross	0	VMONO	CAL	DVOL1	DVOL0	ZERO	ZTM1	ZTM0
04H	Video switch	VRF1	VRF0	VVCR2	VVCR1	VVCR0	VTV2	VTV1	VTV0
05H	Video output enable	CIO	TVFB	VCRC	VCRV	TVB	TVG	TVR	TVV
06H	Video volume/clamp	0	VCLP1	VCLP0	YC	CLAMP1	CLAMP0	VVOL1	VVOL0
07H	S/F Blanking control	SBIO1	SBIO0	SBV1	SBV0	SBT1	SBT0	FB1	FB0
08H	S/F Blanking monitor	0	0	0	0	VMON	FVCR	SVCR1	SVCR0
09H	Monitor mask	0	0	0	0	MVMON	MFVCR	MSVCR	0

When the PDN pin goes “L”, the registers are initialized to their default values.

While the PDN pin =“H”, all registers can be accessed.

Do not write any data to the register over 09H.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	DEM1	DEM0	DIF1	DIF0	AUTO	DAPD	MUTE	STBY
R/W		R/W							
default		0	1	1	1	1	0	1	1

STBY: Standby control

0 : Normal Operation

1 : Standby Mode(default). All registers are not initialized.

DAC	:	powered down and timings are reset.
Gain of Volume#1	:	fixed to 0dB,
Source of TVOUT	:	fixed to VCRIN,
Source of VCROUT	:	fixed to TVIN,
Source of MONOOUT	:	fixed to VCRIN,
Source of TVVOUT	:	fixed to VCRVIN(or Hi-Z),
Source of TVRC	:	fixed to VCRRC(or Hi-Z),
Source of TVG	:	fixed to VCRG(or Hi-Z),
Source of TVB	:	fixed to VCRB(or Hi-Z),
Source of VCRVOUT	:	fixed to TVVIN(or Hi-Z),
Source of VCRC	:	fixed to Hi-Z or VSS(controlled by CIO bit).

MUTE: Audio output control

0 : Normal operation

1 : ALL Audio outputs to GND (default)

DAPD: DAC power down control

0 : Normal operation (default).

1 : DAC power down.
When DAPD bit = “1”, the zero-cross detection and offset calibration does not work.

AUTO: Auto startup bit

0 : Auto startup disable (Manual startup).

1 : Auto startup enable(default).

Note: When the SBIO1bit = “1”(default= “0”), the change of AUTO bit may cause a “L” pulse on INT pin.

DIF1-0: Audio data interface format control

00 : 16bit LSB Justified

01 : 18bit LSB Justified

10 : 24bit MSB Justified

11 : 24bit I^2S Compatible (Default)

DEM1-0: De-emphasis Response Control

00 : 44.1kHz

01 : off (Default)

10 : 48kHz

11 : 32kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Switch	VMUTE	0	VCR1	VCR0	MONO	VOL	TV1	TV0
R/W		R/W							
default		1	0	0	1	0	1	0	1

TV1-0: TVOUTL/R pins source switch
- 00 : DAC
- 01 : VCRINL/R pins (Default)
- 10 : MUTE
- 11 : (Reserved)

VOL: MONOOUT pin source switch
- 0 : Bypass the volume (fixed to DAC out)
- 1 : Through the volume (Default)

MONO: Mono select for TVOUTL/R pins
- 0 : Stereo. (Default)
- 1 : Mono. (L+R)/2

VCR1-0: VCROUTL/R pins source switch
- 00 : DAC
- 01 : TVINL/R pins (Default)
- 10 : MUTE
- 11 : Volume #1 output

VMUTE: Mute switch for volume #1
- 0 : Normal operation
- 1 : Mute the volume #1 (Default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Main volume	0	0	L5	L4	L3	L2	L1	L0
R/W		R/W							
default		0	0	0	1	1	1	1	1

L5-0: Volume #1 control

Those registers control both Lch and Rch of Volume #1.

111111 to
- 100011 : (Reserved)
- 100010 : Volume gain = +6dB
- 100001 : Volume gain = +4dB
- 100000 : Volume gain = +2dB
- 011111 : Volume gain = +0dB (default)
- 011110 : Volume gain = -2dB
- ...
- 000011 : Volume gain = -56dB
- 000010 : Volume gain = -58dB
- 000001 : Volume gain = -60dB
- 000000 : Volume gain = Mute

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Zerocross	0	VMONO	CAL	DVOL1	DVOL0	ZERO	ZTM1	ZTM0
R/W		R/W							
default		0	0	1	0	0	1	1	1

ZTM1-0: The time length control of zero-cross timeout

00 : typ. 256/fs
01 : 512/fs
10 : 1024/fs
11 : 2048/fs (default)

ZERO: Zero-cross detection enable for volume #1 control

0 : Disable
The volume value changes immediately without zero-cross.
1 : Enable (default)
The volume value changes when timeout or zero-cross before timeout.
This function is disabled when STBY bit = "1".

DVOL1-0: Volume #0/Volume #2 control.
Please refer the Table 6 and Table 7

CAL: Offset calibration Enable

0 : Offset calibration disable.
1 : Offset calibration enable(default)

VMONO: Mono select for VCROUTL/R pins

0 : Stereo. (Default)
1 : Mono. (L+R)/2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Video switch	VRF1	VRF0	VVCR2	VVCR1	VVCR0	VTV2	VTV1	VTV0
R/W		R/W							
default		1	0	0	1	1	1	0	0

VTV0-2: Selector for TV video output
Please refer the Table 12.

VVCR0-2: Selector for VCR video output
Please refer the Table 13

RF0-1: Selector for RFV pin output (when YC bit=0).
Please refer the Table 14.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	output enable	CIO	TVFB	VCRC	VCRV	TVB	TVG	TVR	TVV
R/W		R/W							
default		0	0	0	0	0	0	0	0

TVV: TVVOUT output control
TVR: TVRCOUT output control
TVG: TVGOUT output control
TVB: TVBOUT output control
VCRV: VCRVOUT output control
VCRC: VCRC output control (please refer the Table 15)
TVFB: TVFB output control
0 : Hi-Z (default)
1 : Active.

When the CIO pin = “1”, the VCRC pin is connected to GND even if VCRC= “0”.
When the CIO pin = “0”, the VCRC pin follows the setting of VCRC bit.

CIO: VCRC pin I/O control
Please refer the Table 15.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Video volume	0	VCLP1	VCLP0	YC	CLAMP1	CLAMP0	VVOL1	VVOL0
R/W		R/W							
default		0	0	0	0	0	1	0	0

VVOL1-0: RGB video gain control
- 00: +6dB (default)
- 01: +7.2dB
- 10: +8.2dB
- 11: +9.1dB

CLAMP1 : Encoder R/Chroma (ENCRC pin) input clamp control
- 0 : DC restore clamp active (for RED signal. default)
- 1 : Biased (for Chroma signal.)

CLAMP0 : VCR R/C (VCRC pin) input clamp control
- 0 : DC restore clamp active (for RED signal)
- 1 : Biased (for Chroma signal. default.)

YC : Y/C mixing output control for RFV pin
- 0 : Follow VRF1-0 bits (default)
- 1 : Y/C mixing from TVVOUT and TVRC.

VCLP1-0 : DC restore source control
- 00: ENCV pin (default)
- 01: ENCY pin
- 10: VCRVIN pin
- 11: (Reserved)

When the AUTO bit = "1", the source is fixed to VCRVIN pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	S/F Blanking	SBIO1	SBIO0	SBV1	SBV0	SBT1	SBT0	FB1	FB0
R/W		R/W							
default		0	0	0	0	0	0	0	0

FB1-0: TV Fast Blanking output control (for TVFB pin)
- 00: 0V (default)
- 01: 4V
- 10: follow VCR FB input (4V/0V)
- 11: (Reserved)

SBT1-0: TV Slow Blanking output control (for TVSB pin. minimum load is 10kohm.)
- 00: <2V (default)
- 01: 5V<, <7V
- 10: (Reserved)
- 11: 10V<

SBV1-0: VCR Slow Blanking output control (for VCRSB pin. minimum load is 10kohm)
- 00: <2V (default)
- 01: 5V<, <7V
- 10: (Reserved)
- 11: 10V<

SBIO1-0: TV/VCR Slow Blanking I/O control (please refer the Table 21)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	SB/FB monitor	0	0	0	0	VMON	FVCR	SVCR1	SVCR0
R/W		READ							
default		0	0	0	0	0	0	0	0

SVCR1-0: VCR Slow blanking status monitor

SVCR1-0 reflect the voltage at VCRSB pin only when the VCRSB is in the input mode.
When the VCRSB is in the output mode, SVCR1-0 hold previous value.

VCRSB pin input level	SVCR1	SVCR0
< 2V	0	0
4.5 to 7V	0	1
(Reserved)	1	0
9.5<	1	1

Table 25. VCR Slow Blanking monitor

FVCR: VCR Fast blanking input level monitor

This bit is enabled when TVFB bit = "1".

VCRFB pin input level	FVCR
<0.4V	0
1 V<	1

Table 26. VCR Fast Blanking monitor (Typical threshold is 0.7V)

VMON : Video input monitor

0 : No video signal detected via TVVIN pin and VCRVIN pin.
1 : Detects video signal via TVVIN pin OR VCRVIN pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Monitor mask	0	0	0	0	MVMON	MFVCR	MSVCR	0
R/W		R/W							
default		0	0	0	0	1	0	0	0

MVMON: Video input monitor mask.

Please refer the Table 24.

MFVCR: FVCR Monitor mask.

0 : The INT pin reflects the change of MFVCR bit. (default)
1 : The INT pin does not reflect the change of MFVCR bit.

MSVCR: SVCR1-0 Monitor mask.

0 : The INT pin reflects the change of SVCR1-0 bit. (default)
1 : The INT pin does not reflect the change of SVCR1-0 bit.

SYSTEM DESIGN

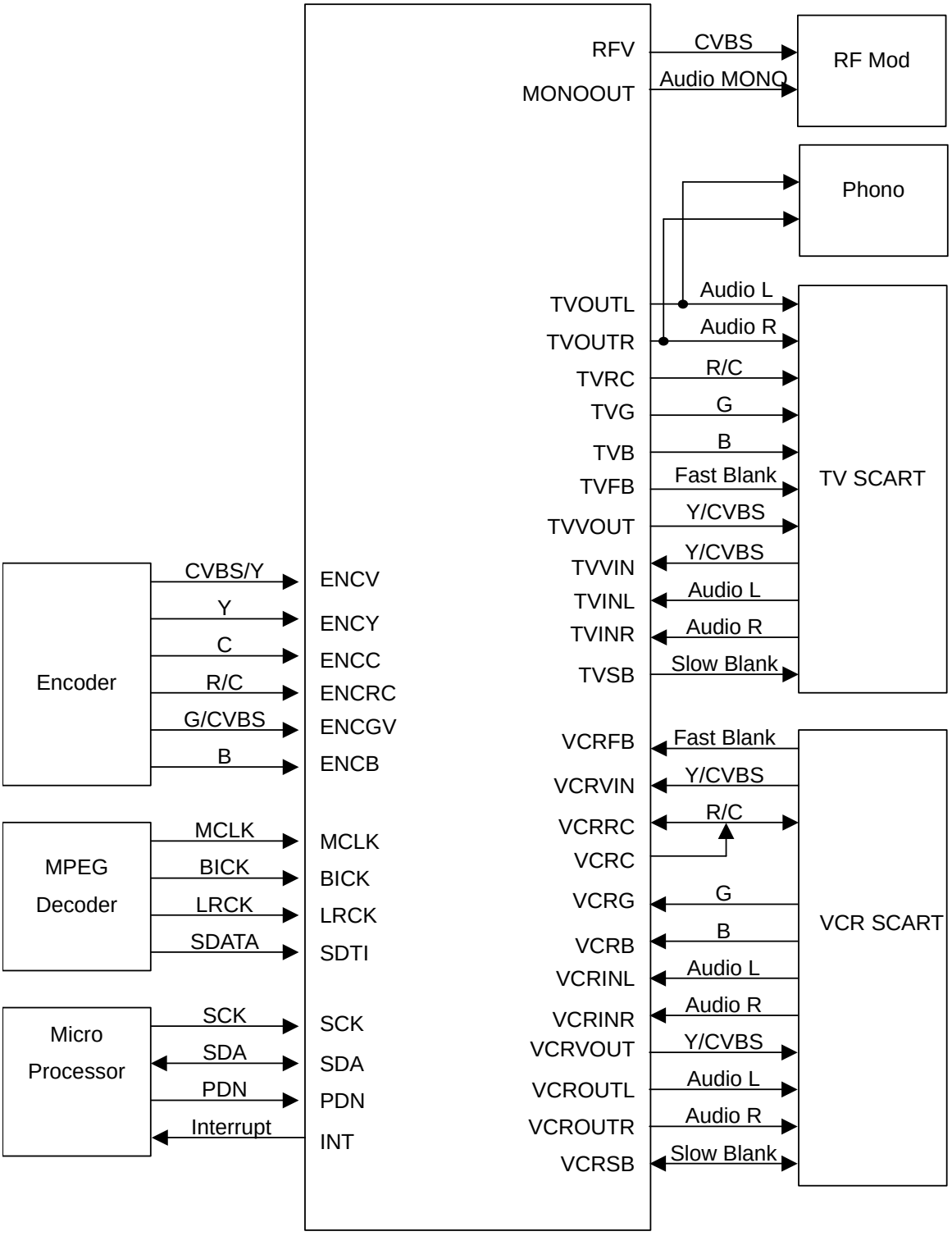


Figure 18. Typical Connection Diagram

■ Grounding and Power Supply Decoupling

VD, VP, VVD1, VVD2, VSS and VVSS should be supplied from analog supply unit with low impedance and be separated from system digital supply. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor should be attached to these pins to eliminate the effects of high frequency noise. The 0.1μF ceramic capacitor should be placed as near to VD (VP, VVD1, VVD2) as possible.

■ Voltage Reference

Each DVCOM/PVCOM are signal ground of this chip. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor should be attached to these VCOM pins to eliminate the effects of high frequency noise. No load current may be drawn from these VCOM pins. All signals, especially clocks, should be kept away from these VCOM pins in order to avoid unwanted coupling into the AK4704.

■ Analog Audio Outputs

The analog outputs are also single-ended and centered on 5.6V(typ.). The output signal range is typically 2Vrms (typ@VD=5V). The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio pass band. Therefore, any external filters are not required for typical application. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is 5.6V(typ.) for 000000H (@24bit). The DC voltage on analog outputs are eliminated by AC coupling.

■ FILT pin

The C (0.1 μF) should be attached as shown in the Figure 19.

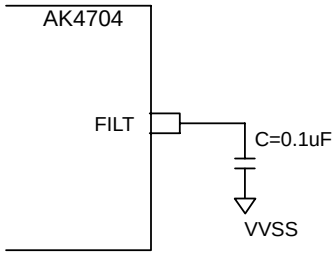
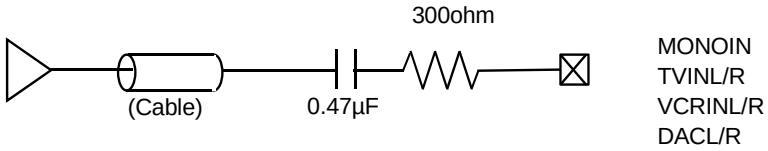


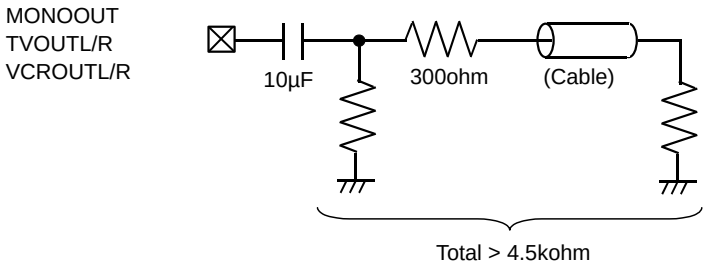
Figure 19. FILT pin

■ External Circuit Example

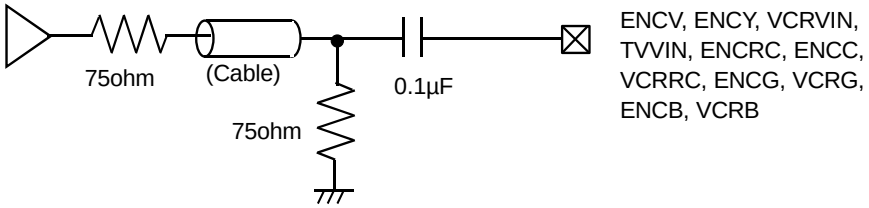
Analog Audio Input pin



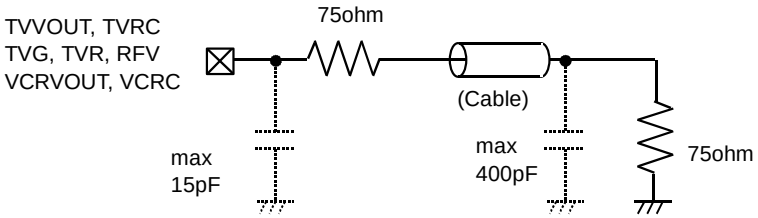
Analog Audio Output pin



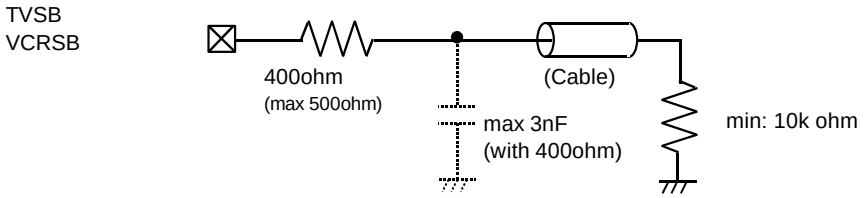
Analog Video Input pin



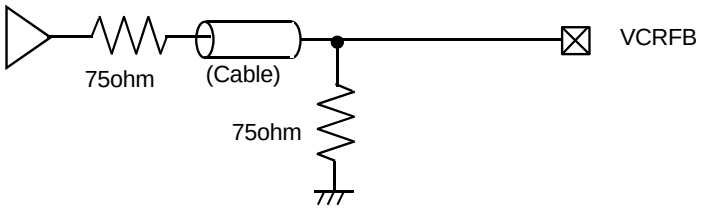
Analog Video Output pin



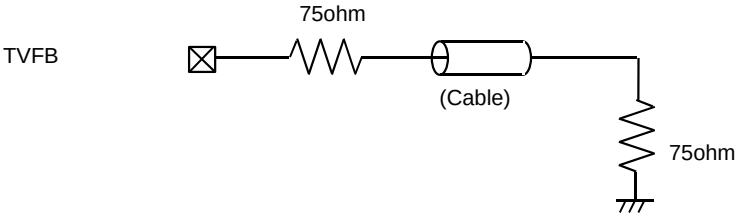
Slow Blanking pin



Fast Blanking Input pin

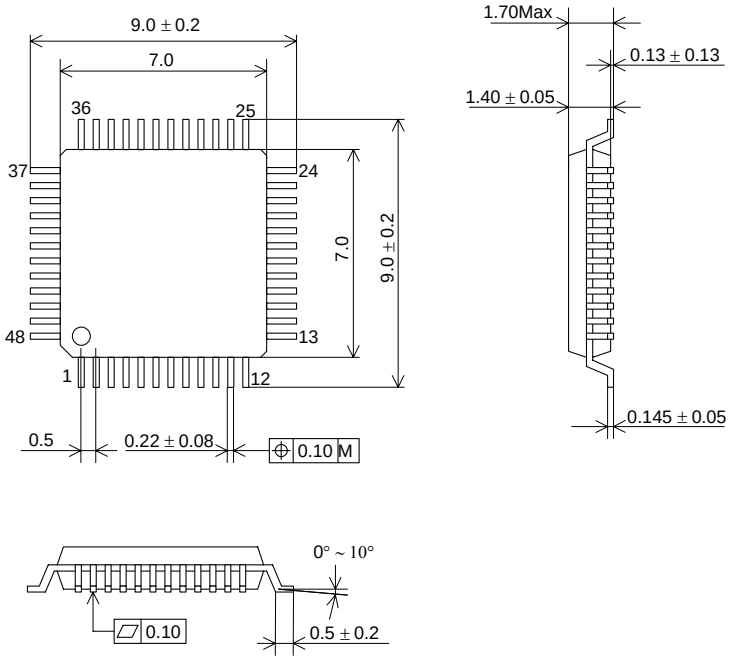


Fast Blanking Output pin



PACKAGE

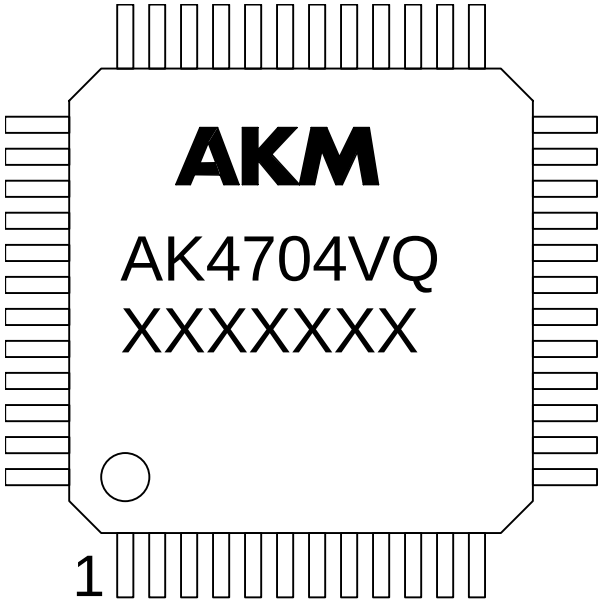
48pin LQFP(Unit:mm)



■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXXXXXX: Date code identifier

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