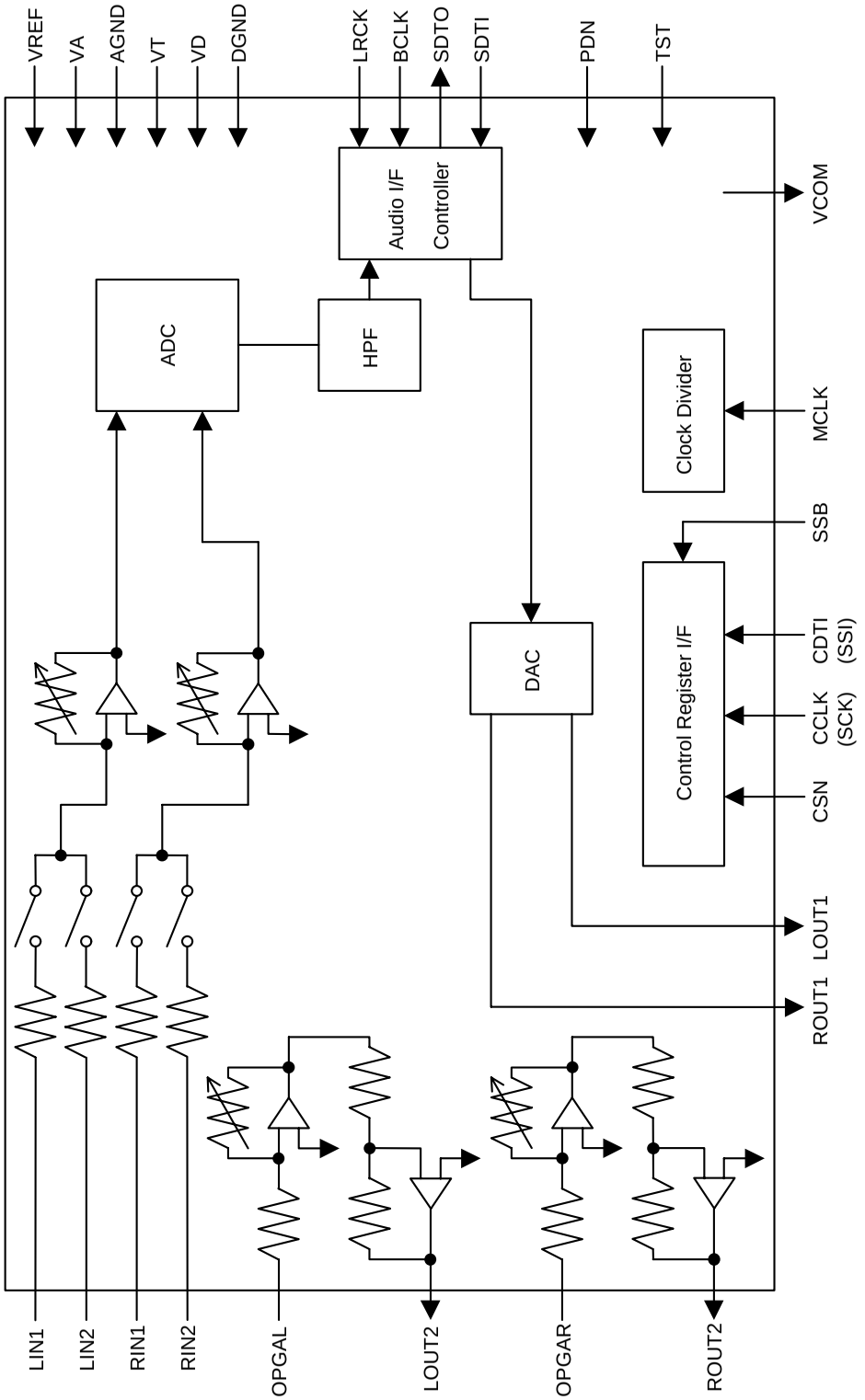
AK4562
Low Power 20bit ΔΣ CODEC with PGA

FEATURES

1. Resolution : 20bits
2. Recording Functions
   - 2-Stereo Inputs Mixer
   - Analog Input PGA
   - Monaural Mixing
   - Digital HPF for DC-offset cancellation (fc=3.4Hz@fs=44.1kHz)
3. Playback Functions
   - Digital De-emphasis Filter (tc=50/15us, fs=32kHz, 44.1kHz and 48kHz)
   - Analog Output PGA
   - 2 types Stereo Outputs (DAC and Analog Output PGA)
4. Power Management
5. ADC Characteristics
   - Input Level : 1.5Vpp = 0.6 x VREF@VREF=2.5V
   - S/(N+D) : 82dB
   - DR, S/N : 88dB
6. DAC Characteristics
   - Output Level : 1.5Vpp = 0.6 x VREF@VREF=2.5V
   - S/(N+D) : 86dB
   - DR, S/N : 93dB
7. 3-wire Serial Control, SSB I/F
8. Master Clock : 256fs/384fs
9. Audio Data Format : MSB First, 2's compliment
   - ADC : 20bit MSB justified, I^2S
   - DAC : 16bit LSB justified, 20bit LSB justified, 24bit LSB justified, I^2S
10. Power Supply
    - CODEC, PGA : 2.2 ~ 3.0V (typ. 2.5V)
    - Digital I/F : 1.8 ~ 3.0V (typ. 2.5V)
11. Power Supply Current
    - IPGA + ADC : 7mA
    - DAC + OPGA : 5.5mA
12. Ta = -20 ~ 70°C
13. Package : 28pin QFN
    - Size : 5.2mm x 5.2mm
    - Height : 1mm (max)
    - Pitch : 0.5mm

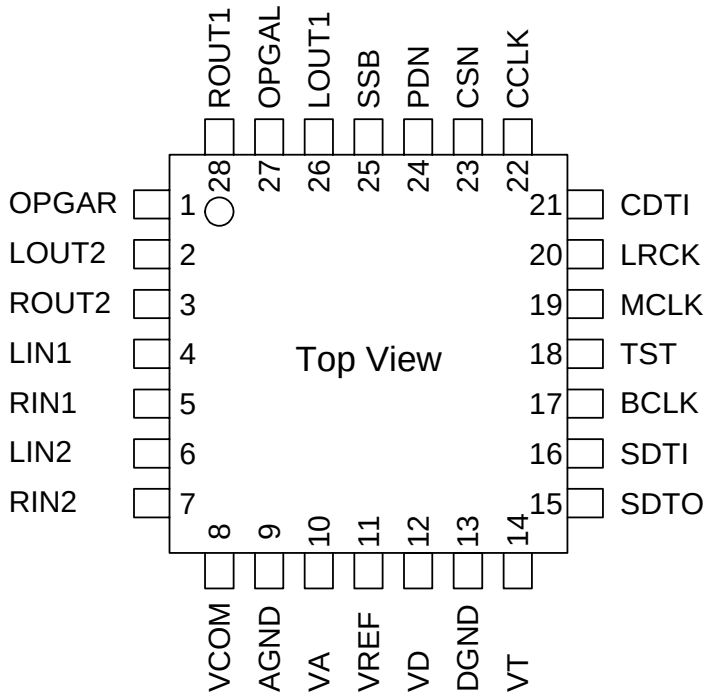
■ Block Diagram



■ Ordering Guide

AK4562VN	-20 ~ +70°C	28pin QFN (0.5mm pitch)
AKD4562	Evaluation Board for AK4562	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	OPGAR	I	Rch OPGA Input Pin
2	LOUT2	O	Lch OPGA Output Pin
3	ROUT2	O	Rch OPGA Output Pin
4	LIN1	I	Lch #1 Input Pin
5	RIN1	I	Rch #1 Input Pin
6	LIN2	I	Lch #2 Input Pin
7	RIN2	I	Rch #2 Input Pin
8	VCOM	-	Analog Common Voltage Output Pin, 0.45 x VA
9	AGND	-	Analog Ground Pin
10	VA	-	Analog Power Supply Pin, +2.5V
11	VREF	-	Analog Voltage Reference Input Pin. Used as a voltage reference of ADC & DAC. VREF is connected externally to filtered VA.
12	VD	-	Digital Power Supply Pin, +2.5V
13	DGND	-	Digital Ground Pin
14	VT	-	Digital Interface Power Supply Pin
15	SDTO	O	Audio Serial Data Output Pin
16	SDTI	I	Audio Serial Data Input Pin
17	BCLK	I	Audio Serial Data Clock Pin
18	TST	I	Test Mode Pin, Fixed to “L”
19	MCLK	I	Master Clock Input Pin
20	LRCK	I	Input/Output Channel Clock Pin
21	CDTI	I	Control Data Input Pin, SSB Mode: SSI
22	CCLK	I	Control Clock Input Pin, SSB Mode: SCK
23	CSN	I	Chip Select Pin, SSB Mode: “H”
24	PDN	I	Reset & Power Down Pin, “L”: Power down & Reset, “H”: Normal Operation
25	SSB	I	Control I/F Mode Select Pin, “L”: AKM Mode, “H”: SSB Mode
26	LOUT1	O	Lch DAC Output Pin
27	OPGAL	I	Lch OPGA Input Pin
28	ROUT1	O	Rch DAC Output Pin

Note : All digital input pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supply	Analog	VA	-0.3	4.6	V
	Digital 1	VD	-0.3	4.6	V
	Digital 2	VT	-0.3	4.6	V
	VD – VA	VDA	-	0.3	V
	|DGND – AGND| (Note 2)	ΔGND	-	0.3	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
Analog Input Voltage LIN1-2, RIN1-2, OPGAL, OPGAR, VREF pins		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VT+0.3	V
Ambient Temperature (power applied)		Ta	-20	70	°C
Storage Temperature		Tstg	-65	150	°C

Note : 1. All voltages with respect to ground.
Note : 2. AGND and DGND must be same voltage.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supply	Analog (VA pin)	VA	2.2	2.5	3.0	V
	Digital 1 (VD pin) (Note 3)	VD	2.2 / VA-0.3	2.5	VA	V
	Digital 2 (VT pin)	VT	1.8	2.5	VD	V
Voltage Reference	Analog Voltage Reference (Note 4)	VREF	-	-	VA	V

Note : 1. All voltages with respect to ground.
Note : 3. Min value is high value either 2.2V or VA-0.3V.
Note : 4. VREF and VA must be same voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA, VD, VT=2.5V; fs=44.1kHz; Signal Frequency=1kHz; Measurement frequency=10Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				20	bits
Input PGA Characteristics (IPGA):					
Input Voltage (LIN1, LIN2, RIN1, RIN2) (Note 5)		1.35	1.5	1.65	Vpp
Input Impedance		6.3	9	15.0	kΩ
Step Width	+28dB ~ -8dB	0.1	0.5	1	dB
	-8dB ~ -16dB	0.1	1	2	dB
	-16dB ~ -32dB	0.1	2	4	dB
	-32dB ~ -40dB	-	2	-	dB
	-40dB ~ -52dB	-	4	-	dB
ADC Analog Input Characteristics: (Note 6)					
S/(N+D) (-0.5dBFS Input)		74	82		dB
D-Range (EIAJ)		82	88		dB
S/N (EIAJ)		82	88		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
DAC Analog Output Characteristics: Measured at LOUT1/ROUT1 (Note 7)					
S/(N+D)		78	86		dB
D-Range (EIAJ)		87	93		dB
S/N (EIAJ)		87	93		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Output Voltage		1.35	1.5	1.65	Vpp
Load Resistance		10			kΩ
Load Capacitance				20	pF
Output PGA Characteristics (OPGA):					
S/(N+D) (Note 8)		82	92		dB
S/N (EIAJ) (Note 8)		89	95		dB
Noise level at Mute (EIAJ) (Note 9)		-	108	-	dB
Input Voltage (Note 10)			1.5	1.65	Vpp
Output Voltage (Note 10)			1.5	1.65	Vpp
Input Impedance		30	50	80	kΩ
Load Resistance		10			kΩ
Load Capacitance				20	pF
Step Width	+0dB ~ -34dB	0.1	1	2	dB
	-34dB ~ -64dB	0.1	2	4	dB
	-64dB ~ -78dB	-	2	-	dB

Note : 5. Analog input voltage (full-scale voltage: IPGA = 0dB) scale with VREF. (IPGA = ADC = 0.6 x VREF.)
Note : 6. ADC is input from LIN1/RIN1 or LIN2/RIN2 and it measures included in IPGA. The value of IPGA is set 0dB. Internal HPF cancels the offset of IPGA and ADC.
Note : 7. Analog output voltage scale with VREF. (DAC = 0.6 x VREF.)
Note : 8. Input: OPGAL/OPGAR; Output: LOUT2/ROUT2; OPGA = 0dB.
Note : 9. Noise level when reference voltage is 1.5Vpp.
Note : 10. Analog input/output voltage scale with VREF. (OPGA = 0.6 x VREF.)

Power Supplies				
Power Supply Current: VA+VD+VT				
Normal Operation (PDN="H")				
AD+DA (PM0=1, PM1=1, PM2=1, PM3=1)		12.0	17.0	mA
AD (PM0=1, PM1=1, PM2=0, PM3=0)		7.0	-	mA
DA (PM0=0, PM1=0, PM2=1, PM3=1)		5.5	-	mA
Power Down (PDN="L") (Note 11)		10	100	uA

Note : 11. In case of power-down mode, all digital input pins including clocks pins (MCLK, BCLK and LRCK) are held VT or DGND. PDN pin is held DGND.

FILTER CHARACTERISTICS

(Ta=-20 ~ 70°C; VA, VD=2.2 ~ 3.0V, VT=1.8 ~ 3.0; fs=44.1kHz; De-emphasis = OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 12)	±0.1dB	PB	0		17.4	kHz
	-1.0dB			20.0		kHz
	-3.0dB			21.1		kHz
Stopband (Note 12)		SB	27.0			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 13)		GD		17.0		1/fs
Group Delay Distortion		ΔGD		0		us
ADC Digital Filter (HPF):						
Frequency Response (Note 12)	-3dB	FR		3.4		Hz
	-0.5dB			10		Hz
	-0.1dB			22		Hz
DAC Digital Filter:						
Passband (Note 12)	±0.1dB	PB	0		20.0	kHz
	-6.0dB			22.05		kHz
Stopband (Note 12)		SB	24.1			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 13)		GD		14.7		1/fs
Group Delay Distortion		ΔGD		0		us
DAC Digital Filter + Analog Filter						
Frequency Response 0 ~ 20.0kHz		FR		±0.5		dB

Note : 12. The passband and stopband frequencies scale with fs (sampling frequency).
For examples, PB=0.454 x fs(@ADC: -1.0dB), PB=0.454 x fs(@DAC: -0.1dB).

Note : 13. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 20bit data of both channels to the output register for ADC and include group delay of HPF. For DAC, this time is from setting the data of both channels on input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=-20 ~ 70°C; VA, VD=2.2 ~ 3.0V, VT=1.8 ~ 3.0V)

Parameter	Symbol	min	Typ	max	Units
High-Level Input Voltage	VIH	75%VT	-	-	V
Low-Level Input Voltage	VIL	-	-	25%VT	V
High-Level Output Voltage (Iout=-400uA)	VOH	VT-0.4	-	-	V
Low-Level Output Voltage (Iout=400uA)	VOL	-		0.4	V
Input Leakage Current	Iin	-	-	± 10	uA

SWITCHING CHARACTERISTICS

(Ta=-20 ~ 70°C; VA, VD=2.2 ~ 3.0V, VT=1.8 ~ 3.0V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Control Clock Frequency					
Master Clock (MCLK)					
256fs: Frequency	fCLK	2.048	11.2896	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs: Frequency	fCLK	3.072	16.9344	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
Channel Clock (LRCK) Frequency	fs	8	44.1	50	kHz
Duty Cycle		45		55	%
Audio Interface Timing					
BCLK Period	tBLK	312.5			ns
BCLK Pulse Width Low	tBLKL	130			ns
Pulse Width High	tBLKH	130			ns
BCLK "↓" to LRCK	tBLR	-tBLKH+50		tBLKL-50	ns
LRCK Edge to SDTO (MSB)	tDLR			80	ns
BCLK "↓" to SDTO	tDSS			80	ns
SDTI Hold Time	tSDH	50			ns
SDTI Setup Time	tSDS	50			ns
Control Interface Timing (AKM)					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDATA Setup Time	tCDS	50			ns
CDATA Hold Time	tCDH	50			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (SSB)					
SCK Period	tSCK	250			ns
SCLK Pulse Width Low	tSCKL	100			ns
Pulse Width High	tSCKH	100			ns
SSI Setup Time	tSIS	50			ns
SSI Hold Time	tSIH	50			ns
Reset / Calibration Timing					
PDN Pulse Width	tPW	150			ns
PDN "↑" to SDTO (Note 14)	tPWV		4128		1/fs

Note : 14. These cycles are the numbers of LRCK rising from PDN pin rising.

■ Timing Diagram

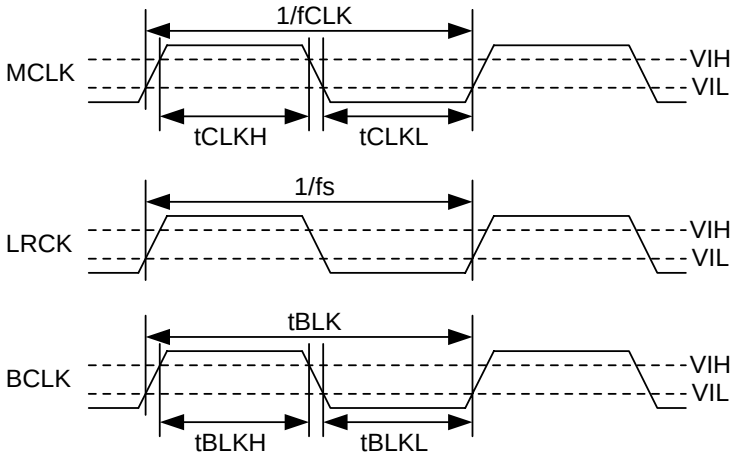


Figure 1. Clock Timing

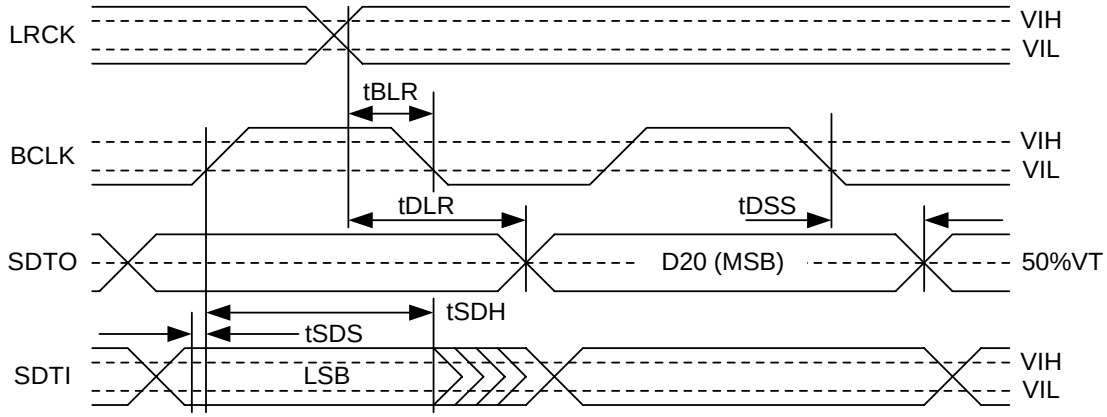


Figure 2. Audio Data Input/Output Timing (Audio I/F = No.0)

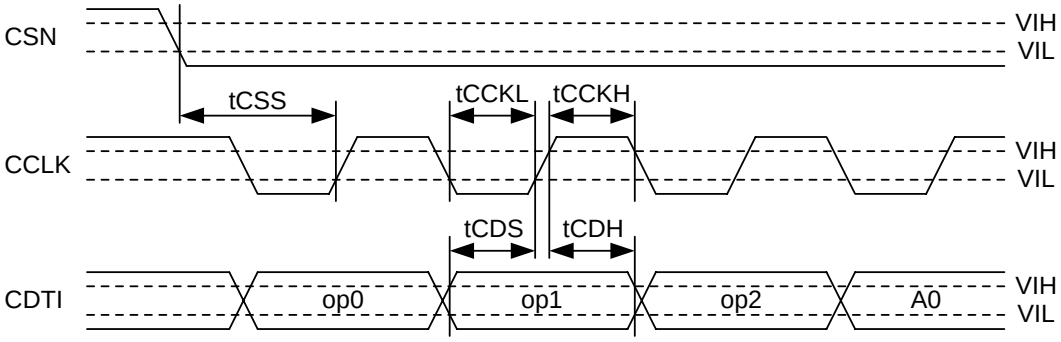


Figure 3. WRITE Command Input Timing (AKM)

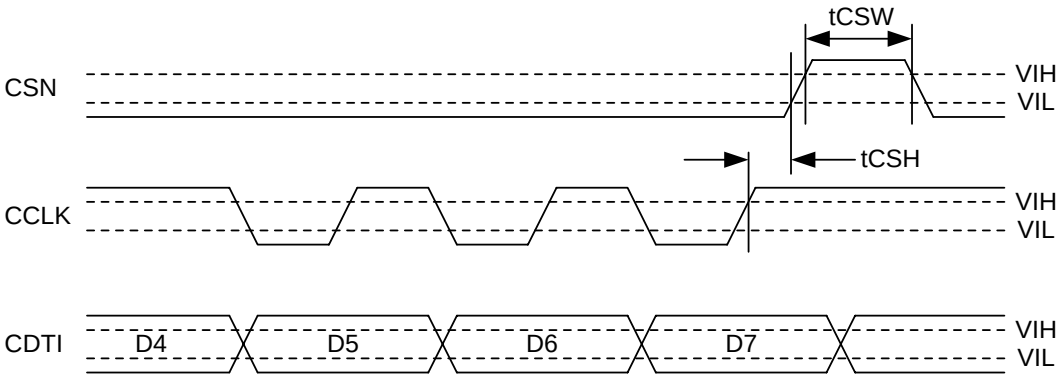


Figure 4. WRITE Data Input Timing (AKM)

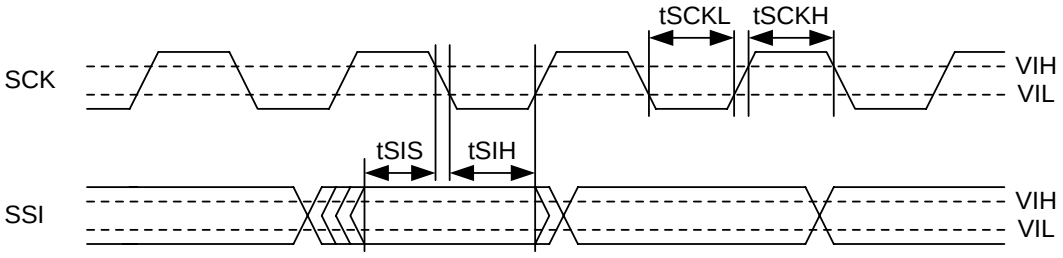


Figure 5. WRITE Data Input Timing (SSB)

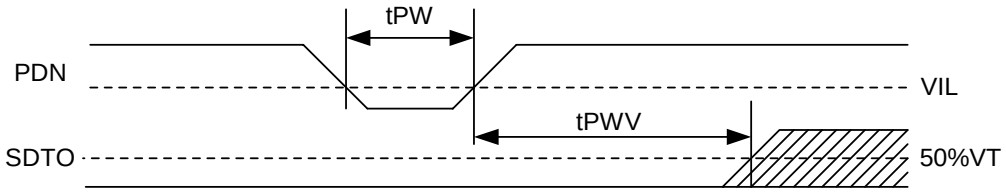


Figure 6. Reset Timing

OPERATION OVERVIEW

■ System Clock

The clocks that are required to operate are MCLK (256fs/384fs), LRCK (fs) and BCLK (32fs~). The master clock (MCLK) should be synchronized with LRCK but the phase is free of care. The frequency of MCLK can be input 256fs or 384fs. When the 384fs is input, the internal master clock is divided into 2/3 automatically.
*fs is sampling frequency.

All external clocks (MCLK, BCLK and LRCK) should always be present whenever ADC and DAC are in operation. If these clocks are not provided, the AK4562 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed internally. If the external clocks are not present, the AK4562 should be in the power-down mode.

■ Audio Data I/F Format

Using SDTO, SDTI, BCLK and LRCK pins are connected to external system. Audio data format has four kinds of mode, the data format is MSB-first, 2's compliment. Setting by DIF0-1 bit. The default value is DIF0 = DIF1 = "0".

No.	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	LRCK	BCLK
0	0	0	20bit MSB justified	20bit LSB justified	Lch: "H", Rch: "L"	≥ 40fs
1	0	1	20bit MSB justified	16bit LSB justified	Lch: "H", Rch: "L"	≥ 32fs
2	1	0	20bit MSB justified	24bit LSB justified	Lch: "H", Rch: "L"	≥ 48fs
3	1	1	I^2S Compatible	I^2S Compatible	Lch: "L", Rch: "H"	≥ 40fs

Table 1. Audio Data Format

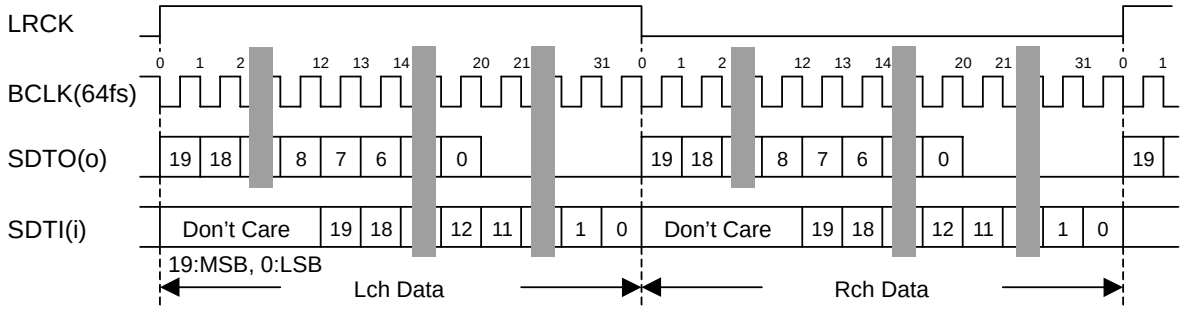


Figure 7. Audio Data Format (No.0)

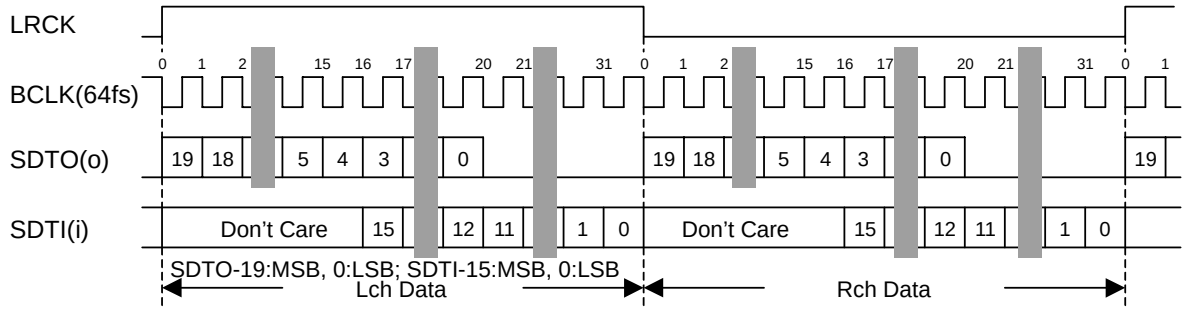


Figure 8. Audio Data Format (No.1)

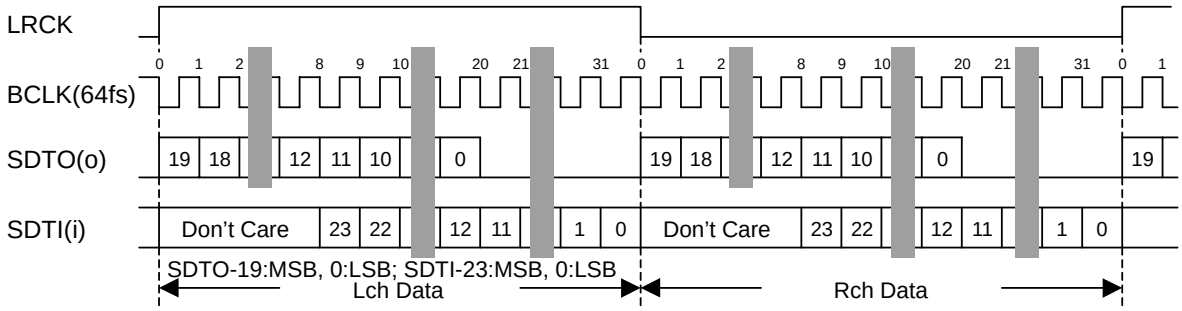


Figure 9. Audio Data Format (No.2)

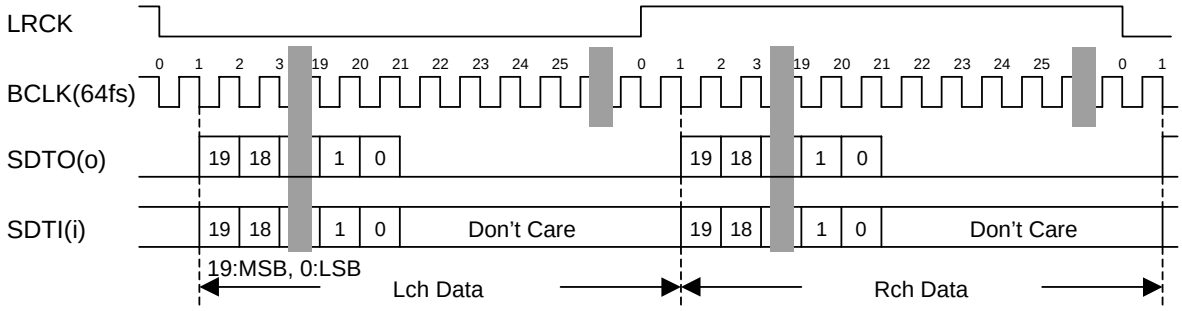


Figure 10. Audio Data Format (No.3)

■ Digital High Pass Filter

The AK4562 has a Digital High Pass Filter (HPF) to cancel DC-offset in ADC and IPGA. The cut-off frequency of the HPF is 3.4Hz at fs=44.1kHz. It also scales with the sampling frequency (fs).

■ System Reset & Offset Calibration

The AK4562 should be reset once by bringing PDN pin "L" after power-up. The control register values are initialized by PDN "L".

Offset calibration starts by PDN pin "L" to "H". It takes 4128/fs to offset calibration cycle. During offset calibration, the ADC digital data outputs of both channels are forced to a 2's compliment "0". Output data of settles data equivalent for analog input signal after offset calibration. This cycle is not for DAC. IPGA and OPGA are set MUTE during offset calibration and after offset calibration.

As a normal offset calibration may not be executed, nothing write at address 01H during offset calibration.

When offset calibration is executed once, the calibration memory is held even if each block is powered down (PM0 = "0" or PM3 = "0") by power management bits.

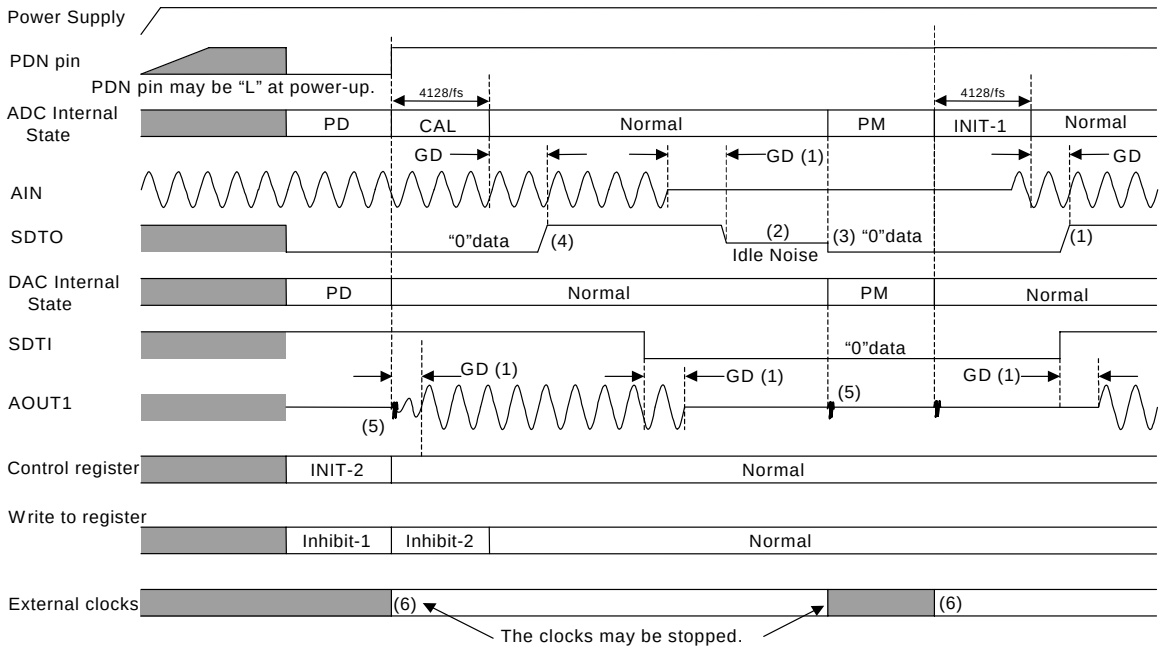


Figure 11. Power up / Power down Timing Example

- PD: Power-down state. ADC is output "0", analog output of DAC and OPGA goes floating.
- PM: Power-down state by Power Management bit. ADC is output "0", analog output of DAC goes floating.
- CAL: During offset calibration cycle. IPGA and OPGA are set MUTE state.
- INIT-1: Initialize cycle of ADC. Offset calibration is not executed.
- INIT-2: Initializing all control registers.
- Inhibit-1: Inhibits writing to all control registers.
- Inhibit-2: Enable writing to control registers except address 01H.

Note: See "Register Definitions" about the condition of each register.

(1). Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD). Output signal gradually comes to settle to input signal during a group delay.

(2). If the analog signal does not be input, digital outputs have the offset to op-amp of input and some offset error of a internal ADC.

(3). ADC output is "0" at power down.

(4). This figure shows that MUTE of IPGA is canceled during offset calibration. If MUTE of IPGA is canceled, SDTO outputs Idle Noise.

(5). Click noise occurs at the "↑↓" of PDN signal. Please mute the analog output external if the click noise influences system application.

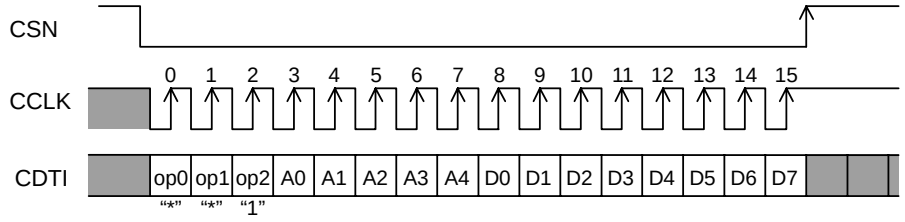
(6). When the external clocks (MCLK, BCLK and LRCK) are stopped, the AK4562 should be in the power down (PDN pin = "L" or PM2-1 bit = "0") mode.

■ Timing of Control Register

- AKM mode

AKM mode is the data in I/F with 3-wire serial control, these data are included by Op-code (3bit), Address (LSB-first, 5bit) and Control data (LSB-first, 8bit). A side of transmitted data is output to each bit by "↓" of CCLK, a side of receiving data is input by "↑" of CCLK. Writing of data becomes effective by "↑" of CSN. CSN should be held to "H" at no access.

Address except 00H ~ 04H inhibits control of writing. And CCLK always need 16 edges of "↑" during CSN = "L".



op0-op2: Op code (Fixed to "**1:WRITE")
A0-A4: Register Address
D0-D7: Control data

Figure 12. Control Data Timing (AKM)

- SSB mode

SSB mode is the data in I/F with 2-wire serial interface, these data are included by information bit (3bit) and data bit (LSB-first, 8bit). Serial clock (SCK) is burst-transmitted, not continuous receiving data. Transmitter outputs each bit by "↑" of SCK, receiver latches the bit when transmitting the data is input by "↓" of SCK. Writing of data and command becomes effective by next "↑" of SCK after taking in the last data bit (D7).

Address except 00H ~ 04H inhibits control of writing.

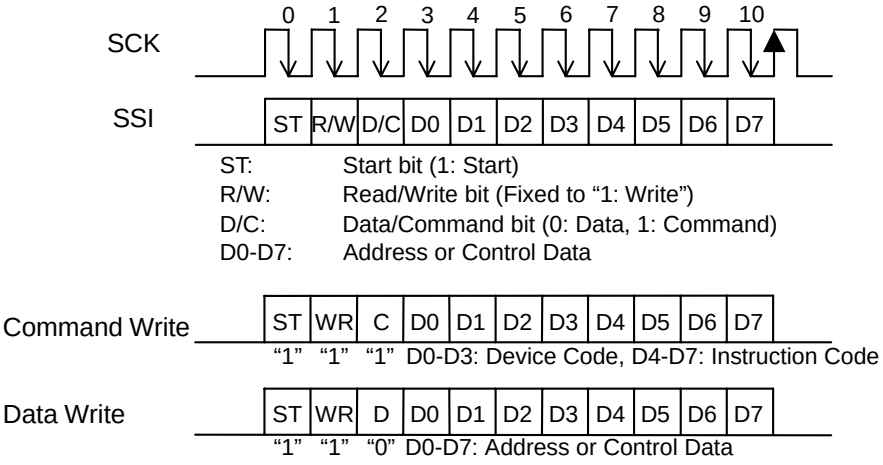


Figure 13. Control Data Timing (SSB)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Select	0	0	0	0	RIN2	RIN1	LIN2	LIN1
01H	Mode Control 1	0	0	0	0	PM3	PM2	PM1	PM0
02H	Mode Control 2	MONO1	MONO0	ZTM1	ZTM0	DEM1	DEM0	DIF1	DIF0
03H	Input Analog PGA Control	ZEIP	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
04H	Output Analog PGA Control	ZEOP	OPGA6	OPGA5	OPGA4	OPGA3	OPGA2	OPGA1	OPGA0

All registers are reset at PDN = “L”, then inhibits writing to all registers.

■ Register Definition

Input Select

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Select	0	0	0	0	RIN2	RIN1	LIN2	LIN1
RESET		0	0	0	0	0	1	0	1

LIN2-1: Select ON/OFF of Lch input. (0: OFF, 1: ON)
RIN2-1: Select ON/OFF of Rch input. (0: OFF, 1: ON)

Mode Control 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Mode Control 1	0	0	0	0	PM3	PM2	PM1	PM0
RESET		0	0	0	0	1	1	1	1

PM3-0: Power Management (0: Power down, 1: Power up)
PM0: Power control of IMIX and IPGA
PM1: Power control of ADC
PM2: Power control of DAC
PM3: Power control of OPGA

PM3-0 can be partly powered-down by ON/OFF of PM3-0. When PDN pin goes “L”, all circuit in the AK4562 can be powered-down in no relation to PM3-0. When PM3-0 goes all “0”, all circuit in the AK4562 can be also powered-down. However, the contents of control registers are held.

In case of PM1 = “1” or PM2 = “1”, MCLK is not stopped.
In case of PM0 = “1” or PM3 = “1”, the powered-up circuit does not need MCLK. However, zero crossing detection can not operate in this case.

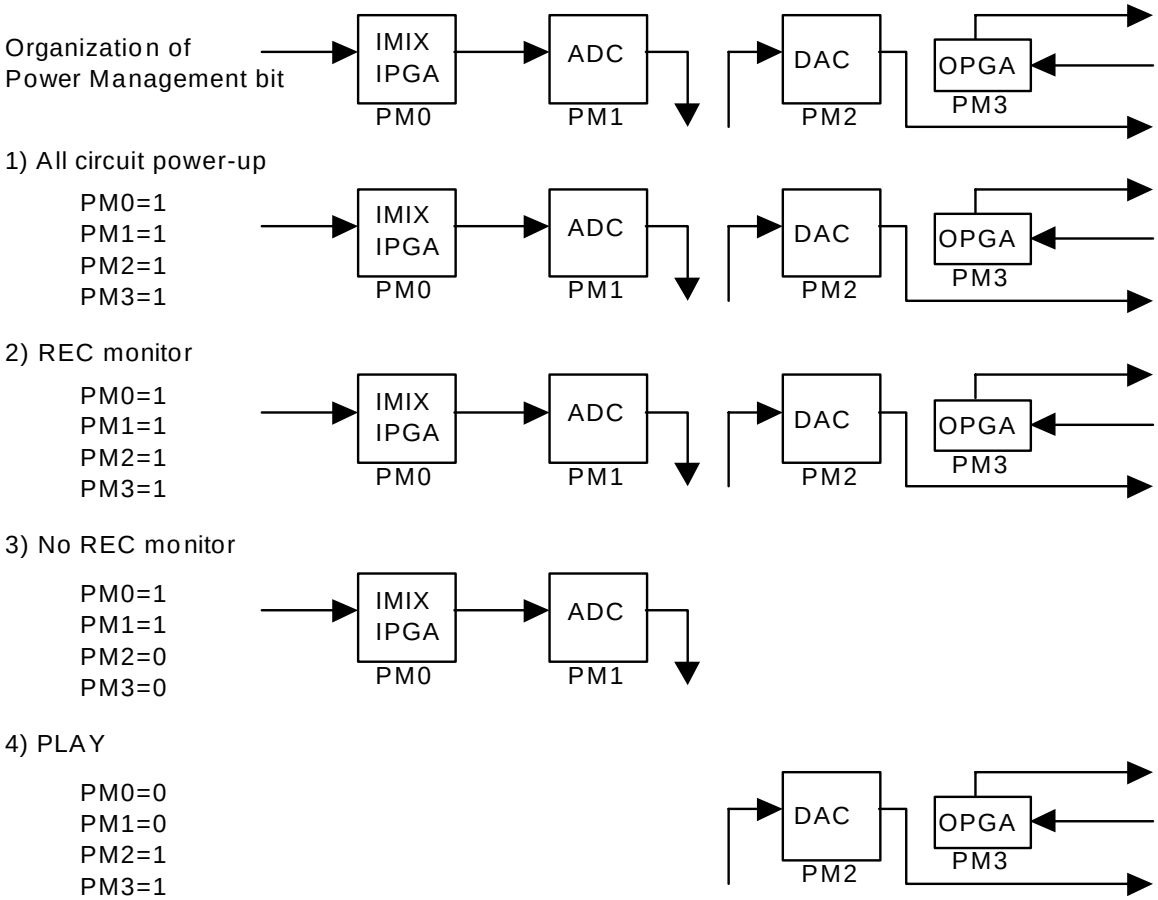


Figure 14. Power Management

Mode Control 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Mode Control 2	MONO1	MONO0	ZTM1	ZTM0	DEM1	DEM0	DIF1	DIF0
RESET		0	0	1	1	0	1	0	0

MONO1-0: Monaural Mixing
- 00: Stereo (RESET)
- 01: (L+R)/2
- 10: LL
- 11: RR

ZTM1-0: Setting of Zero Crossing Timeout for IPGA and OPGA
- 00: 256/fs
- 01: 512/fs
- 10: 1024/fs
- 11: 2048/fs (RESET)

DEM1-0: Select Frequency of De-emphasis
- 00: 44.1kHz ON
- 01: OFF (RESET)
- 10: 48kHz ON
- 11: 32kHz ON

DIF1-0: Select Digital Interface Format

No.	DIF1 bit	DIF0 bit	SDTO(ADC)	SDTI(DAC)	LRCK	BCLK	
0	0	0	20bit MSB justified	20bit LSB justified	Lch: “H”, Rch: “L”	≥ 40fs	Reset
1	0	1	20bit MSB justified	16bit LSB justified	Lch: “H”, Rch: “L”	≥ 32fs	
2	1	0	20bit MSB justified	24bit LSB justified	Lch: “H”, Rch: “L”	≥ 48fs	
3	1	1	I^2S Compatible	I^2S Compatible	Lch: “L”, Rch: “H”	≥ 40fs	

Table 2. Audio Data Format

Input Analog PGA Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Input Analog PGA Control	ZEIP	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
RESET		0	00H (MUTE)						

ZEIP: Select IPGA zero crossing operation (0: Disable, 1: Enable)

Writing to IPGA value at ZEIP = "1", IPGA value of L/R channels changes by zero crossing detection or timeout independently.

In the timeout cycle, it is possible to set in ZTM1-0 bit.
When ZTM1-0 is "11", timeout cycle is 2048/fs = 46.4ms (@fs=44.kHz).
When ZEIP is "0", IPGA changes immediately.

IPGA6-0: Input Analog PGA. 97 levels. 00H=MUTE.

ON/OFF of zero crossing detection can be controlled by ZEIP bit.

DATA	GAIN (dB)	Step	Level
60H	+28.0	0.5dB	73
5FH	+27.5		
5EH	+27.0		
•	•		
28H	+0.0		
27H	-0.5		
•	•		
19H	-7.5		
18H	-8.0		
17H	-9.0	1dB	8
16H	-10.0		
•	•		
11H	-15.0		
10H	-16.0		
0FH	-18.0	2dB	12
0EH	-20.0		
•	•		
05H	-38.0		
04H	-40.0		
03H	-44.0	4dB	3
02H	-48.0		
01H	-52.0		
00H	MUTE		1

Table 3. Input Gain Setting

• About zero crossing operation

Comparator for zero crossing detection in the AK4562 has offset. Therefore, it is a possible that IPGA (OPGA) value is changed by zero crossing timeout as zero crossing detection does not occur by a little offset of comparator.

For example, when Lch and Rch are in the state of IPGA (OPGA) = 30H, both channels are set to IPGA (OPGA) = 31H. And then the only Lch completed zero crossing, Rch is waiting for zero crossing detection, zero crossing counter is reset when IPGA (OPGA) is newly written 32H, zero crossing operation starts toward IPGA (OPGA) = 32H in state Lch = 31H, Rch = 30H. Internal IPGA (OPGA) value in the AK4562 has the registers of L/R channels independently, according to change IPGA (OPGA) value independently, IPGA (OPGA) value of L/R channels may become a difference in level.

Therefore, if IPGA (OPGA) is written before zero crossing detection on zero crossing timeout, IPGA (OPGA) is keeping the same value. When IPGA (OPGA) is finished by normal zero crossing timeout on IPGA (OPGA) value of L/R channels does not give a difference in level, the change of IPGA (OPGA) should be written after zero crossing timeout cycle and over.

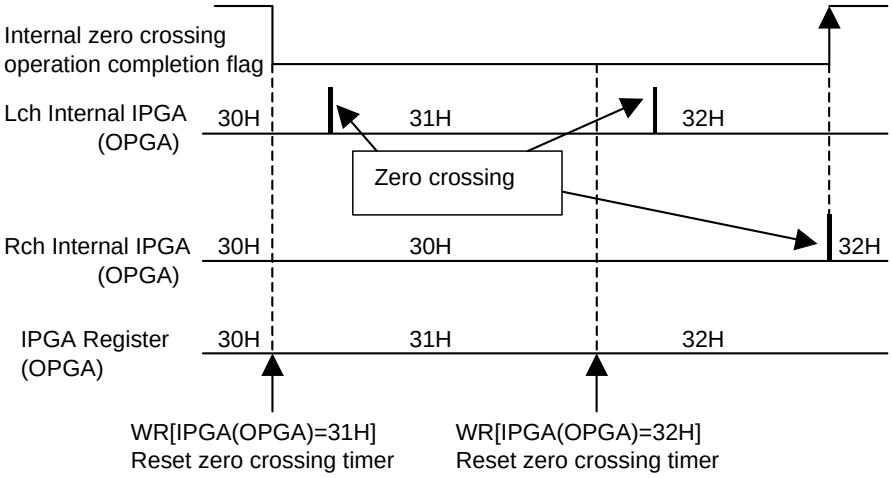


Figure 15. About Zero Crossing Operation

Output Analog PGA Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Output Analog PGA Control	ZEOP	OPGA6	OPGA5	OPGA4	OPGA3	OPGA2	OPGA1	OPGA0
RESET		0	00H (MUTE)						

ZEOP: Select OPGA zero crossing operation (0: Disable, 1: Enable)

Writing to OPGA value at ZEOP = "1", OPGA value of L/R channels changes by zero crossing detection or timeout independently.

Timeout cycle can be set by ZTM1-0 bit.
When ZTM1-0 is "11", timeout cycle is 2048/fs = 46.4ms (@fs=44.kHz).
When ZEOP is "0", OPGA changes immediately.

OPGA6-0: Output Analog PGA. 58 levels. 00H=MUTE.

ON/OFF of zero crossing detection can be controlled by ZEOP bit.
Please do not use 3AH ~ 7FH.

DATA (D6-0)	HEX CODE	OPGA (dB)	Step	Level
011 1001	39H	+0	1dB	35
011 1000	38H	-1		
011 0111	37H	-2		
•	•	•		
001 1000	18H	-33		
001 0111	17H	-34		
001 0110	16H	-36	2dB	22
001 0101	15H	-38		
•	•	•		
000 0011	03H	-74		
000 0010	02H	-76		
000 0001	01H	-78		
000 0000	00H	MUTE		1

Table 4. Output Gain Setting

■ Detail of functions

(1) Input Analog PGA with Zero Crossing Detection

Zero crossing is detected on L/R channels independently. If zero crossing is not detected, IPGA value changes by timeout. Timeout cycle can be set by ZTM1-0 bit. For example, when ZTM1-0 is "11", timeout cycle is 2048/fs = 46.4ms (@fs=44.kHz). Zero crossing detection function can be controlled by ON/OFF of ZEIP bit. If ZEIP is OFF, gain level changes immediately by writing IPGA value.

Offset calibration starts by PDN pin "L" to "H". IPGA is set MUTE during offset calibration and after offset calibration.

(2) Monaural Mixing

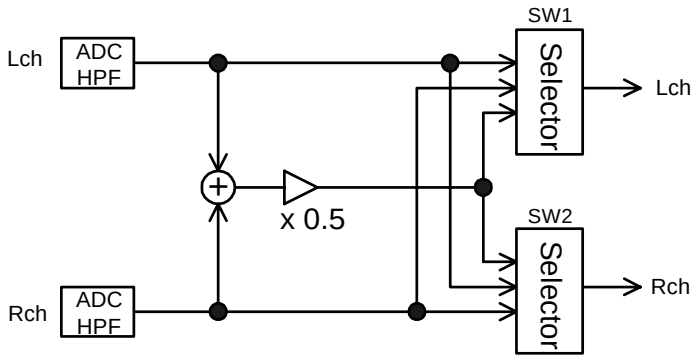


Figure 16. Monaural Mixing

Mode	SW1	SW2	MONO1	MONO0
Stereo Recording	Lch	Rch	0	0
Monaural Recording Stereo Input	(L+R)/2	(L+R)/2	0	1
Monaural Recording Lch Input only	Lch	Lch	1	0
Monaural Recording Rch Input only	Rch	Rch	1	1

Table 5. Monaural Mode Setting

(3) De-emphasis

Include digital de-emphasis filter circuit with tc=50/15us.

(4) Output Analog PGA with Zero Crossing Detection

Zero crossing is detected on L/R channels independently. If zero crossing is not detected, OPGA value changes by timeout. Timeout cycle can be set by ZTM1-0 bit. For example, when ZTM1-0 is "11", timeout cycle is 2048/fs = 46.4ms (@fs=44.kHz). Zero crossing detection function can be controlled by ON/OFF of ZEOP bit. If ZEOP is OFF, gain level changes immediately by writing OPGA value.

Offset calibration starts by PDN pin "L" to "H". OPGA is set MUTE during offset calibration and after offset calibration.

Usually, to remove the offset of DAC, it needs a capacitor (Ca) between LOUT1/ROUT1 and OPGAL/OPGAR. The cut off frequency is decided by capacity of Ca and input impedance (typ. 50kΩ) of OPGA.

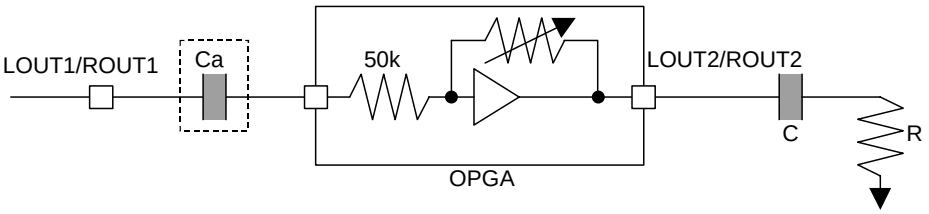


Figure 17. Example of Connection between LOUT1/ROUT1 and LOUT2/ROUT2

(5) Power Management

Power down and analog through mode in each block are controlled by 4bit.

(6) SSB I/F

♦ Summary
- 2-wire
- Bit Rate: Max. 4Mbps
- AK4562 has the device code (Max. 4bits, AK4562 is fixed to "05H".), enable to connect bus to the maximum 16 devices.
  Each device accepts data after recognizing own device code.
- Data transmitting to continuity address is enabled by the appointed address at once as there is the auto-increment/auto-decrement functions.
- The counter with 14 bit shift register starts from a start bit, if there is a 14th carrier, the counter is reset by recognizing the first "1" as the start bit.

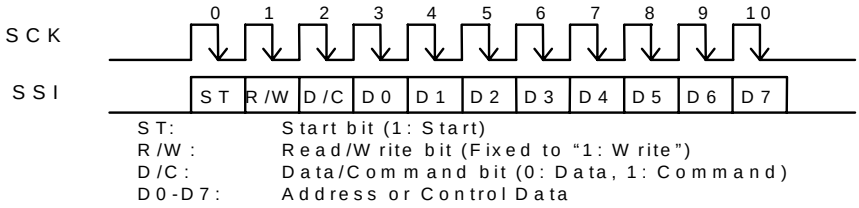


Figure 18. SSB Timing

• Write command

When D/C bit is “1”, 8 bit data after information bits indicates a command.

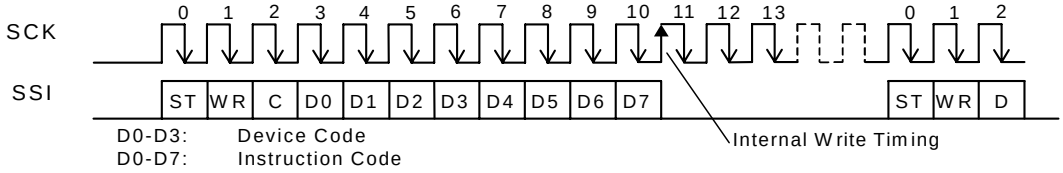


Figure 19. Write Command Timing

• Device code

D0-3 bits are the device code, the bus can be connected to maximum 16 devices, however, and the device code is fixed to 05H in the AK4562.

• Instruction code

The following instruction is set by D4-D7 bits.

Instruction Code				Command	Function
D4	D5	D6	D7		
0	0	0	0	RESET	Only the contents of control register are reset.
1	0	0	0	ADRSL	When the next data is data write, the address is sent. If not so, this command is invalidated.
0	1	0	0	NOP	Invalidity
1	1	0	0	AINC	Auto increment mode of address Holds this state until sending the next ADEC and AHOLD.
0	0	1	0	ADEC	Auto decrement mode of address Holds this state until sending the next AINC and AHOLD.
1	0	1	0	AHOLD	Fixed mode of address Holds this state until sending the next AINC and ADEC.
0	1	1	0	NOP	Invalidity
- - - - -					
0	1	1	1		
1	1	1	1	RESET	Only the contents of control register are reset.

Table 6. SSB Instruction

SSB I/F becomes disable by PDN = “L”, it is set to address = “00H”, AHOLD mode. Therefore, after exiting PDN = “L” at power-on, SSB I/F is enabled by writing command (including NOP) of a appointed device code and accepts data WRITE ever since.

• Data write

When D/C bit is “0”, 8 bit data after the information bits indicates Data. If ADRSL command is sent just before the data is written as the address. The control data is sent in the other case.

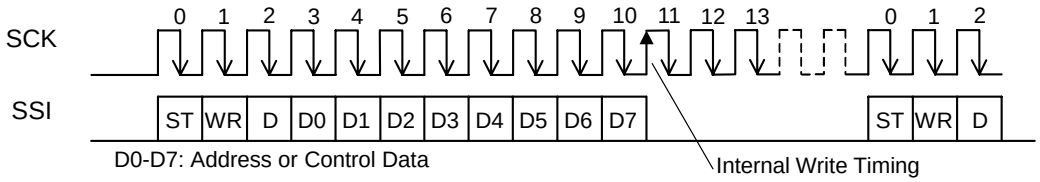
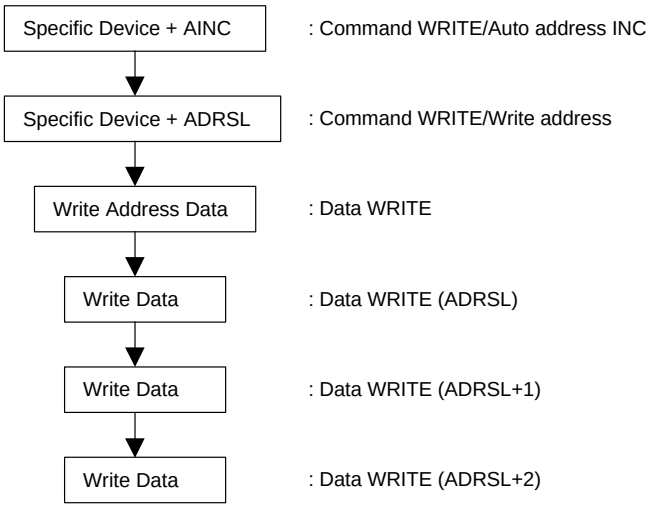


Figure 20. Data Write Timing

- Example for access of Command and Data

[WRITE Operation]



Until coming the command of the next specific device after coming the command except specific device, SSB I/F becomes disable and writing address and writing of data are not complete done. It becomes enable at coming a command of specific device and keeps the state until coming the command except the next specific device.

When address auto-increment mode or address auto-decrement mode is set, the internal address is updated after completing the operation of writing the data. ADRSL in 00H ~ 04H is capable to use, but writing should not be done at setting the address except that.

SYSTEM DESIGN

Figure 21 shows the system connection diagram. An evaluation board [AKD4562] is available which demonstrates application circuit, optimum layout, power supply arrangements and measurement results.

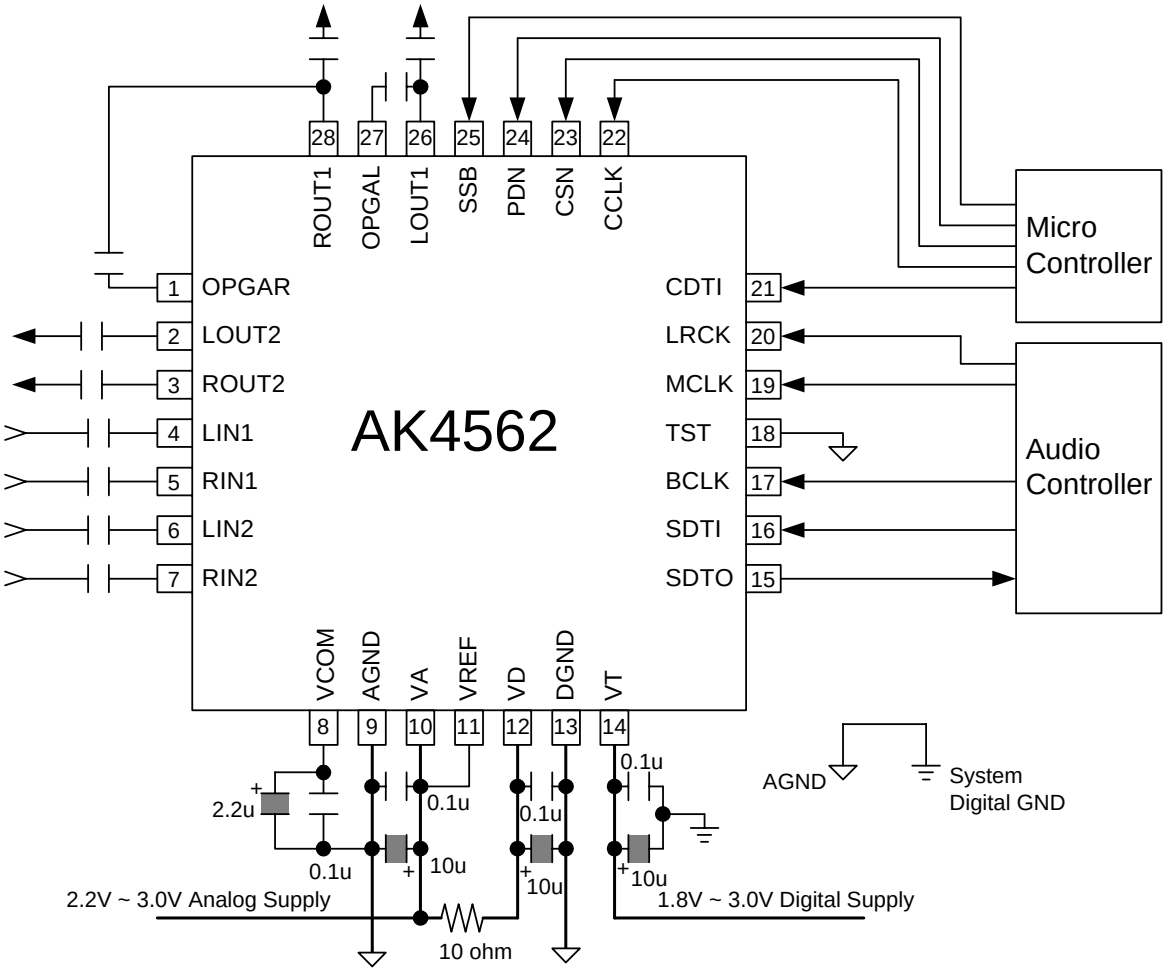


Figure 21. System Connection Diagram Example

Notes:

- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- TST pin always fixes to “L”.
- AGND and DGND pins connect to AGND.

1. Grounding and Power Supply Decoupling

The AK4562 requires careful attention to power supply and grounding arrangements. VA and VD are usually supplied from analog supply in system. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. VT is a power supply pin to interface with the external ICs and is supplied from digital supply in system. AGND and DGND of the AK4562 should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4562 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The differential voltage between VREF and AGND sets the analog input/output range. VREF pin is normally connected to VA with a 0.1uF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 2.2uF parallel with a 0.1uF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4562.

3. Analog Inputs

The analog inputs are single-ended and the input resistance 9kΩ (typ). The input signal range scales with the VREF voltage and nominally 0.6 x VREF Vpp (typ) centered in the internal common voltage (typ. 0.45 x VA). Usually, the input signal cuts DC with a capacitor. The cut-off frequency is $fc=(1/2\pi RC)$. The AK4562 can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFH(@20bit) for input above a positive full scale and 80000H(@20bit) for input below a negative fill scale. The ideal code is 00000H(@20bit) with no input signal. The DC offset including ADC own DC offset removed by the internal HPF (fc=3.4Hz).

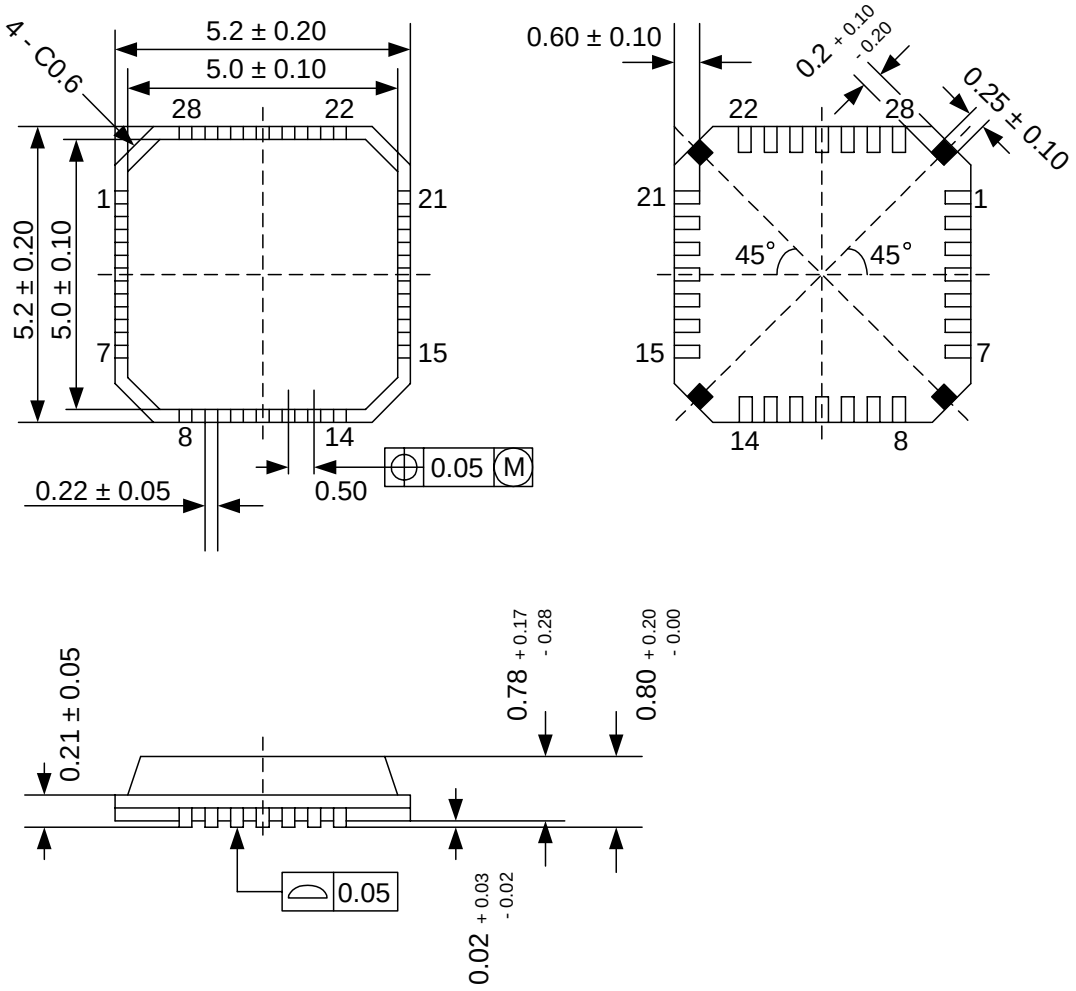
4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage (typ 0.45 x VA). The input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp (typ). The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFH(@20bit) and a negative full scale for 80000H(@20bit). The ideal output is VCOM voltage for 00000H(@20bit). If the noise generated by the delta-sigma modulator beyond the audio band would be the problem, the attenuation by external filter is required.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have VCOM and DC offsets of a few mV.

PACKAGE

● 28pin QFN (Unit: mm)

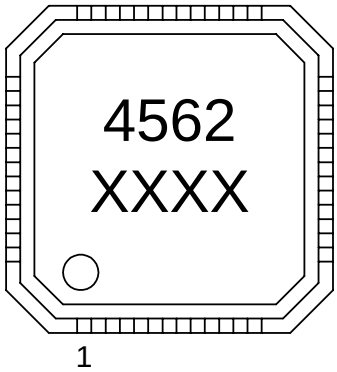


Note : The black parts of back package should be open.

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



XXXX : Date code identifier

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