



AK4377A

Low-Power Advanced 32-bit DAC with HP

1. General Description

The AK4377A is stereo advanced 32-bit high sound quality audio DAC with a built-in ground-referenced headphone amplifier. An internal circuit integrates 32-bit digital filters for better sound quality, achieving low distortion characteristics and wide dynamic range. The sampling frequency supports up to 384 kHz. The AK4377A is available in a 36-pin CSP package, utilizing less board space than competitive offerings.

2. Features

1. Stereo High Sound Quality Low Power Advanced 32-bit DAC
 - 4 types of Digital Filter for Sound Color Selection
 - 2 types of Operation Mode (High Performance Mode / Low Power Mode)
2. Ground-referenced Class-G Stereo Headphone-Amp
 - Output Power: 25 mW @ $R_L = 32 \Omega$
60 mW @ $R_L = 16 \Omega$
 - THD+N: -107 dB @ 10 mW, $R_L = 32 \Omega$
-106 dB @ 25 mW, $R_L = 32 \Omega$
 - S/N: 125 dB
 - Output Noise Level: -125 dBV (Analog Volume ≤ -14 dB)
 - Analog Volume: +6 to -20 dB & Mute, 2 dB Step
 - Ground Loop Noise Cancellation
3. HeadPhone-Amp Output comply with IEC61000-4-2 Level4 ESD Protection
4. Digital Audio interface
 - Master/Slave mode
 - Sampling Frequency:
 - Slave Mode: 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 128 k, 176.4 k, 192 kHz, 256 k, 352.8 k, 384 kHz
 - Master Mode: 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 176.4 k, 192 kHz
 - Interface Format: 32/24/16-bit I²S/MSB justified
5. Power Management
6. PLL
7. X'tal Oscillator
8. μ P I/F: I²C (400 kHz)
9. Ta = -40 to 85 °C
10. Power Supply:
 - AVDD (DAC, PLL): 1.7 to 1.9 V
 - CVDD (HP-Amp, Charge Pump): 1.7 to 1.9 V
 - LVDD (LDO2 for Digital Core): 1.7 to 1.9 V (built-in LDO)
 - TVDD (Audio I/F): 1.65 to 3.6 V
11. Package: 36-pin CSP (2.56 x 2.74 mm, 0.4 mm pitch)

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4. Block Diagram and Functions

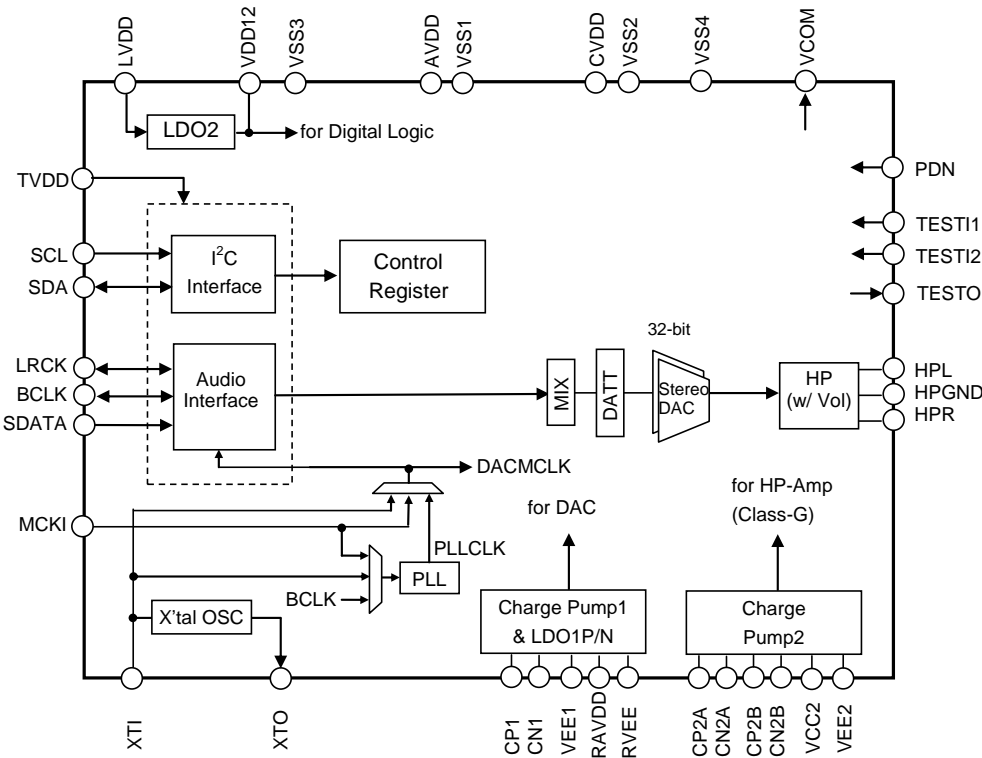
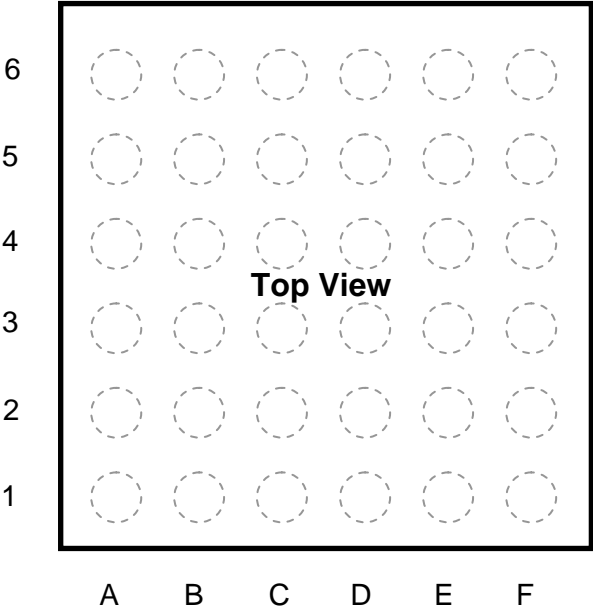


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations

36-pin CSP (2.56 x 2.74 mm, 0.4 mm pitch)



| | | | | | | |
|---|-------|-------|--------|-------|-------|------|
| 6 | VDD12 | SDATA | LVDD | VEE1 | CN1 | CVDD |
| 5 | VSS3 | LRCK | PDN | CP1 | CP2B | CN2B |
| 4 | BCLK | TVDD | TESTI1 | VSS2 | CP2A | CN2A |
| 3 | MCKI | SDA | TESTI2 | TESTO | VCC2 | VEE2 |
| 2 | XTO | SCL | VSS4 | VSS1 | HPGND | HPR |
| 1 | XTI | RAVDD | RVEE | AVDD | VCOM | HPL |
| | A | B | C | D | E | F |

Top View

■ Pin Functions

| No. | Pin Name | I/O | Function | Protection Diode | Power Domain |
|---------------------|----------|-----|--|------------------|--------------|
| Power Supply | | | | | |
| D1 | AVDD | - | Analog Power Supply Pin | | AVDD |
| D2 | VSS1 | - | Analog Ground Pin | | |
| F6 | CVDD | - | HP-Amp/Charge Pump Power Supply Pin | | CVDD |
| D4 | VSS2 | - | HP-Amp/Charge Ground Pin | | |
| C6 | LVDD | - | Digital Core & LDO2 Power Supply Pin | | LVDD |
| A5 | VSS3 | - | Digital Ground Pin | | |
| C2 | VSS4 | - | Substrate Pin | | |
| B4 | TVDD | - | Digital I/F Power Supply Pin | | TVDD |
| E1 | VCOM | O | Common Voltage Output Pin This pin must be connected to the VSS1 pin with a 10 $\mu\text{F} \pm 50\%$ Ceramic capacitor in series. (Note 2) | AVDD/ VSS1 | |
| A6 | VDD12 | - | LDO2 (1.2 V) Output Power Supply Pin (Note 1) This pin must be connected to the VSS3 pin with a capacitor in series. (Note 2) | LVDD/ VSS1 | LVDD |

Note 1. Capacitor value for the VDD12 pin should be selected from 2.2 $\mu\text{F} \pm 50\%$ to 4.7 $\mu\text{F} \pm 50\%$.

Note 2. Do not connect a load to the VCOM pin and the VDD12 pin.

| No. | Pin Name | I/O | Function | Protection Diode | Power Domain |
|------------------------------|----------|-----|---|------------------|--------------|
| Charge Pump & LDO | | | | | |
| E3 | VCC2 | O | Charge Pump Circuit Positive Voltage Output Pin (CVDD or 1/2*CVDD) This pin must be connected to the VSS2 pin with a $2.2\ \mu\text{F} \pm 50\%$ capacitor in series. (Note 4) | CVDD/ VSS2 | CVDD |
| E4 | CP2A | O | Positive Charge-Pump Capacitor Terminal 2A Pin This pin must be connected to the CN2A pin with a $2.2\ \mu\text{F} \pm 50\%$ capacitor in series. | CVDD/ VSS2 | CVDD |
| F4 | CN2A | I | Negative Charge Pump Capacitor Terminal 2A Pin This pin must be connected to the CP2A pin with a $2.2\ \mu\text{F} \pm 50\%$ capacitor in series. | CVDD | CVDD |
| E5 | CP2B | O | Positive Charge Pump Capacitor Terminal 2B Pin This pin must be connected to the CN2B pin with a $2.2\ \mu\text{F} \pm 50\%$ capacitor in series. | CVDD/ VSS2 | CVDD |
| F5 | CN2B | I | Negative Charge Pump Capacitor Terminal 2B Pin This pin must be connected to the CP2B pin with a $2.2\ \mu\text{F} \pm 50\%$ capacitor in series. | CVDD | CVDD |
| F3 | VEE2 | O | Charge Pump Circuit Negative Voltage (–CVDD or –1/2*CVDD) Output 2 Pin This pin must be connected to the VSS2 pin with a $2.2\ \mu\text{F} \pm 50\%$ capacitor in series. (Note 4) | CVDD/ VSS2 | |
| D5 | CP1 | O | Positive Charge Pump Capacitor Terminal 1 Pin This pin must be connected to the CN1 pin with a $1\ \mu\text{F} \pm 50\%$ capacitor in series. | CVDD/ VSS2 | CVDD |
| E6 | CN1 | I | Negative Charge Pump Capacitor Terminal 1 Pin This pin must be connected to the CP1 pin with a $1\ \mu\text{F} \pm 50\%$ capacitor in series. | CVDD | CVDD |
| D6 | VEE1 | O | Charge Pump Circuit Negative Voltage (–CVDD) Output 1 Pin This pin must be connected to the VSS2 pin with a $1\ \mu\text{F} \pm 50\%$ capacitor in series. (Note 4) | CVDD/ VSS2 | |
| B1 | RAVDD | O | LDO1P (1.5 V) Output Pin (Note 3) This pin must be connected to the VSS1 pin with a capacitor in series. (Note 4) | AVDD/ VSS1 | |
| C1 | RVEE | O | LDO1N (–1.5 V) Output Pin (Note 3) This pin must be connected to the VSS1 pin with a capacitor in series. (Note 4) | AVDD/ VSS1 | |

Note 3. Capacitor values for the RAVDD pin and the RVEE pin should be selected from $1\ \mu\text{F} \pm 50\%$ to $4.7\ \mu\text{F} \pm 50\%$.

Note 4. Do not connect a load to the VEE1 pin, VCC2 pin, VEE2 pin, RAVDD pin and the RVEE pin.

| No. | Pin Name | I/O | Function | Protection Diode | Power Domain |
|--------------------------|----------|-----|--|------------------|---------------|
| Control Interface | | | | | |
| B2 | SCL | I | I ² C Serial Data Clock Pin | TVDD/ VSS3 | TVDD |
| B3 | SDA | I/O | I ² C Serial Data Input/Output Pin | TVDD/ VSS3 | TVDD |
| Audio Interface | | | | | |
| A3 | MCKI | I | External Master Clock Input Pin | TVDD/ VSS3 | TVDD |
| A1 | XTI | I | X'tal Oscillator Input Pin | AVDD/ VSS1 | AVDD |
| A2 | XTO | O | X'tal Oscillator Output Pin | AVDD/ VSS1 | AVDD |
| A4 | BCLK | I/O | Audio Serial Data Clock Pin | TVDD/ VSS3 | TVDD |
| B5 | LRCK | I/O | Frame Sync Clock Pin | TVDD/ VSS3 | TVDD |
| B6 | SDATA | I | Audio Serial Data Input Pin | TVDD/ VSS3 | TVDD |
| Analog Output | | | | | |
| F1 | HPL | O | Lch Headphone-Amp Output Pin | CVDD/ VEE2 | CVDD/ VEE2 |
| F2 | HPR | O | Rch Headphone-Amp Output Pin | CVDD/ VEE2 | CVDD/ VEE2 |
| E2 | HPGND | I | Headphone-Amp Ground Loop Noise Cancellation Pin | - | - |
| Others | | | | | |
| C5 | PDN | I | Power down Pin "L": Power-down, "H": Power-up | TVDD/ VSS3 | TVDD |
| C4 | TESTI1 | I | Test Input Pin It must be tied "L". | TVDD/ VSS3 | TVDD |
| D3 | TESTO | O | Test Output Pin | AVDD/ VSS1 | AVDD |
| C3 | TESTI2 | I | Test Input Pin It must be tied "L". | TVDD/ VSS3 | TVDD |

Note 5. The SCL pin, SDA pin, MCKI pin, BCLK pin, LRCK pin, SDATA pin, HPGND pin, PDN pin, TESTI1 pin and the TESTI2 pin must not be allowed to float. I/O pins should be connected appropriately.

■ Handing of Unused Pins

Unused I/O pins must be connected appropriately.

| Classification | Pin Name | Setting |
|----------------|----------------------|----------------------------------|
| Analog | HPL, HPR, XTO | Open |
| | XTI | Open (PMOSC bit is fixed to "0") |
| Digital | TESTO | Open |
| | MCKI, TESTI1, TESTI2 | Connect to VSS3 |

6. Absolute Maximum Ratings

(VSS1 = VSS2 = VSS3 = VSS4 = 0 V; [Note 7](#), [Note 8](#))

| Parameter | | Symbol | Min. | Max. | Unit |
|---|-----------------------|--------|------|-------------------|------|
| Power Supplies: (Note 6) | Analog | AVDD | -0.3 | 4.3 | V |
| | HP-Amp/Charge Pump | CVDD | -0.3 | 4.3 | V |
| | LDO2 for Digital Core | LVDD | -0.3 | 4.3 | V |
| | Digital I/F | TVDD | -0.3 | 4.3 | V |
| Input Current, Any Pin Except Supplies | | IIN | - | ±10 | mA |
| Analog Input Voltage (Note 9) | | VINA | -0.3 | AVDD + 0.3 or 4.3 | V |
| Digital Input Voltage (Note 10) | | VIND | -0.3 | TVDD + 0.3 or 4.3 | V |
| Ambient Temperature (powered applied) | | Ta | -40 | 85 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Note 6. Charge pump 1 & 2 are not in operation. In the case that charge pump 1 & 2 are in operation, the maximum values of AVDD and CVDD become 2.15 V.

Note 7. All voltages with respect to ground.

Note 8. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog plane.

Note 9. XTI pin

The maximum value of input voltage is lower value between (AVDD + 0.3) V and 4.3 V.

Note 10. MCKI, BCLK, LRCK, SDATA, SCL, SDA, PDN, TESTI1, TESTI2 pins

The maximum value of input voltage is lower value between (TVDD + 0.3) V and 4.3 V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal Operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 = VSS2 = VSS3 = VSS4 = 0 V; [Note 11](#))

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|-----------------------|--------|------|------|------|------|
| Power supplies (Note 12) | Analog | AVDD | 1.7 | 1.8 | 1.9 | V |
| | HP-Amp / Charge Pump | CVDD | 1.7 | 1.8 | 1.9 | V |
| | LDO2 for Digital Core | LVDD | 1.7 | 1.8 | 1.9 | V |
| | Digital I/F | TVDD | 1.65 | 1.8 | 3.6 | V |

Note 11. All voltages with respect to ground.

Note 12. Each power up/down sequence is shown below.

<Power-up>

1. PDN pin = "L"
2. TVDD, AVDD, LVDD, CVDD
(AVDD must be powered up before or at the same time of CVDD. The power-up sequence of TVDD and LVDD is not critical.)
3. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

<Power-down>

1. PDN pin = "L"
2. TVDD, AVDD, LVDD, CVDD
(CVDD must be powered down before or at the same time of AVDD. The power-down sequence of TVDD and LVDD is not critical.)

8. Electrical Characteristics

■ Analog Characteristics

(Ta = 25 °C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V;
Signal Frequency = 1 kHz; 24-bit Data; fs = 44.1 kHz, BCLK = 64 fs; Measurement Bandwidth = 20 Hz to 20 kHz; unless otherwise specified)

<High Performance Mode>

| Parameter | Min. | Typ. | Max. | Unit | |
|---|---|------|------|------|----|
| Stereo DAC Characteristics: | | | | | |
| Resolution | - | - | 32 | Bit | |
| Headphone-Amp Characteristics: | | | | | |
| DAC (Stereo) → HPL/HPR pins, OVL/R = 0 dB, HPG = 0 dB, R _L = 32 Ω | | | | | |
| Output Power | | | | | |
| 0 dBFS, R _L = 32 Ω, HPG = 0 dB, | - | 25 | - | mW | |
| 0 dBFS, R _L = 32 Ω, HPG = -4 dB | - | 10 | - | mW | |
| R _L = 16 Ω, HPG = 0 dB, THD+N < -60 dB | - | 45 | - | mW | |
| R _L = 16 Ω, HPG = +2 dB, THD+N < -20 dB | - | 60 | - | mW | |
| Output Level (0 dBFS, R _L = 32Ω, HPG = -4 dB) (Note 13) | 0.52 | 0.57 | 0.61 | Vrms | |
| THD+N | | | | | |
| 0 dBFS, R _L = 32 Ω, HPG = -4 dB (P _o = 10 mW) | f _s = 44.1 kHz BW = 20 kHz | - | -107 | - | dB |
| | f _s = 96 kHz BW = 40 kHz | - | -103 | - | dB |
| | f _s = 192 kHz BW = 40 kHz | - | -103 | - | dB |
| | f _{in} = 10kHz f _s = 44.1kHz BW = 20kHz | - | -103 | - | dB |
| 0 dBFS, R _L = 32 Ω, HPG = 0 dB (P _o = 25 mW) | f _s = 44.1 kHz BW = 20 kHz | - | -106 | - | dB |
| 0 dBFS, R _L = 32 Ω, OVL = OVR = -10 dB, HPG = 0 dB (P _o = 2.5 mW) | f _s = 44.1 kHz BW = 20 kHz | - | -100 | -90 | dB |
| 0 dBFS, R _L = 16 Ω, HPG = -4 dB (P _o = 20 mW) | f _s = 44.1 kHz BW = 20 kHz | - | -106 | - | dB |
| 0 dBFS, R _L = 600 Ω, HPG = +2 dB, (P _o = 2.0 mW @ 1.1 Vrms) | f _s = 44.1 kHz BW = 20 kHz | - | -104 | - | dB |

| Parameter | Min. | Typ. | Max. | Unit |
|---|--------------------|-----------|---------------|----------|
| Dynamic Range –60 dBFS, A-weighted, HPG = 0 dB | 108 | 116 | - | dB |
| S/N (A-weighted, Noise Gate Enable) Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / “0” Data) | - | 125 | - | dB |
| S/N (A-weighted, Noise Gate Disable) Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / “0” Data) | 108 | 116 | - | dB |
| Output Noise Level (Noise Gate Enable, A-weighted) | - | –126 | - | dBV |
| Output Noise Level (Noise Gate Disable, A-weighted, HPG ≤ –14 dB) | - | –125 | - | dBV |
| Interchannel Isolation 0 dBFS, HPG = –4 dB (Po = 10 mW) External Impedance = 0.01 Ω (Note 14) External Impedance = 0.1 Ω (Note 14) | 80 - | 100 80 | - - | dB dB |
| Interchannel Gain Mismatch | - | 0 | 0.8 | dB |
| Load Resistance | 14.4 | 32 | - | Ω |
| Load Capacitance | - | - | 1000 | pF |
| Load Inductance | - | - | 0.375 | μH |
| PSRR (HPG = –4 dB) (Note 15) 217 Hz 1 kHz | - - | 85 85 | - - | dB dB |
| DC-offset (Note 16) HPG = 0 dB HPG = All Gain | –0.25 –0.4 | 0 0 | +0.25 +0.4 | mV mV |
| Headphone Output Volume Characteristics: | | | | |
| Gain Setting | –20 | - | +6 | dB |
| Step Width | Gain: +6 to –20 dB | 1 | 2 | 3 |

Note 13. Output level is proportional to AVDD. Typ. $0.57 V_{rms} \times AVDD / 1.8 V$ @headphone amplifier gain = –4 dB.

Note 14. Impedance between the HPGND pin and the system ground.

Note 15. PSRR is referred to all power supplies with 100 mVpp sine wave.

Note 16. When there is no gain change and temperature drift after HP-Amp is powered up.

| Parameter | Value | Unit |
|--|-------|------|
| ESD Immunity IEC61000-4-2 Level4, Contact (Note 17) | ±8 | kV |

Note 17. It is measured at the HPL and HPR pins using an evaluation board (AKD4377A-SA Rev.0).

<Low Power Mode>

| Parameter | Min. | Typ. | Max. | Unit | |
|---|------------------------------|-----------|---------------|----------|----|
| Headphone-Amp Characteristics: | | | | | |
| DAC(Stereo) → HPL/HPR pins, OVL/R = 0 dB, HPG = 0 dB, R _L = 32 Ω | | | | | |
| Output Power | | | | | |
| 0 dBFS, R _L = 32 Ω, HPG = 0 dB, | - | 25 | - | mW | |
| 0 dBFS, R _L = 32 Ω, HPG = −4 dB | - | 10 | - | mW | |
| R _L = 16 Ω, HPG = 0 dB,THD+N < −60 dB | - | 45 | - | mW | |
| R _L = 16 Ω, HPG = +2 dB,THD+N < −20 dB | - | 60 | - | mW | |
| Output Level (0 dBFS, R _L = 32 Ω, HPG = −4 dB) (Note 18) | 0.52 | 0.57 | 0.61 | Vrms | |
| THD+N | | | | | |
| 0 dBFS, R _L = 32 Ω, HPG = −4 dB (Po = 10 mW) | fs = 44.1 kHz BW = 20 kHz | - | −98 | - | dB |
| 0 dBFS, R _L = 16 Ω, HPG = −4 dB (Po = 20 mW) | fs = 44.1 kHz BW = 20 kHz | - | −98 | - | dB |
| −4 dBFS,R _L = 600 Ω,HPG = + 6 dB (Po = 2.0 mW @ 1.1 Vrms) | fs = 44.1 kHz BW = 20 kHz | - | −99 | - | dB |
| Dynamic Range (−60 dBFS, A-weighted, HPG = 0 dB, Data = 0 dBFS) | - | 113 | - | dB | |
| S/N (A-weighted) Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / “0” Data) | - | 113 | - | dB | |
| Interchannel Isolation 0 dBFS, HPG = −4 dB (Po = 10 mW) External Impedance = 0.01 Ω (Note 19) External Impedance = 0.1 Ω (Note 19) | 80 - | 100 80 | - - | dB dB | |
| Interchannel Gain Mismatch | - | 0 | 0.8 | dB | |
| Load Resistance | 14.4 | 32 | - | Ω | |
| Load Capacitance | - | - | 1000 | pF | |
| Load Inductance | - | - | 0.375 | μH | |
| PSRR (HPG = −4 dB) (Note 20) 217 Hz 1 kHz | - - | 85 85 | - - | dB dB | |
| DC-offset (Note 21) HPG = 0 dB HPG = All Gain | −0.35 −0.5 | 0 0 | +0.35 +0.5 | mV mV | |
| Headphone Output Volume Characteristics: | | | | | |
| Gain Setting | −20 | - | +6 | dB | |
| Step Width | Gain: +6 to −20 dB | 1 | 2 | 3 | dB |

Note 18. Output level is proportional to AVDD. Typ. $0.57\ \text{Vrms} \times \text{AVDD} / 1.8\ \text{V}$ @headphone amplifier gain = -4 dB.

Note 19. Impedance between the HPGND pin and the system ground.

Note 20. PSRR is referred to all power supplies with 100 mVpp sine wave.

Note 21. When there is no gain change and temperature drift after HP-Amp is powered up.

| Parameter | Value | Unit |
|--|---------|------|
| ESD Immunity IEC61000-4-2 Level4, Contact (Note 22) | ± 8 | kV |

Note 22. It is measured at the HPL and HPR pins using an evaluation board (AKD4377A-SA Rev.0).

■ PLL Characteristics

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; unless otherwise specified)

| Parameter | Min. | Typ. | Max. | Unit |
|---------------------------------------|-------|----------|-------|------|
| PLL Characteristics | | | | |
| Reference Clock (Figure 11) | 0.256 | - | 3.072 | MHz |
| Output Frequency (PLLCLK) (Figure 11) | | | | |
| 44.1 kHz * 256fs * 9 | - | 101.6064 | - | MHz |
| 48.0 kHz * 256fs * 9 | - | 110.592 | - | MHz |
| 44.1 kHz * 256fs * 10 | - | 112.896 | - | MHz |
| 48.0 kHz * 256fs * 10 | - | 122.880 | - | MHz |
| Lock Time | - | - | 2 | ms |

■ Charge Pump & LDO Circuit Power-up Time

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; unless otherwise specified)

| Parameter | Capacitor | Min. | Typ. | Max. | Unit |
|----------------------------------|----------------|------|------|------|------|
| Block power up time | | | | | |
| CP1 (Note 23) | 1 μF @ VEE1 | - | - | 6.5 | ms |
| CP2 (Class-G) (Note 23, Note 24) | 2.2 μF @ VEE2 | - | - | 4.5 | ms |
| LDO1P (Note 25) | 1 μF @ RAVDD | - | - | 1 | ms |
| LDO1N (Note 25) | 1 μF @ RVEE | - | - | 1 | ms |
| LDO2 (Note 23) | 2.2 μF @ VDD12 | - | - | 1 | ms |

Note 23. Power up time is a fixed value that is not affected by a capacitor.

Note 24. Power up time is a value to -1/2CVDD, since CP2 starts with 1/2 VDD Mode as part of Class-G operation.

Note 25. Power-up time is proportional to a capacitor value.

For instance, if a 2.2 μF capacitor is connected to the RVEE pin, LDO1N power-up time is 2.2 ms (max.).

■ Power Supply Current

(Ta = 25 °C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V, BCLK = 64 fs; Slave Mode, No Data input, RL = 32 Ω; unless otherwise specified)

| Parameter | Min. | Typ. | Max. | Unit |
|---|------|------|------|------|
| Power Supply Current: | | | | |
| Power Up (PDN pin = "H", All Circuits Power-up) (Note 26) | | | | |
| AVDD+ CVDD + LVDD + TVDD | - | 23 | - | mA |
| Power Up (PDN pin = "H", DAC+HP-amp Power-Up, PLL & X'tal OSC Power Down) (Note 27) | | | | |
| AVDD+ CVDD + LVDD + TVDD | - | 20 | 30 | mA |
| Power Down (PDN pin = "L") | | | | |
| AVDD + CVDD + LVDD + TVDD | - | 0 | 10 | μA |

Note 26. DAC, Headphone-Amplifier, PLL and X'tal OSC are all powered up.

Note 27. All digital input pins are fixed to TVDD or VSS3.

■ Power Consumptions for Each Operation Mode

(Ta = 25 °C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = VSS4 = 0 V;
MCKI = 256 fs, BCLK = 64 fs; Slave Mode, No data input, R_L = 32 Ω, X'tal OSC Power-down)

<High Performance Mode>

| | AVDD [mA] | CVDD [mA] | LVDD [mA] | TVDD [mA] | Total Power [mW] |
|--------------------------|--------------|--------------|--------------|--------------|---------------------|
| DAC → HP (fs = 44.1 kHz) | 8.58 | 11.54 | 0.47 | 0.02 | 37.10 |
| DAC → HP (fs = 96 kHz) | 8.68 | 11.64 | 0.57 | 0.02 | 37.64 |
| DAC → HP (fs = 192 kHz) | 8.68 | 11.64 | 0.62 | 0.02 | 37.73 |

<Low Power Mode>

| | AVDD [mA] | CVDD [mA] | LVDD [mA] | TVDD [mA] | Total Power [mW] |
|--------------------------|--------------|--------------|--------------|--------------|---------------------|
| DAC → HP (fs = 44.1 kHz) | 3.23 | 4.03 | 0.36 | 0.02 | 13.75 |

■ DAC Sharp Roll-Off Filter (fs = 44.1 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 44.1 kHz;
DASD bit = "0", DASL bit = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|--------------------------------|--------|--------|------------|------------|------------|
| DAC Digital Filter(LPF): | | | | | | |
| Passband (Note 28) | −0.006 to +0.124 dB −6.0 dB | PB | 0 - | - 22.05 | 20.42 - | kHz kHz |
| Stopband (Note 28) | | SB | 24.1 | - | - | kHz |
| Passband Ripple | | PR | −0.006 | - | +0.124 | dB |
| Stopband Attenuation (Note 29) | | SA | 69.9 | - | - | dB |
| Group Delay (Note 30) | | GD | - | 26 | - | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode : | | | | | | |
| Frequency Response: 0 to 20.0 kHz | | FR | −0.12 | - | +0.03 | dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode : | | | | | | |
| Frequency Response: 0 to 20.0 kHz | | FR | −0.68 | - | +0.03 | dB |

Note 28. The passband and stopband frequencies scale with fs (system sampling rate).

PB = $0.4630 \times fs$ (@ -0.006 / +0.124 dB), SB = $0.5465 \times fs$. Each frequency response refers to that of 1 kHz.

Note 29. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 30. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Sharp Roll-Off Filter (fs = 96 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 96 kHz;
DASD bit = "0", DASL bit = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|--------------------------------|--------|--------|------------|-----------|------------|
| DAC Digital Filter(LPF): | | | | | | |
| Passband (Note 31) | −0.003 to +0.127 dB −6.0 dB | PB | 0 - | - 48.01 | 44.4 - | kHz kHz |
| Stopband (Note 31) | | SB | 52.5 | - | - | kHz |
| Passband Ripple | | PR | −0.003 | - | +0.127 | dB |
| Stopband Attenuation (Note 32) | | SA | 69.9 | - | - | dB |
| Group Delay (Note 33) | | GD | - | 26 | - | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode : | | | | | | |
| Frequency Response: 0 to 40.0 kHz | | FR | −0.72 | - | +0.11 | dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode : | | | | | | |
| Frequency Response: 0 to 40.0 kHz | | FR | −2.18 | - | +0.10 | dB |

Note 31. The passband and stopband frequencies scale with fs (system sampling rate).

PB = $0.4625 \times fs$ (@ -0.003/+0.127 dB), SB = $0.547 \times fs$. Each frequency response refers to that of 1 kHz.

Note 32. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 33. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Sharp Roll-Off Filter (fs = 192 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 192 kHz;
DASD bit = "0", DASL bit = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|--|--------------------|--------|--------|-------|-------|------|
| DAC Digital Filter(LPF): | | | | | | |
| Passband (Note 34) | -0.002 to +0.13 dB | PB | 0 | - | 88.94 | kHz |
| | -6.0 dB | | - | 96.01 | - | kHz |
| Stopband (Note 34) | | SB | 105 | - | - | kHz |
| Passband Ripple | | PR | -0.002 | - | +0.13 | dB |
| Stopband Attenuation (Note 35) | | SA | 69.9 | - | - | dB |
| Group Delay (Note 36) | | GD | - | 26 | - | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode : | | | | | | |
| Frequency Response: 0 to 80.0 kHz | | FR | -2.90 | - | +0.35 | dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode : | | | | | | |
| Frequency Response: 0 to 80.0 kHz | | FR | -6.42 | - | +0.35 | dB |

Note 34. The passband and stopband frequencies scale with fs (system sampling rate).

PB = 0.4538 x fs (@-0.002/+0.13 dB), SB = 0.5469 x fs. Each frequency response refers to that of 1 kHz.

Note 35. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 36. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Slow Roll-Off Filter (fs = 44.1 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 44.1 kHz;
DASD bit = "0", DASL bit = "1")

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|-------------------------------|------|--------|------------|------------|
| DAC Digital Filter(LPF): | | | | | |
| Passband (Note 37) | -0.07 to +0.006 dB -3.0 dB | PB | 0 - | - 18.34 | 7.7 kHz |
| Stopband (Note 37) | | SB | 39.1 | - | kHz |
| Passband Ripple | | PR | -0.07 | - | +0.006 dB |
| Stopband Attenuation (Note 38) | | SA | 72.8 | - | dB |
| Group Delay (Note 39) | | GD | - | 26 | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode : | | | | | |
| Frequency Response: 0 to 20.0 kHz | | FR | -4.44 | - | +0.03 dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode : | | | | | |
| Frequency Response: 0 to 20.0 kHz | | FR | -5.00 | - | +0.03 dB |

Note 37. The passband and stopband frequencies scale with fs (system sampling rate).

PB = $0.1746 \times fs$ (@-0.07/+0.006 dB), SB = $0.887 \times fs$. Each frequency response refers to that of 1 kHz.

Note 38. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 39. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Slow Roll-Off Filter (fs = 96 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 96 kHz;
DASD bit = "0", DASL bit = "1")

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|-------------------------------|------|--------|-----------|--------------|
| DAC Digital Filter (LPF): | | | | | |
| Passband (Note 40) | -0.07 to +0.007 dB -3.0 dB | PB | 0 - | - 39.9 | 16.76 kHz |
| Stopband (Note 40) | | SB | 85.2 | - | kHz |
| Passband Ripple | | PR | -0.07 | - | +0.007 dB |
| Stopband Attenuation (Note 41) | | SA | 72.8 | - | dB |
| Group Delay (Note 42) | | GD | - | 26 | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode: | | | | | |
| Frequency Response: 0 to 40.0 kHz | | FR | -4.00 | - | +0.10 dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode: | | | | | |
| Frequency Response: 0 to 40.0 kHz | | FR | -5.46 | - | +0.10 dB |

Note 40. The passband and stopband frequencies scale with fs (system sampling rate).

PB = $0.1746 \times fs$ (@-0.07/+0.007 dB), SB = $0.887 \times fs$. Each frequency response refers to that of 1 kHz.

Note 41. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 42. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Slow Roll-Off Filter (fs = 192 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 192 kHz;
DASD bit = "0", DASL bit = "1")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|--|--------------------|--------|-------|------|--------|------|
| DAC Digital Filter (LPF): | | | | | | |
| Passband (Note 43) | -0.07 to +0.007 dB | PB | 0 | - | 33.56 | kHz |
| | -3.0 dB | | - | 79.9 | - | kHz |
| Stopband (Note 43) | | SB | 170.3 | - | - | kHz |
| Passband Ripple | | PR | -0.07 | - | +0.007 | dB |
| Stopband Attenuation (Note 44) | | SA | 72.8 | - | - | dB |
| Group Delay (Note 45) | | GD | - | 26 | - | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode : | | | | | | |
| Frequency Response: 0 to 80.0 kHz | | FR | -6.00 | - | +0.35 | dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode : | | | | | | |
| Frequency Response: 0 to 80.0 kHz | | FR | -9.47 | - | +0.35 | dB |

Note 43. The passband and stopband frequencies scale with fs (system sampling rate).

PB = $0.1748 \times fs$ (@ -0.07/+0.007 dB), SB = $0.887 \times fs$. Each frequency response refers to that of 1 kHz.

Note 44. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 45. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Sharp Roll-Off Filter (fs = 44.1 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 44.1 kHz;
DASD bit = "1", DASL bit = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|--|--------------------------------|--------|--------|------------|-----------|------------|
| DAC Digital Filter (LPF): | | | | | | |
| Passband (Note 46) | -0.008 to +0.126 dB -6.0 dB | PB | 0 - | - 22.18 | 20.4 - | kHz kHz |
| Stopband (Note 46) | | SB | 24.1 | - | - | kHz |
| Passband Ripple | | PR | -0.008 | - | +0.126 | dB |
| Stopband Attenuation (Note 47) | | SA | 56.4 | - | - | dB |
| Group Delay (Note 48) | | GD | - | 5.5 | - | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode : | | | | | | |
| Frequency Response: 0 to 20.0 kHz | | FR | -0.12 | - | +0.03 | dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode : | | | | | | |
| Frequency Response: 0 to 20.0 kHz | | FR | -0.68 | - | +0.03 | dB |

Note 46. The passband and stopband frequencies scale with fs (system sampling rate).

PB = $0.4626 \times fs$ (@-0.008/+0.126 dB), SB = $0.5465 \times fs$. Each frequency response refers to that of 1 kHz.

Note 47. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 48. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Sharp Roll-Off Filter (fs = 96 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 96 kHz;
DASD bit = "1", DASL bit = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|-------------------------------|--------|--------|------------|-----------|------------|
| DAC Digital Filter (LPF): | | | | | | |
| Passband (Note 49) | -0.003 to +0.132dB -6.0 dB | PB | 0 - | - 48.28 | 44.4 - | kHz kHz |
| Stopband (Note 49) | | SB | 52.5 | - | - | kHz |
| Passband Ripple | | PR | -0.003 | - | +0.132 | dB |
| Stopband Attenuation (Note 50) | | SA | 56.4 | - | - | dB |
| Group Delay (Note 51) | | GD | - | 5.5 | - | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode: | | | | | | |
| Frequency Response: 0 to 40.0 kHz | | FR | -0.90 | - | +0.11 | dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode: | | | | | | |
| Frequency Response: 0 to 40.0 kHz | | FR | -2.36 | - | +0.10 | dB |

Note 49. The passband and stopband frequencies scale with fs (system sampling rate).

PB = $0.4625 \times fs$ (@-0.003/+0.132 dB), SB = $0.5465 \times fs$. Each frequency response refers to that of 1 kHz.

Note 50. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 51. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Sharp Roll-Off Filter ($f_s = 192$ kHz)

($T_a = -40$ to 85 °C; $AVDD = CVDD = LVDD = 1.7$ to 1.9 V; $TVDD = 1.65$ to 3.6 V; $f_s = 192$ kHz;
DASD bit = "1", DASL bit = "0")

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|--------------------------------|------|--------|------------|-------------------------|
| DAC Digital Filter (LPF): | | | | | |
| Passband (Note 52) | -0.001 to +0.135 dB -6.0 dB | PB | 0 - | - 96.57 | 88.8 - kHz kHz |
| Stopband (Note 52) | | SB | 105 | - | - kHz |
| Passband Ripple | | PR | -0.001 | - | +0.135 dB |
| Stopband Attenuation (Note 53) | | SA | 56.4 | - | - dB |
| Group Delay (Note 54) | | GD | - | 5.5 | - 1/ f_s |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode : | | | | | |
| Frequency Response: 0 to 80.0 kHz | | FR | -3.00 | - | +0.36 dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode : | | | | | |
| Frequency Response: 0 to 80.0 kHz | | FR | -6.52 | - | +0.35 dB |

Note 52. The passband and stopband frequencies scale with f_s (system sampling rate).

PB = $0.4625 \times f_s$ (@ -0.001/+0.135 dB), SB = $0.5469 \times f_s$. Each frequency response refers to that of 1 kHz.

Note 53. The bandwidth of the stopband attenuation value is from stopband to f_s (system sampling rate).

Note 54. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within ± 1 [1/ f_s].

■ DAC Short Delay Slow Roll-Off Filter (fs = 44.1 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 44.1 kHz;
DASD bit = "1", DASL bit = "1")

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|-------------------------------|------|--------|------------|-------------|
| DAC Digital Filter (LPF): | | | | | |
| Passband (Note 55) | -0.07 to +0.025 dB -3.0 dB | PB | 0 - | - 18.72 | 8.83 kHz |
| Stopband (Note 55) | | SB | 39.5 | - | kHz |
| Passband Ripple | | PR | -0.07 | - | +0.025 dB |
| Stopband Attenuation (Note 56) | | SA | 75.1 | - | dB |
| Group Delay (Note 57) | | GD | - | 4.7 | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode : | | | | | |
| Frequency Response: 0 to 20.0 kHz | | FR | -4.16 | - | +0.05 dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode : | | | | | |
| Frequency Response: 0 to 20.0 kHz | | FR | -4.66 | - | +0.03 dB |

Note 55. The passband and stopband frequencies scale with fs (system sampling rate).

PB = $0.2002 \times fs$ (@ -0.07/+0.025 dB), SB = $0.8957 \times fs$. Each frequency response refers to that of 1 kHz.

Note 56. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 57. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Slow Roll-Off Filter (fs = 96 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 96 kHz;
DASD bit = "1", DASL bit = "1")

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|-------------------------------|------|--------|------------|--------------|
| DAC Digital Filter (LPF): | | | | | |
| Passband (Note 58) | -0.07 to +0.027 dB -3.0 dB | PB | 0 - | - 40.78 | 19.29 kHz |
| Stopband (Note 58) | | SB | 86 | - | kHz |
| Passband Ripple | | PR | -0.07 | - | +0.027 dB |
| Stopband Attenuation (Note 59) | | SA | 75.1 | - | dB |
| Group Delay (Note 60) | | GD | - | 4.7 | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode : | | | | | |
| Frequency Response: 0 to 40.0 kHz | | FR | -3.80 | - | +0.10 dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode : | | | | | |
| Frequency Response: 0 to 40.0 kHz | | FR | -5.26 | - | +0.10 dB |

Note 58. The passband and stopband frequencies scale with fs (system sampling rate).

PB = $0.2009 \times fs$ (@ -0.07/+0.027 dB), SB = $0.8958 \times fs$. Each frequency response refers to that of 1 kHz.

Note 59. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 60. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Slow Roll-Off Filter (fs = 192 kHz)

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 192 kHz;
DASD bit = "1", DASL bit = "1")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|--------------------|--------|-------|-------|--------|------|
| DAC Digital Filter (LPF): | | | | | | |
| Passband (Note 61) | -0.07 to +0.027 dB | PB | 0 | - | 38.63 | kHz |
| | -3.0 dB | | - | 81.57 | - | kHz |
| Stopband (Note 61) | | SB | 172 | - | - | kHz |
| Passband Ripple | | PR | -0.07 | - | +0.027 | dB |
| Stopband Attenuation (Note 62) | | SA | 75.1 | - | - | dB |
| Group Delay (Note 63) | | GD | - | 4.7 | - | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode: | | | | | | |
| Frequency Response: 0 to 80.0 kHz | | FR | -5.90 | - | +0.35 | dB |
| DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode: | | | | | | |
| Frequency Response: 0 to 80.0 kHz | | FR | -9.38 | - | +0.35 | dB |

Note 61. The passband and stopband frequencies scale with fs (system sampling rate).

PB = $0.2012 \times fs$ (@ -0.07/+0.027 dB), SB = $0.8958 \times fs$. Each frequency response refers to that of 1 kHz.

Note 62. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 63. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

DC Characteristics

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|--------|-----------|------|----------|------|
| I/O Pins (Note 64) | | | | | |
| High-Level Input Voltage Except for XTI pin | VIH | 70 %TVDD | - | - | V |
| XTI pin | VIH | 70 %AVDD | - | - | V |
| Low-Level Input Voltage Except for XTI pin | VIL | - | - | 30 %TVDD | V |
| XTI pin | VIL | - | - | 30 %AVDD | V |
| High-Level Output Voltage (Iout = -200 μA) | VOH | TVDD -0.2 | - | - | V |
| Low-Level Output Voltage Except for SDA, XTO pin, Iout = 200 μA | VOL | - | - | 0.2 | V |
| SDA pin | VOL | - | - | 0.4 | V |
| 2 V < TVDD ≤ 3.6 V (Iout = 3 mA) | VOL | - | - | 0.4 | V |
| 1.65 V ≤ TVDD ≤ 2 V (Iout = 2 mA) | VOL | - | - | 20 %TVDD | V |
| Input Leakage Current | Iin | -5 | - | +5 | μA |

Note 64. MCKI, BCLK, LRCK, SDATA, SCL, SDA, PDN, TESTI1, TESTO, TESTI2 pins

■ Switching Characteristics

(Ta = -40 to 85 °C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; CL = 80 pF; unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------------------|---------|------------|----------|-----------------|------|
| MCKI | | | | | |
| Input Frequency | fMCK | 0.256 | - | 28.8 | MHz |
| Pulse Width Low | tMCKL | 0.4 / fMCK | - | - | ns |
| Pulse Width High | tMCKH | 0.4 / fMCK | - | - | ns |
| X'tal Oscillator (XTI pin) | | | | | |
| Input Frequency | fMCK | 11.2896 | - | 24.576 | MHz |
| Audio Interface Timing | | | | | |
| Master Mode | | | | | |
| LRCK Output Timing | | | | | |
| Frequency (Note 65) | fs | 8 | - | 192 | kHz |
| Duty | LRDuty | - | 50 | - | % |
| BCLK Output Timing | | | | | |
| Period (BCKO bit = "0") | tBCK | - | 1/(64fs) | - | ns |
| (BCKO bit = "1") | tBCK | - | 1/(32fs) | - | ns |
| Duty | BCKDuty | - | 50 | - | % |
| BCLK "↓" to LRCK Edge | tBLR | -20 | - | 20 | ns |
| SDATA Setup Time | tBDS | 10 | - | - | ns |
| SDATA Hold Time | tBDH | 10 | - | - | ns |
| Slave Mode | | | | | |
| LRCK Input Timing | | | | | |
| Frequency | fs | 8 | - | 384 | kHz |
| Duty | LRDuty | 45 | 50 | 55 | % |
| BCLK Input Timing | | | | | |
| Period (Note 66) | tBCK | 0.256 | - | 24.576 or 512fs | MHz |
| Pulse Width Low | tBCKL | 0.4 x tBCK | - | - | ns |
| Pulse Width High | tBCKH | 0.4 x tBCK | - | - | ns |
| BCLK "↑" to LRCK Edge | tBLR | 16 | - | - | ns |
| LRCK Edge to BCLK "↑" | tLRB | 16 | - | - | ns |
| SDATA Setup Time | tBDS | 10 | - | - | ns |
| SDATA Hold Time | tBDH | 10 | - | - | ns |

Note 65. Supported sampling rates are 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 176.4 k and 192 kHz.

Note 66. The maximum value is shorter period between "24.576 MHz" and "512fs".

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|---------|------|------|------|------|
| Control Interface Timing (I²C Bus mode): (Note 67) | | | | | |
| SCL Clock Frequency | fSCL | - | - | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | - | - | μs |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 0.6 | - | - | μs |
| Clock Low Time | tLOW | 1.3 | - | - | μs |
| Clock High Time | tHIGH | 0.6 | - | - | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | - | - | μs |
| SDA Hold Time from SCL Falling (Note 68) | tHD:DAT | 0 | - | - | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | - | - | μs |
| Rise Time of Both SDA and SCL Lines | tR | - | - | 0.3 | μs |
| Fall Time of Both SDA and SCL Lines | tF | - | - | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | - | - | μs |
| Capacitive Load on Bus | Cb | - | - | 400 | pF |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | - | 50 | ns |
| Power-down & Reset Timing | | | | | |
| PDN accept pulse width (Note 69) | tPDN | 1 | - | - | ms |
| PDN Reject Pulse Width (Note 69) | tRPD | - | - | 50 | ns |

Note 67. I²C-bus is a registered trademark of NXP B.V.

Note 68. Data must be held long enough to bridge the 300 ns-transition time of SCL.

Note 69. The AK4377A will be reset by the PDN pin = "L" for tPDN (Min.). The PDN pin must held "L" for longer period than or equal to tPDN (Min.). The AK4377A will not be reset by the "L" pulse shorter than or equal to tRPD (Max.).

■ Timing Diagram (System Clock)

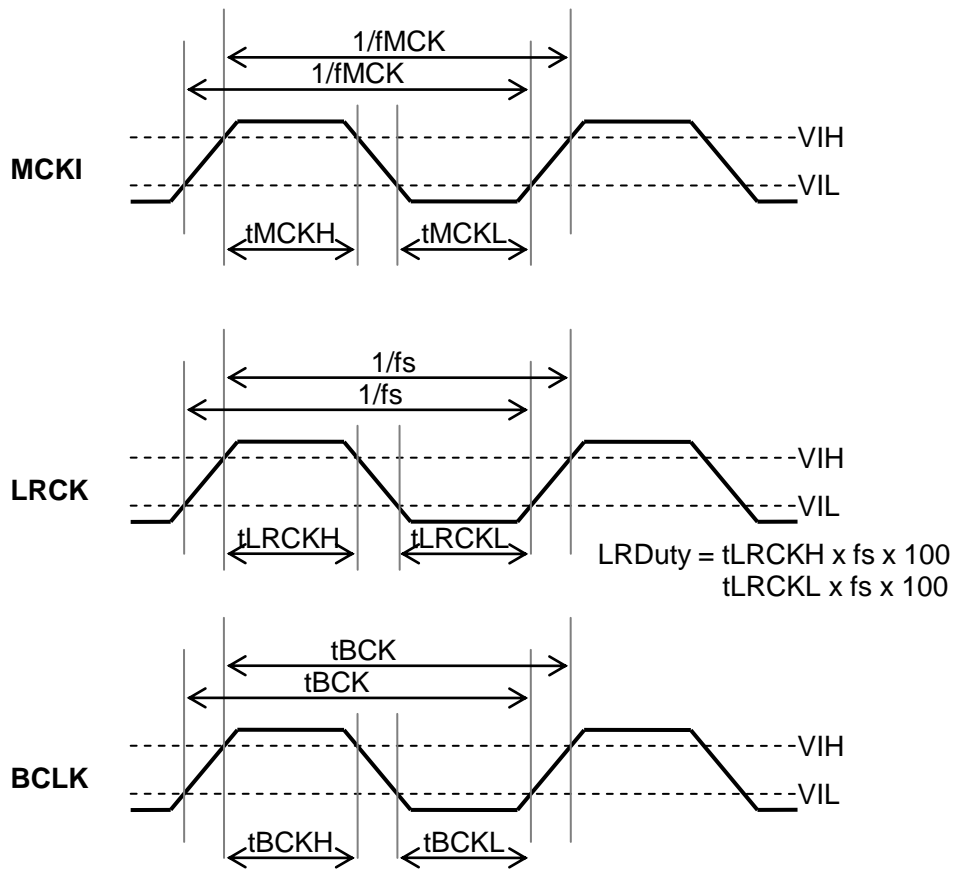


Figure 2. System Clock (Slave Mode)

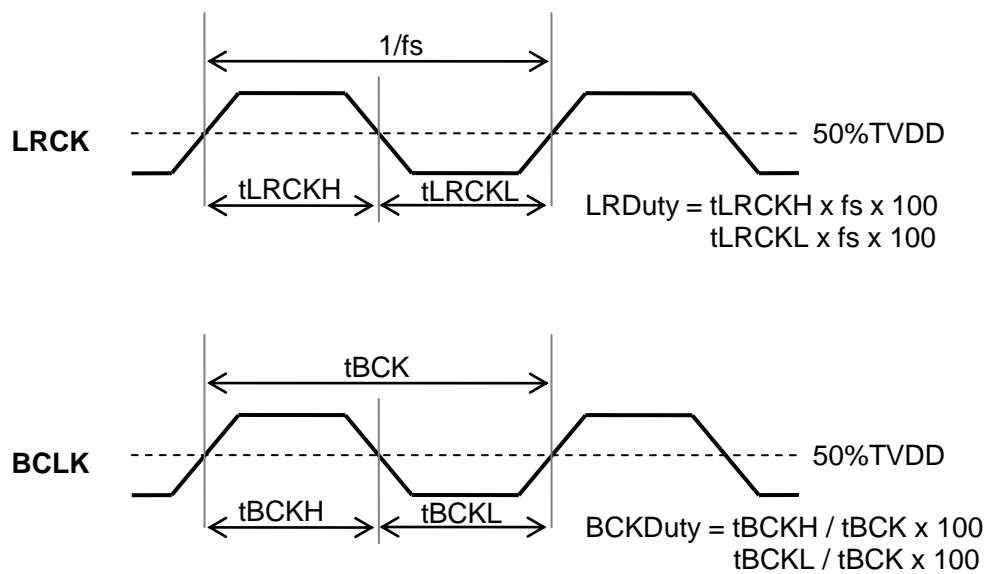


Figure 3. System Clock (Master Mode)

■ Timing Diagram (Serial Audio I/F)

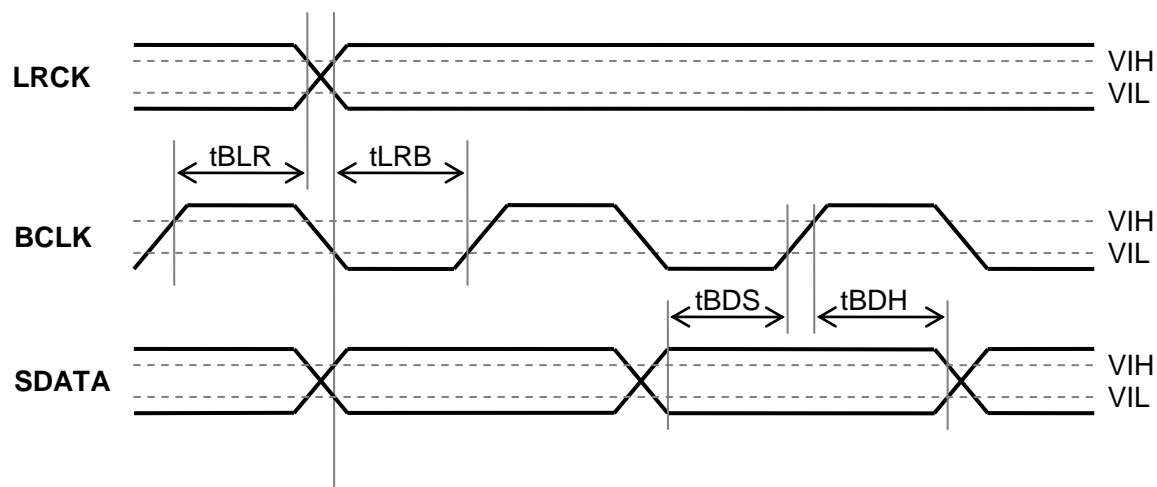


Figure 4. Serial Data Interface (Slave Mode)

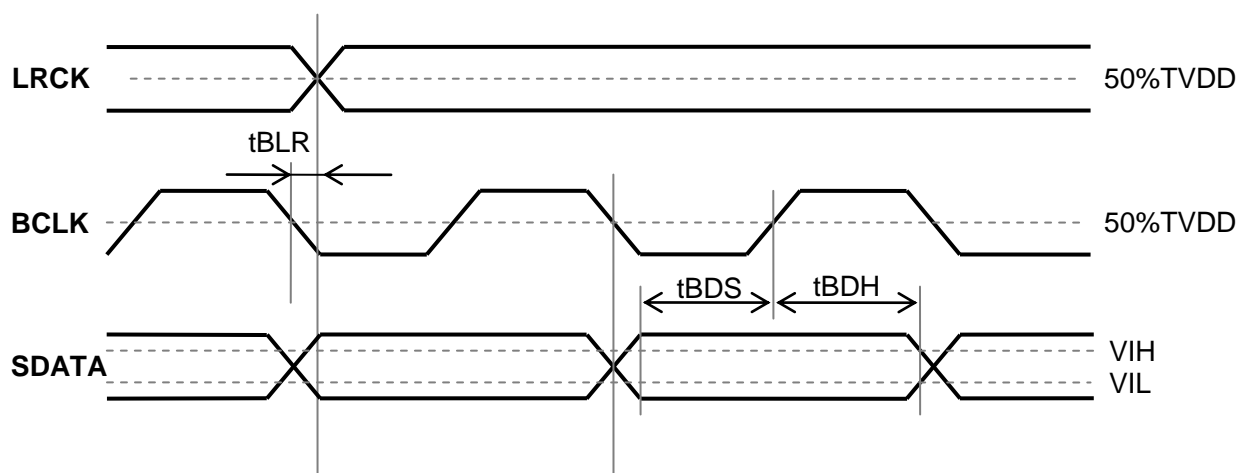


Figure 5. Serial Data Interface (Master Mode)

■ Timing Diagram (I²C Interface)

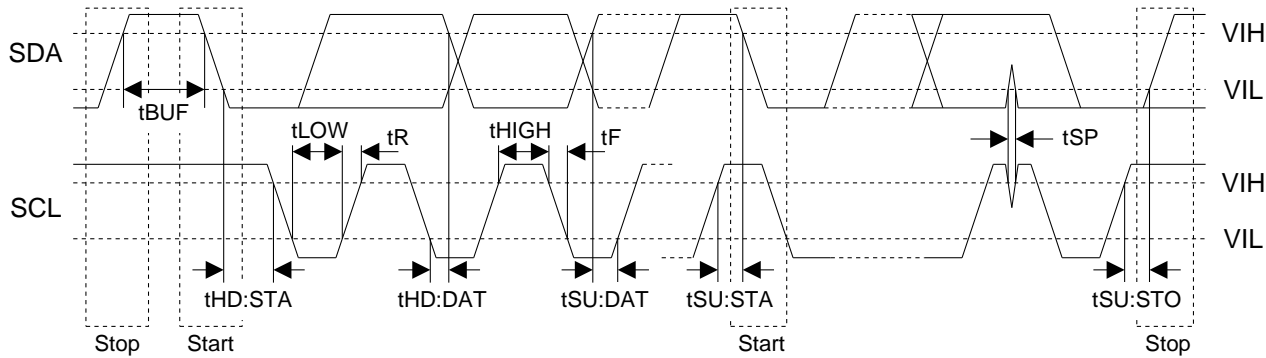


Figure 6. I²C Bus Mode Timing

■ Timing Diagram (Reset)

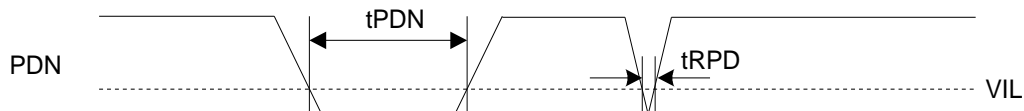


Figure 7. Power Down and Standby

9. Functional Description

■ System Clock

The AK4377A is operated by a clock generated by PLL or an externally input clock or X'tal oscillator (XTI pin). DACCKS[1:0] bits select the clock source of the DAC (Table 1). PLL clock source is selected from external MCKI, BCLK or the clock by X'tal oscillator (Table 7). Master clock frequency and sampling frequency are set by CM[1:0] bits and FS[4:0] bits, respectively. PMDA, PMHPL and PMHPR bits must be set to "0" when changing these frequencies.

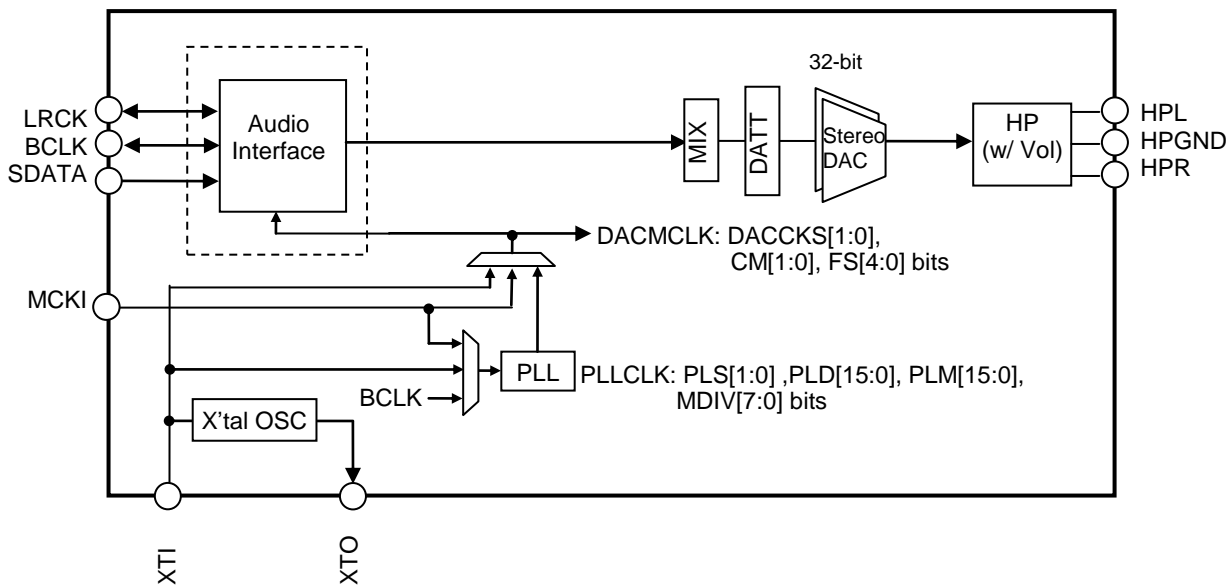


Figure 8. Clock & Data Flow

Table 1. DAC Master Clock Setting (x: Do not care)

| DACCKS[1:0] bits | DAC Master Clock | (default) |
|------------------|--------------------|-----------|
| 00 | MCKI pin | |
| 01 | PLLCLK | |
| 1x | X'tal (or XTI pin) | |

The AK4377A can be operated in both master and slave modes. Clock mode of LRCK pin and BCLK pin can be selected by MS bit. When using master mode, the LRCK pin and the BCLK pin should be pulled down or pulled up with an external resistor (about 100 kΩ) because both pins are floating state until MS bit becomes "1".

Table 2. Master/Slave Mode Select

| MS bit | LRCK pin, BCLK pin | (default) |
|--------|--------------------|-----------|
| 0 | Slave Mode | |
| 1 | Master Mode | |

Master/slave mode switching is not allowed while the AK4377A is in normal operation. The DAC and Headphone-Amp must be powered down before master/slave mode is switched. Furthermore PLL and Charge Pump must also be powered down in case that sampling frequency is changed or PLLCLK is stopped.

<MS bit Setting Sequence Example>

- 1.DAC, Headphone-Amp (PLL, Charge Pump) Power-down
- 2.Clock Mode of ACPU Setting (In case clock mode of ACPU is master, switch to slave.)
- 3.MS bit Selection
- 4.Clock Mode of ACPU Setting (In case clock mode of ACPU is slave, switch to master.)
- 5.DAC, Headphone-Amp (PLL, Charge Pump) Power-up

Figure 9 shows clock & data flow in slave mode. Figure 10 shows clock & data flow in master mode.

<Slave Mode>

MS bit = "0", PMPLL bit = "0", DACCKS[1:0] bits = "00"

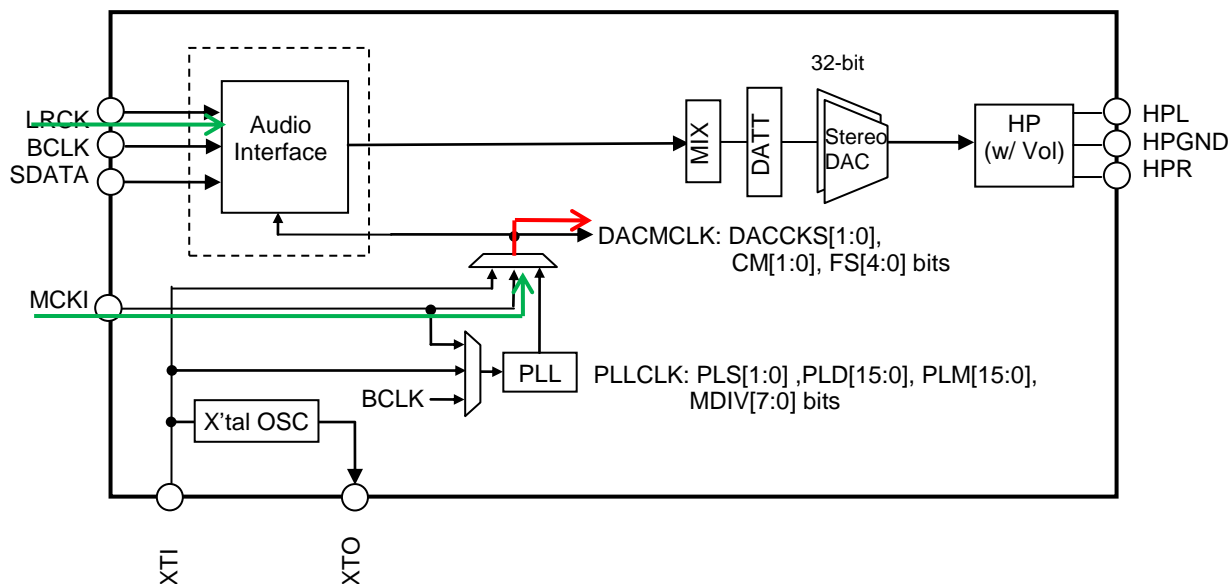


Figure 9. Example of Clock and Data Flow (Slave Mode, Not using PLL)

<Master Mode>

MS bit = "1", PMPLL bit = "1", PLS[1:0] bits = "00", DACCKS[1:0] bits = "01"

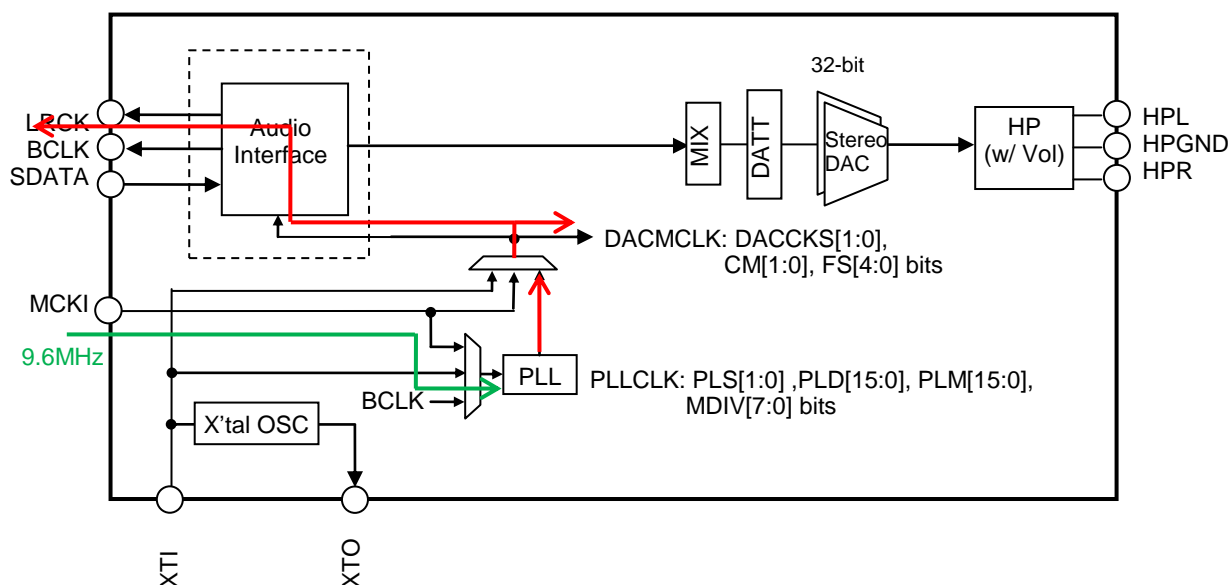


Figure 10. Example of Clock and Data Flow (Master Mode, Using PLL)

<High Performance Mode: LPMODE bit = "0">

Table 3. Setting of Master Clock Frequency (High Performance Mode)

| DSMLP bit | CM1 bit | CM0 bit | Master Clock Frequency | Sampling Frequency Range | (default) |
|-----------|---------|---------|------------------------|--------------------------|-----------|
| 1 | 0 | 0 | 256fs | 8 to 12 kHz | |
| 0 | 0 | 0 | 256fs | 16 to 96 kHz | |
| | | | 32fs | 256 to 384 kHz | |
| 0 | 0 | 1 | 512fs | 8 to 48 kHz | |
| | | | 64fs | 256 to 384 kHz | |
| 0 | 1 | 0 | 1024fs | 8 to 24 kHz | |
| 0 | 1 | 1 | 128fs | 128 to 192 kHz | |

<Low Power Mode: LPMODE bit = "1">

Table 4. Setting of Master Clock Frequency (Low Power Mode)

| DSMLP bit | CM1 bit | CM0 bit | Master Clock Frequency | Sampling Frequency Range | (default) |
|-----------|---------|---------|------------------------|--------------------------|-----------|
| 1 | 0 | 0 | 256fs | 8 to 96 kHz | |
| 1 | 0 | 1 | 512fs | 8 to 48 kHz | |
| 1 | 1 | 0 | 1024fs | 8 to 24 kHz | |
| 1 | 1 | 1 | 128fs | 128 to 192 kHz | |

Note 70. The AK4377A does not support Oct speed mode (fs = 256 to 384 kHz) in low power mode.

Table 5. Setting of Sampling Frequency (N/A: Not available)

| FS4 bit | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency | (default) |
|---------|---------|---------|---------|---------|--------------------|-----------|
| 0 | 0 | 0 | 0 | 0 | 8 kHz | |
| 0 | 0 | 0 | 0 | 1 | 11.025 kHz | |
| 0 | 0 | 0 | 1 | 0 | 12 kHz | |
| 0 | 0 | 1 | 0 | 0 | 16 kHz | |
| 0 | 0 | 1 | 0 | 1 | 22.05 kHz | |
| 0 | 0 | 1 | 1 | 0 | 24 kHz | |
| 0 | 1 | 0 | 0 | 0 | 32 kHz | |
| 0 | 1 | 0 | 0 | 1 | 44.1 kHz | |
| 0 | 1 | 0 | 1 | 0 | 48 kHz | |
| 0 | 1 | 1 | 0 | 0 | 64 kHz | |
| 0 | 1 | 1 | 0 | 1 | 88.2 kHz | |
| 0 | 1 | 1 | 1 | 0 | 96 kHz | |
| 1 | 0 | 0 | 0 | 0 | 128 kHz | |
| 1 | 0 | 0 | 0 | 1 | 176.4 kHz | |
| 1 | 0 | 0 | 1 | 0 | 192 kHz | |
| 1 | 0 | 1 | 0 | 0 | 256 kHz | |
| 1 | 0 | 1 | 0 | 1 | 352.8 kHz | |
| 1 | 0 | 1 | 1 | 0 | 384 kHz | |
| Others | | | | | N/A | |

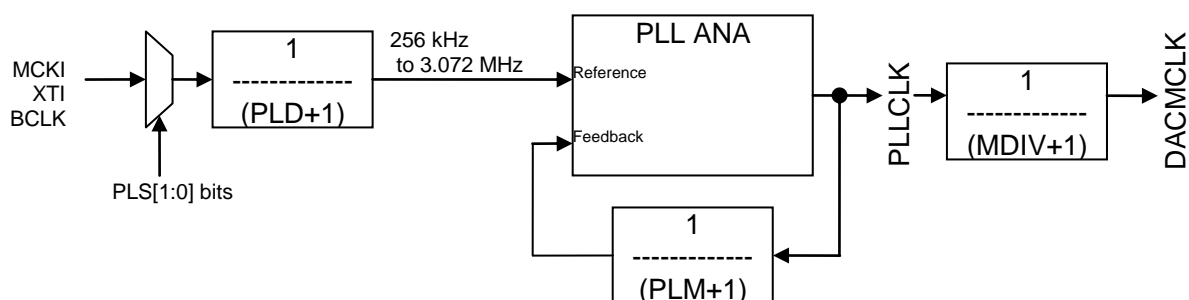
* Depending on the PLL divider setting, the sampling frequency may differ.
Please set PLD[15:0] and PLM[15:0] bits precisely.

■ PLL

The PLL generates a PLLCLK which is used as the DAC operation clock DACMCLK. The output frequency should be set in the range from 101.6064 to 122.88 MHz (Table 6 shows setting example of 48 kHz and 44.1 kHz base rates). Refer to Table 11 to Table 12 for frequency setting examples. Reference clock of PLL should be set in the range from 256 kHz to 3.072 MHz.

Table 6. PLLCLK Setting Example

| | 48 kHz base rate | 44.1 kHz base rate |
|---------|------------------|--------------------|
| 2560/fs | 122.88 MHz | 112.896 MHz |
| 2304/fs | 110.592 MHz | 101.6064 MHz |



Reference clock = PLL Source / (PLD + 1)

PLLCLK = Reference clock x (PLM + 1)

DACMCLK = PLLCLK / (MDIV + 1)

Figure 11. PLL Block Diagram

■ Input Clock Select Function

The PLL has a function that selects the input clock. The clock source pin is selected by PLS[1:0] bits.

Table 7. PLL Clock Select (x: Do not care)

| PLS[1:0] bits | Clock Source | |
|---------------|-----------------|-----------|
| 00 | MCKI pin | (default) |
| 01 | BCLK pin | |
| 1x | X'tal (XTI pin) | |

1. PLL Reference Clock Divider

The PLL can set the dividing number of the reference clock in 16-bit. The input clock is used as PLL reference clock by dividing by (PLD+1).

Table 8. PLL Reference Clock Divider

| PLD[15:0] bits | Dividing Number | |
|----------------|-----------------|-----------|
| 0000H | 1 | (default) |
| 0001H to FFFFH | 1 / (PLD + 1) | |

Note 71. The reference clock divided by PLD should be set in the range from 256 kHz to 3.072 MHz.

2. PLL Feedback Clock Divider

The dividing number of feedback clock can be set freely in 16-bit. PLLCLK is divided by (PLM + 1) and used as PLL feedback clock. The feedback clock is fixed to “L” without dividing when PLM[15:0] bits = 0000H.

Table 9. PLL Feedback Clock Divider

| PLM[15:0] bits | Dividing Number | (default) |
|----------------|------------------------|-----------|
| 0000H | Clock Stop | |
| 0001H to FFFFH | $1 / (\text{PLM} + 1)$ | |

3. Power Management (PMPLL)

PLL can be powered down by a control register setting.

Table 10. PLL Power Control

| PMPLL bit | PLL Status | (default) |
|-----------|------------|-----------|
| 0 | Power-Down | |
| 1 | Power-Up | |

4. Frequency Setting Examples

Table 11. PLL Frequency Setting Example (PLL reference source: MCKI)

| CLKIN | | PLL condition | | | PLLCLK | | |
|--------|-------------------|---------------|----------------|-----|-------------------|-------|-------------|
| Source | Frequency [Hz] | D+1 | REFCLK [Hz] | M+1 | Base Rate [Hz] | | |
| | | | | | | [fs] | [Hz] |
| MCKI | 9,600,000 | 5 | 1,920,000 | 64 | 48,000 | 2,560 | 122,880,000 |
| | 19,200,000 | 10 | 1,920,000 | 64 | | 2,560 | 122,880,000 |
| | 12,288,000 | 4 | 3,072,000 | 40 | | 2,560 | 122,880,000 |
| | 24,576,000 | 8 | 3,072,000 | 40 | | 2,560 | 122,880,000 |
| | 12,000,000 | 25 | 480,000 | 256 | | 2,560 | 122,880,000 |
| | 24,000,000 | 25 | 960,000 | 128 | | 2,560 | 122,880,000 |
| | 9,600,000 | 25 | 384,000 | 294 | 44,100 | 2,560 | 112,896,000 |
| | 19,200,000 | 25 | 768,000 | 147 | | 2,560 | 112,896,000 |
| | 11,289,600 | 4 | 2,822,400 | 40 | | 2,560 | 112,896,000 |
| | 22,579,200 | 8 | 2,822,400 | 40 | | 2,560 | 112,896,000 |

Table 12. PLL Frequency Setting Example (PLL reference source: BCLK)

| CLKIN | | | PLL condition | | | PLLCLK | | |
|----------------|---------------------------|-------------------|---------------|----------------|-----|-------------------|-------|-------------|
| Source | Sampling Frequency[Hz] | Frequency [Hz] | D+1 | REFCLK [Hz] | M+1 | Base Rate [Hz] | | |
| | | | | | | | [fs] | [Hz] |
| BCLK (32fs) | 8,000 | 256,000 | 1 | 256,000 | 480 | 48,000 | 2,560 | 122,880,000 |
| | 11,025 | 352,800 | 1 | 352,800 | 320 | 44,100 | 2,560 | 112,896,000 |
| | 16,000 | 512,000 | 1 | 512,000 | 240 | 48,000 | 2,560 | 122,880,000 |
| | 22,050 | 705,600 | 1 | 705,600 | 160 | 44,100 | 2,560 | 112,896,000 |
| | 24,000 | 768,000 | 1 | 768,000 | 160 | 48,000 | 2,560 | 122,880,000 |
| | 32,000 | 1,024,000 | 1 | 1,024,000 | 120 | 48,000 | 2,560 | 122,880,000 |
| | 44,100 | 1,411,200 | 1 | 1,411,200 | 80 | 44,100 | 2,560 | 112,896,000 |
| | 48,000 | 1,536,000 | 1 | 1,536,000 | 80 | 48,000 | 2,560 | 122,880,000 |
| BCLK (48fs) | 8,000 | 384,000 | 1 | 384,000 | 320 | 48,000 | 2,560 | 122,880,000 |
| | 11,025 | 529,200 | 1 | 529,200 | 192 | 44,100 | 2,304 | 101,606,400 |
| | 16,000 | 768,000 | 1 | 768,000 | 160 | 48,000 | 2,560 | 122,880,000 |
| | 22,050 | 1,058,400 | 3 | 352,800 | 320 | 44,100 | 2,560 | 112,896,000 |
| | 24,000 | 1,152,000 | 3 | 384,000 | 320 | 48,000 | 2,560 | 122,880,000 |
| | 32,000 | 1,536,000 | 1 | 1,536,000 | 80 | 48,000 | 2,560 | 122,880,000 |
| | 44,100 | 2,116,800 | 3 | 705,600 | 160 | 44,100 | 2,560 | 112,896,000 |
| | 48,000 | 2,304,000 | 3 | 768,000 | 160 | 48,000 | 2,560 | 122,880,000 |
| BCLK (64fs) | 8,000 | 512,000 | 1 | 512,000 | 240 | 48,000 | 2,560 | 122,880,000 |
| | 11,025 | 705,600 | 1 | 705,600 | 160 | 44,100 | 2,560 | 112,896,000 |
| | 16,000 | 1,024,000 | 1 | 1,024,000 | 120 | 48,000 | 2,560 | 122,880,000 |
| | 22,050 | 1,411,200 | 1 | 1,411,200 | 80 | 44,100 | 2,560 | 112,896,000 |
| | 24,000 | 1,536,000 | 1 | 1,536,000 | 80 | 48,000 | 2,560 | 122,880,000 |
| | 32,000 | 2,048,000 | 1 | 2,048,000 | 60 | 48,000 | 2,560 | 122,880,000 |
| | 44,100 | 2,822,400 | 1 | 2,822,400 | 40 | 44,100 | 2,560 | 112,896,000 |
| | 48,000 | 3,072,000 | 1 | 3,072,000 | 40 | 48,000 | 2,560 | 122,880,000 |

■ DACMCLK Generating Divider Setting

MDIV[7:0] bits control DACMCLK divider.

Table 13. DACMCLK Divider Setting

| MDIV[7:0] bits | Dividing Number | (default) |
|----------------|-------------------------|-----------|
| 00H | 1 | |
| 01H to FFH | $1 / (\text{MDIV} + 1)$ | |

■ Crystal Oscillator

The clock for the XTI pin can be generated by two methods. PMOSC bit must be set to “1” when using a crystal oscillator.

1) X'tal Mode (PMOSC bit = “1”)

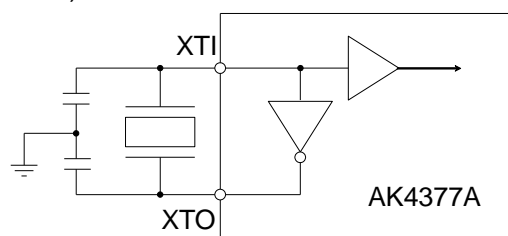


Figure 12. X'tal Mode

Note 72. The capacitor value is dependent on the crystal oscillator.

$C_L = 21.5 \text{ pF}$ (Max.), R_L (Equivalent Series Resistance) = 80Ω (Max.) @ 24.576 MHz

$C_L = 30.6 \text{ pF}$ (Max.), R_L (Equivalent Series Resistance) = 200Ω (Max.) @ 11.2896 MHz

2) External Clock Mode (PMOSC bit = “0”)

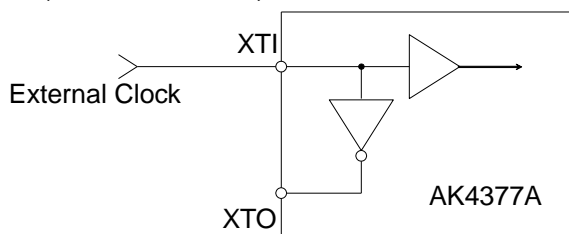


Figure 13. External Clock Mode

Note 73. Do not input a clock more than AVDD.

3) OFF Mode (Not Using XTI/XTO pins (PMOSC bit = “0”))

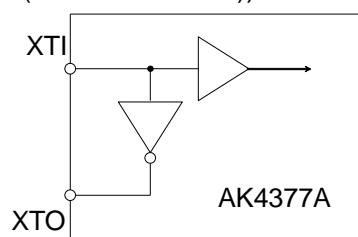


Figure 14. OFF Mode

■ DAC Digital Filter

The AK4377A has four types of digital filter. The filter mode of DAC can be selected by DASD and DASL bits. The default setting is DASL bit = DASD bit = "0" (Sharp Roll-Off Filter).

Table 14. DAC Digital Filter Setting

| DASD bit | DASL bit | DAC Filter Mode Setting | (default) |
|----------|----------|-----------------------------------|-----------|
| 0 | 0 | Sharp Roll-Off Filter | |
| 0 | 1 | Slow Roll-Off Filter | |
| 1 | 0 | Short Delay Sharp Roll-Off Filter | |
| 1 | 1 | Short Delay Slow Roll-Off Filter | |

■ Digital Mixing

The AK4377A has digital mixing circuits for each Lch and Rch. They can mix the data digitally and convert the polarity. The inverted data by this polarity conversion is calculated in 2's complement format.

Table 15. DAC L/Rch Input Signal Select

| MDACL bit MDACR bit | RDACL bit RDACR bit | LDACL bit LDACR bit | DAC Lch Input Data DAC Rch Input Data | (default) |
|------------------------|------------------------|------------------------|--|-----------|
| 0 | 0 | 0 | MUTE | |
| 0 | 0 | 1 | Lch | |
| 0 | 1 | 0 | Rch | |
| 0 | 1 | 1 | Lch + Rch | |
| 1 | 0 | 0 | MUTE | |
| 1 | 0 | 1 | Lch/2 | |
| 1 | 1 | 0 | Rch/2 | |
| 1 | 1 | 1 | (Lch + Rch)/2 | |

Table 16. DAC L/Rch Input Signal Polarity Select

| INVL bit INVR bit | Output Data | (default) |
|----------------------|-------------|-----------|
| 0 | Normal | |
| 1 | Inverting | |

■ Digital Volume

The AK4377A has a 32-level digital volume in front of DAC for each L and R channel. The volume is changed from +3 dB to −12 dB in 0.5 dB step including Mute. The volume change is executed immediately by setting registers.

When OVOLCN bit is “1”, the OVL[4:0] bits control Lch level and OVR[4:0] bits control Rch level. When OVOLCN bit = “0”, the OVL[4:0] bits control both Lch and Rch attenuation levels. In this case, the setting of OVR[4:0] bits is ignored.

When Oct Speed Mode ($f_s = 256$ to 384 kHz), Digital Volume cannot be used.

Table 17. Digital Volume Setting

| OVL[4:0] bits OVR[4:0] bits | Volume (dB) | |
|--------------------------------|-------------|-----------|
| 1FH | +3 | |
| 1EH | +2.5 | |
| 1DH | +2 | |
| 1CH | +1.5 | |
| 1BH | +1 | |
| 1AH | +0.5 | |
| 19H | 0 | (default) |
| 18H | −0.5 | |
| 17H | −1 | |
| 16H | −1.5 | |
| 15H | −2 | |
| 14H | −2.5 | |
| 13H | −3 | |
| 12H | −3.5 | |
| 11H | −4 | |
| 10H | −4.5 | |
| 0FH | −5 | |
| 0EH | −5.5 | |
| 0DH | −6 | |
| 0CH | −6.5 | |
| 0BH | −7 | |
| 0AH | −7.5 | |
| 09H | −8 | |
| 08H | −8.5 | |
| 07H | −9 | |
| 06H | −9.5 | |
| 05H | −10 | |
| 04H | −10.5 | |
| 03H | −11 | |
| 02H | −11.5 | |
| 01H | −12 | |
| 00H | MUTE | |

■ Headphone Amplifier Output (HPL/HPR pins)

Headphone amplifiers are operated by positive and negative power that is supplied from internal charge pump circuit. The VEE2 pin output the negative voltage generated by the internal charge pump circuit from CVDD. This charge pump circuit is switched between VDD mode and 1/2VDD mode by the output level of the headphone amplifiers. The headphone amplifier output is single-ended and centered on HPGND (0 V). A capacitor for AC coupling is not necessary. The load resistance is 14.4Ω (Min.). The output power is 10 mW when 0 dBFS, $R_L = 32\ \Omega$, $AVDD = CVDD = 1.8\ V$ and $HPG = -4\ dB$, and it is 25 mW when 0 dBFS, $R_L = 32\ \Omega$, $AVDD = 1.8\ V$ and $HPG = 0\ dB$. Ground loop noise cancelling function for headphone amplifier is available by connecting the HPGND pin to the ground of the jack.

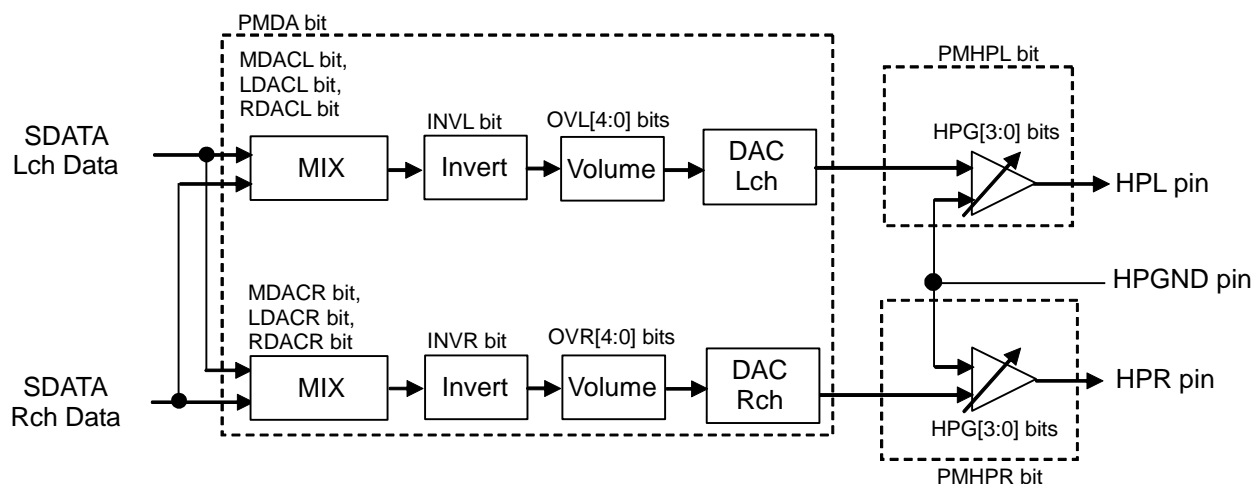


Figure 15. DAC & Headphone-Amp Block Diagram

Table 18. Charge Pump Mode Setting (N/A: Not available)

| CPMODE1 bit | CPMODE0 bit | Mode | Operation Voltage | |
|-------------|-------------|-------------------------------|---------------------|-----------|
| 0 | 0 | Class-G Operation Mode | Automatic Switching | (default) |
| 0 | 1 | $\pm VDD$ Operation Mode | $\pm VDD$ | |
| 1 | 0 | $\pm 1/2\ VDD$ Operation Mode | $\pm 1/2\ VDD$ | |
| 1 | 1 | N/A | N/A | |

• Class-G Mode Switching Level:

$VDD \rightarrow 1/2\ VDD$: $< 1.05\ mW$ at both channels (@ $CVDD = 1.8\ V$, $R_L = 32\ \Omega$)

$1/2\ VDD \rightarrow VDD$: $\geq 1.05\ mW$ at either channel (@ $CVDD = 1.8\ V$, $R_L = 32\ \Omega$)

When the charge pump operation mode is changed to VDD mode from 1/2 VDD mode, an internal counter for holding VDD mode starts (Table 19). The charge pump changes to 1/2 VDD mode if the output signal level is lower than the switching level and 1/2 VDD mode detection time that is set by LVDTM[2:0] bits is passed after VDD mode hold time is finished.

Table 19. VDD Mode Holding Period Setting (x: Do not care)

| VDDTM[3:0] bits | | VDD Mode Holding Period | | | | |
|-----------------|-----------|-------------------------|----------|-----------|-----------|-----------|
| | | 8 kHz | 44.1 kHz | 96 kHz | 192 kHz | |
| 0000 | 1024/fs | 128 ms | 23.2 ms | 10.7 ms | 5.3 ms | (default) |
| 0001 | 2048/fs | 256 ms | 46.4 ms | 21.3 ms | 10.7 ms | |
| 0010 | 4096/fs | 512 ms | 92.9 ms | 42.7 ms | 21.3 ms | |
| 0011 | 8192/fs | 1024 ms | 186 ms | 85.3 ms | 42.7 ms | |
| 0100 | 16384/fs | 2048 ms | 372 ms | 170.7 ms | 85.3 ms | |
| 0101 | 32768/fs | 4096 ms | 743 ms | 341.3 ms | 170.7 ms | |
| 0110 | 65536/fs | 8192 ms | 1486 ms | 682.7 ms | 341.3 ms | |
| 0111 | 131072/fs | 16384 ms | 2972 ms | 1365.3 ms | 682.7 ms | |
| 1xxx | 262144/fs | 32768 ms | 5944 ms | 2730.7 ms | 1365.3 ms | |

Note 74. Oct speed mode (fs = 256 k / 352.8 k / 384 kHz) has the same cycle as fs = 32 k / 44.1 k / 48 kHz.

When the output voltage becomes less than class-G mode switching level, the internal detection counter for 1/2 VDD mode which is set by LVDTM[2:0] bits starts. This counter is reset when the output voltage exceeds class-G mode switching level. The charge pump operation mode is changed to VDD from 1/2 VDD if the detection counter of 1/2VDD mode is finished and also the VDD mode hold period is passed.

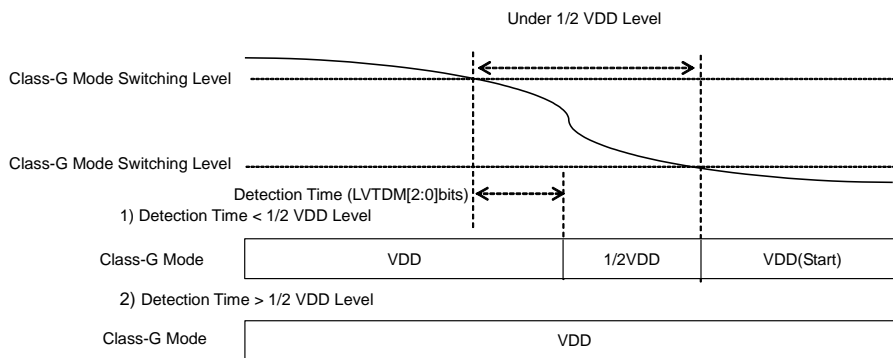


Figure 16. Transition to 1/2 VDD Mode from VDD Mode

Table 20. 1/2VDD Detection Period (Minimum frequency that is not detected)

| LVDTM[2:0] bits | | 1/2 VDD Mode Detection Time / Minimum Frequency That Is Not Detected | | | | |
|-----------------|---------|---|----------|----------|----------|-----------|
| | | 8 kHz | 44.1 kHz | 96 kHz | 192 kHz | |
| 000 | 64/fs | 8 ms | 1.5 ms | 0.67 ms | 0.33 ms | (default) |
| | | 62.5 Hz | 344.5 Hz | 750 Hz | 1500 Hz | |
| 001 | 128/fs | 16 ms | 2.9 ms | 1.3 ms | 0.67 ms | |
| | | 31.3 Hz | 172.3 Hz | 375 Hz | 750 Hz | |
| 010 | 256/fs | 32 ms | 5.8 ms | 2.7 ms | 1.3 ms | |
| | | 15.6 Hz | 86.1 Hz | 187.5 Hz | 375 Hz | |
| 011 | 512/fs | 64 ms | 11.6 ms | 5.3 ms | 2.7 ms | |
| | | 7.8 Hz | 43.1 Hz | 93.8 Hz | 187.5 Hz | |
| 100 | 1024/fs | 128 ms | 23.2 ms | 10.7 ms | 5.3 ms | |
| | | 3.9 Hz | 21.5 Hz | 46.9 Hz | 93.8 Hz | |
| 101 | 2048/fs | 256 ms | 46.4 ms | 21.3 ms | 10.7 ms | |
| | | 2.0 Hz | 10.8 Hz | 23.4 Hz | 46.9 Hz | |
| 110 | 4096/fs | 512 ms | 92.9 ms | 42.7 ms | 21.3 ms | |
| | | 1.0 Hz | 5.4 Hz | 11.7 Hz | 23.4 Hz | |
| 111 | 8192/fs | 1024 ms | 185.8 ms | 92.9 ms | 42.7 ms | |
| | | 0.5 Hz | 2.7 Hz | 5.9 Hz | 11.7 Hz | |

Note 75. Oct speed mode (fs = 256 k / 352.8 k / 384 kHz) has the same cycle as fs = 32 k / 44.1 k / 48 kHz.

The output level of the headphone amplifier is controlled by HPG[3:0] bits. The volume setting is common for both L and R channels and ranges from +6dB to –20 dB in 2 dB step (Table 21). The volume change is executed immediately by setting registers.

Table 21. Headphone Amplifier Volume Setting (N/A: Not available)

| HPG[3:0] bits | Volume (dB) | (default) |
|---------------|-------------|-----------|
| FH | N/A | |
| EH | +6 | (default) |
| DH | +4 | |
| CH | +2 | |
| BH | 0 | |
| AH | –2 | |
| 9H | –4 | |
| 8H | –6 | |
| 7H | –8 | |
| 6H | –10 | |
| 5H | –12 | |
| 4H | –14 | |
| 3H | –16 | |
| 2H | –18 | |
| 1H | –20 | |
| 0H | MUTE | |

< Headphone Amplifier External Circuit >

It is necessary to put an oscillation prevention circuit ($0.1\ \mu\text{F} \pm 20\%$ capacitor and $10\ \Omega \pm 20\%$ resistor) because there is a possibility that the headphone amplifier oscillates.

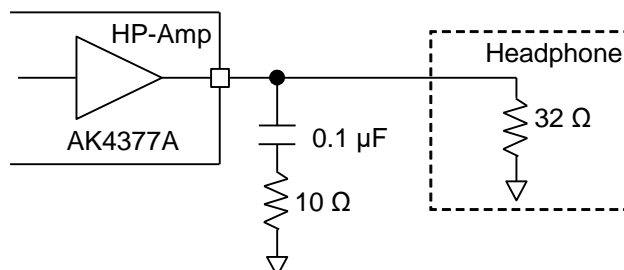


Figure 17. Headphone Amplifier Oscillation Prevention Circuit Example

< Power-Up/Down Sequence of Headphone Amplifier >

After releasing DAC power-down state by PMDA bit, the headphone amplifier should be powered up by PMHPL/R bits. A wait time from DAC power-up to headphone power-up is not necessary. PMDA bit releases a power-down of the digital block of the DAC, PMHPL bit or PMHPR bit powers up the analog block of the DAC and the headphone amplifier. Then, initialization cycle of the headphone amplifier is executed. The gain setting (HPG[3:0] bits) should be made before PMHPL bit or PMHPR bit is set to "1". Do not change the gain setting (HPG[3:0] bits) during the headphone initialization cycle. The gain setting can be changed after the headphone initialization cycle is finished. A wait time from the gain setting to PMHPL bit or PMHPR bit = "1" is not necessary.

When the AK4377A is powered down, the headphone amplifier should be powered down first. The DAC should be powered down next. A wait time from a headphone power-down to the DAC power-down is not necessary.

When the headphone amplifier is powered down, the HPL pin and the HPR pin are pulled down to HPGND via the internal pull-down register. The pull-down resistor is $6\ \Omega$ (Typ.) @ HPLHZ bit = HPRHZ bit = "0". When the headphone amplifier is powered down, the HPL pin and the HPR pin are pulled down by $200\ \text{k}\Omega$ (Typ.) by setting HPLHZ bit and HPRHZ bit to "1", respectively. These bits must be set to "0" before power up the headphone amplifier.

Table 22. Headphone Lch Output Status (N/A: Not available)

| PMHPL bit | HPLHZ bit | HP-Amp Status |
|-----------|-----------|---|
| 0 | 0 | Pull-Down by $6\ \Omega$ (Typ.) |
| 0 | 1 | Pull-Down by $200\ \text{k}\Omega$ (Typ.) |
| 1 | 0 | Normal Operation |
| 1 | 1 | N/A |

Table 23. Headphone Rch Output Status (N/A: Not available)

| PMHPR bit | HPRHZ bit | HP-Amp Status |
|-----------|-----------|---|
| 0 | 0 | Pull-Down by $6\ \Omega$ (Typ.) |
| 0 | 1 | Pull-Down by $200\ \text{k}\Omega$ (Typ.) |
| 1 | 0 | Normal Operation |
| 1 | 1 | N/A |

When the HPL pin and the HPR pin are connected to analog signal pins of an external device by Wire-OR, CP1, CP2, LDO1P and LDO1N should be powered up. Do not input a negative voltage to the HPL and the HPR pins when CP1, CP2, LDO1P and LDO1N are powered down.

If the pop noise at power-down exceeds an acceptable range, headphone amplifier should be powered down after attenuating the headphone volume gradually until mute.

The power-up time of headphone amplifier is shown in [Table 24](#). The HPL pin and the HPR pin output 0 V (HPGND) when the headphone amplifier is powered up. The power-down is executed immediately.

Table 24. Headphone Power Up Time

| Sampling Frequency [kHz] | Power-Up Time (Max.) |
|--|----------------------|
| 8/12/16/24/32/48/64/96/128/192/256/384 | 23.9 ms |
| 11.025/22.05/44.1/88.2/176.4/352.8 | 25.9 ms |

<Power-Up Sequence Example>

1. DAC Initial Settings (Write "70H" data into DAC Adjustment1 (Addr.26H),
Write "00H" data into DAC Adjustment2 (Addr.2AH)
Write "69H" data into DAC Adjustment3 (Addr.25H)) ([Note 76](#))
2. Audio I/F, DAC Clock, Sampling Frequency, Path, Digital Volume, Analog Volume Settings
3. CP1 Power-Up (PMCP1 bit: "0" → "1")
4. Wait 6.5 ms ([Note 77](#))
5. LDO1P & LDO1N Power-Up (PMLDO1P bit & PMLDO1N bit: "0" → "1")
6. Wait 1 ms ([Note 77](#))
7. DAC Power-Up (PMDA bit: "0" → "1")
8. CP2 Power-Up (PMCP2 bit: "0" → "1")
9. Wait 4.5 ms ([Note 77](#))
10. Headphone Amplifier Power-Up (PMHPL bit & PMHPR bit: "0" → "1")
11. Wait 25.9 ms (@ fs = 44.1 kHz)
12. Playback

<Power-Down Sequence Example>

1. Headphone Amplifier Power-Down (PMHPL bit & PMHPR bit: "1" → "0")
2. CP2 Power-Down (PMCP2 bit: "1" → "0")
3. DAC Power-Down (PMDA bit: "1" → "0")
4. LDO1P & LDO1N Power-Down (PMLDO1P bit & PMLDO1N bit: "1" → "0")
5. CP1 Power-Down (PMCP1 bit: "1" → "0")
6. Stop

Note 76. Recommended setting of DAC Adjustment2 (Addr.2AH) is "00H" data. However, T[15:12]bits setting should be changed appropriately since the optimum setting for T[15:12] bits varies depending on the PCB layout.

Note 77. Refer to "■ Charge Pump & LDO Circuit Power-up Time"

< Low Power Mode >

The DAC and the headphone amplifier will be in low power mode by setting LPMODE bit and DSMLP bit to “1”. PMHPL bit and PMHPR bit must be set to “0” when changing operation mode of the DAC and the headphone amplifier between low power mode and high performance mode. The AK4377A does not support Oct speed mode ($f_s = 256$ to 384 kHz) in low power mode.

Table 25. DAC, HP-Amp Mode Setting

| LPMODE bit | Mode | (default) |
|------------|-----------------------|-----------|
| 0 | High Performance Mode | |
| 1 | Low Power Mode | |

< Noise Gate >

When NGDIS bit = "0", a noise gate is enabled and noise level will be improved if both L and R channels input data of the DAC is continuously "0" for the period set by NGT and FS[4:0] bits. The noise gate will be disabled if one of these L channel and R channel input data of the DAC is not "0" even once and the AK4377A returns to normal operation from the state that Noise gate is enabled. The noise gate is always disable when NGDIS bit = "1" or when LPMODE bit = "1" (in low power mode). It is only available in high performance mode (LPMODE bit = "0"). PMDA bit, PMHPL bit and PMHPR bit must be set to "0" when changing NGT bit.

Table 26. Noise Gate Zero Detection Period (N/A: Not available)

| NGT bit | FS4 bit | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency (fs) | Zero Detection Time | |
|---------|---------|---------|---------|---------|---------|-------------------------|---------------------|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 8 kHz | 128.0 ms | 1024/fs |
| | 0 | 0 | 0 | 0 | 1 | 11.025 kHz | 92.9 ms | 1024/fs |
| | 0 | 0 | 0 | 1 | 0 | 12 kHz | 85.3 ms | 1024/fs |
| | 0 | 0 | 1 | 0 | 0 | 16 kHz | 128.0 ms | 2048/fs |
| | 0 | 0 | 1 | 0 | 1 | 22.05 kHz | 92.9 ms | 2048/fs |
| | 0 | 0 | 1 | 1 | 0 | 24 kHz | 85.3 ms | 2048/fs |
| | 0 | 1 | 0 | 0 | 0 | 32 kHz | 128.0 ms | 4096/fs |
| | 0 | 1 | 0 | 0 | 1 | 44.1 kHz | 92.9 ms | 4096/fs |
| | 0 | 1 | 0 | 1 | 0 | 48 kHz | 85.3 ms | 4096/fs |
| | 0 | 1 | 1 | 0 | 0 | 64 kHz | 128.0 ms | 8192/fs |
| | 0 | 1 | 1 | 0 | 1 | 88.2 kHz | 92.9 ms | 8192/fs |
| | 0 | 1 | 1 | 1 | 0 | 96 kHz | 85.3 ms | 8192/fs |
| | 1 | 0 | 0 | 0 | 0 | 128 kHz | 128.0 ms | 16384/fs |
| | 1 | 0 | 0 | 0 | 1 | 176.4 kHz | 92.9 ms | 16384/fs |
| | 1 | 0 | 0 | 1 | 0 | 192 kHz | 85.3 ms | 16384/fs |
| | 1 | 0 | 1 | 0 | 0 | 256 kHz | 128.0 ms | 32768/fs |
| | 1 | 0 | 1 | 0 | 1 | 352.8 kHz | 92.9 ms | 32768/fs |
| | 1 | 0 | 1 | 1 | 0 | 384 kHz | 85.3 ms | 32768/fs |
| | Others | | | | | N/A | - | N/A |
| 1 | 0 | 0 | 0 | 0 | 0 | 8 kHz | 256.0 ms | 2048/fs |
| | 0 | 0 | 0 | 0 | 1 | 11.025 kHz | 185.8 ms | 2048/fs |
| | 0 | 0 | 0 | 1 | 0 | 12 kHz | 170.7 ms | 2048/fs |
| | 0 | 0 | 1 | 0 | 0 | 16 kHz | 256.0 ms | 4096/fs |
| | 0 | 0 | 1 | 0 | 1 | 22.05 kHz | 185.8 ms | 4096/fs |
| | 0 | 0 | 1 | 1 | 0 | 24 kHz | 170.7 ms | 4096/fs |
| | 0 | 1 | 0 | 0 | 0 | 32 kHz | 256.0 ms | 8192/fs |
| | 0 | 1 | 0 | 0 | 1 | 44.1 kHz | 185.8 ms | 8192/fs |
| | 0 | 1 | 0 | 1 | 0 | 48 kHz | 170.7 ms | 8192/fs |
| | 0 | 1 | 1 | 0 | 0 | 64 kHz | 256.0 ms | 16384/fs |
| | 0 | 1 | 1 | 0 | 1 | 88.2 kHz | 185.8 ms | 16384/fs |
| | 0 | 1 | 1 | 1 | 0 | 96 kHz | 170.7 ms | 16384/fs |
| | 1 | 0 | 0 | 0 | 0 | 128 kHz | 256.0 ms | 32768/fs |
| | 1 | 0 | 0 | 0 | 1 | 176.4 kHz | 185.8 ms | 32768/fs |
| | 1 | 0 | 0 | 1 | 0 | 192 kHz | 170.7 ms | 32768/fs |
| | 1 | 0 | 1 | 0 | 0 | 256 kHz | 256.0 ms | 65536/fs |
| | 1 | 0 | 1 | 0 | 1 | 352.8 kHz | 185.8 ms | 65536/fs |
| | 1 | 0 | 1 | 1 | 0 | 384 kHz | 170.7 ms | 65536/fs |
| | Others | | | | | N/A | - | N/A |

Table 27. Noise Gate Setting

| NGDIS bit | Noise Gate Status | |
|-----------|-------------------|-----------|
| 0 | Enable | (default) |
| 1 | Disable | |

< Overcurrent Protection Circuit >

If the headphone amplifier is in an overcurrent state, such as when output pins are shorted, the headphone amplifier limits the operation current. The headphone amplifier returns to a normal operation state if all causes are cleared.

■ Charge Pump & LDO Circuits

The charge pump circuits are operated by CVDD power supply voltage. CVDD is used to generate negative voltage. The power-up/down sequence of charge pump and LDO circuits are as follows. CP1 should be powered up before LDO1P/N are powered up. CP2 should be powered up after LDO1P/N are powered up. LDO1P and LDO1N blocks must be powered up or down at the same time.

Power-Up Sequence: CP1 → LDO1P, LDO1N → CP2

Power-Down Sequence: CP2 → LDO1P, LDO1N → CP1

LDO1P and LDO1N have an overcurrent protection circuit. When overcurrent flows in a normal operation, the LDO1P and LDO1N circuits limit the operation current. If the over current state is cleared, the overcurrent protection will be off and the LDO1P and LDO1N circuits will return to normal operation.

LDO2 has an overvoltage protection circuit. This overvoltage protection circuit powers the LDO2 down when the power supply becomes unstable by an instantaneous power failure, etc. during operation. The LDO2 circuit will not return to a normal operation until being reset by the PDN pin ("L" → "H") after removing the problems.

The charge pump and the LDO circuits can be powered up again while they are in power-down state.

Table 28. Input/Output Voltage and Operation Block of the Charge Pump

| Charge Pump | Power Management bit | Input Voltage | Output Voltage (Typ.) | Operation Block |
|---------------|----------------------|---------------|-----------------------|-----------------|
| CP1 | PMCP1 | CVDD | −1.8 V | LDO1N DAC |
| CP2 (Class-G) | PMCP2 | CVDD | ±1.8 V / ±0.9 V | Headphone |

Table 29. Input/Output Voltage and Operation Block of the LDO

| LDO | Power Management bit | Power Supply | Output Voltage (Typ.) | Operation Block |
|-------|----------------------|----------------------|-----------------------|-----------------------------|
| LDO1P | PMLDO1P | AVDD / VSS1 | +1.5 V | VREF+ for DAC, Headphone |
| LDO1N | PMLDO1N | VSS1 / CP2 Output | −1.5 V | VREF− for DAC, Headphone |
| LDO2 | - | LVDD / VSS1 | +1.2 V | Digital Core |

■ Serial Audio Interface

The serial audio interface format is set by DIF bit and its data length is controlled by DL[1:0] bits. In case that the input data length is less than the value which set by DL[1:0] bits, unused lower bits are filled with "0". When using master mode, DL[1:0] bits is set in accordance with the setting of BCKO bit.

Table 30. Digital I/F Format Setting

| DIF bit | Digital I/F Format | |
|---------|-----------------------------|-----------|
| 0 | I ² S Compatible | (default) |
| 1 | MSB justified | |

Table 31. Data Length Setting (x: Do not care)

| DL1 bit | DL0 bit | Data Length | BCLK Frequency | | |
|---------|---------|---------------|----------------|--------------------------|-----------|
| | | | Slave Mode | Master Mode | |
| 0 | 0 | 24-bit linear | ≥ 48fs | 64fs (BCKO bit = "0") | (default) |
| 0 | 1 | 16-bit linear | ≥ 32fs | 32fs (BCKO bit = "1") | |
| 1 | x | 32-bit linear | ≥ 64fs | 64fs (BCKO bit = "0") | |

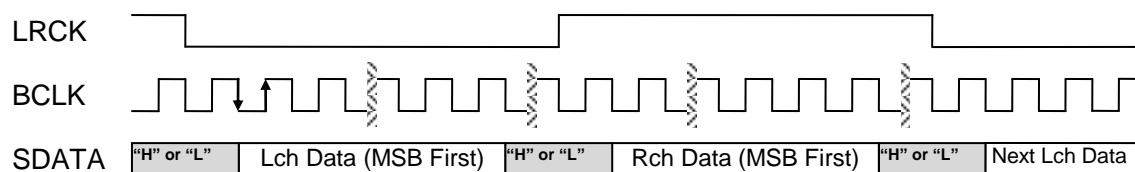


Figure 18. I²S Compatible Format (DIF bit = "0")

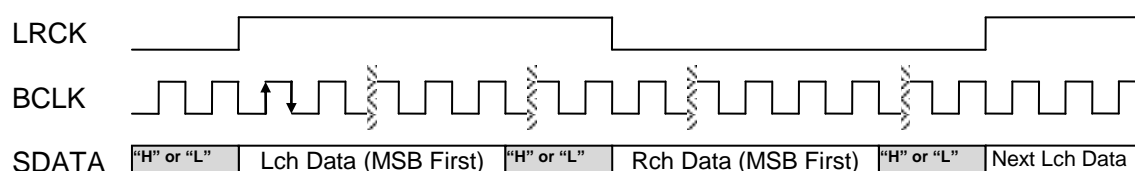


Figure 19. MSB justified format (DIF bit = "1")

■ Power-up & Operation Mode

Power Down State (PDN pin = "L")

When the PDN pin is "L", the AK4377A is in a power-down state. Power supplies must be applied when the PDN pin = "L". Set the PDN pin to "H" to release the power-down state after all the power supplies are on. More than one tPDN cycle of "L" period is needed before releasing the power-down state. The state of the AK4377A transitions to LDO2 Ctrl state by bringing the PDN pin to "H".

LDO2 Ctrl State

This is a state to control the LDO2.

LDO2 is powered up and the internal DRSTN signal is changed from "L" to "H" after max. 1 ms, and the AK4377A enters a Standby state.

Standby State

I²C interface is powered up and register accesses are enabled.

*10 ms (min.) wait time for power-up of analog circuit blocks (CP1, CP2, LDO1P, LDO1N, DAC, HP-Amp and PLL) is needed after setting the PDN pin to "H" to release the power-down state.

<State Transition Diagram>

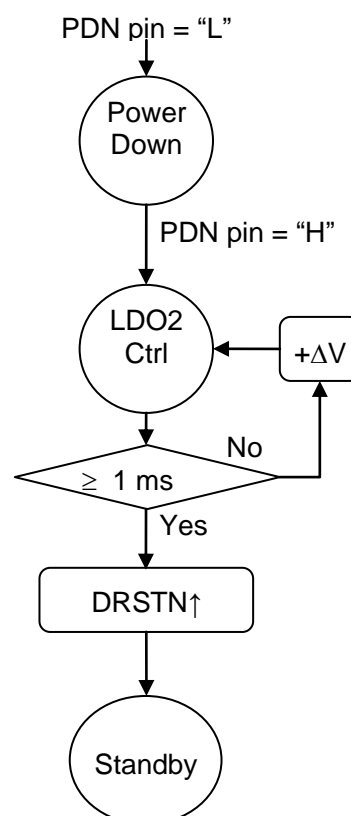


Figure 20. Device State Diagram

1. PDN pin "L" → "H"
2. Wait 1 ms until LDO2 1.2V output is stable.
3. Internal DRSTN Signal: "L" → "H"
4. Register Access Ready

■ Serial Control Interface (I²C-bus)

The AK4377A supports the fast-mode I²C-bus (max: 400 kHz). Pull-up resistors at the SDA and SCL pins must be connected to (TVDD + 0.3) V or less voltage.

1. WRITE Operation

Figure 21 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 27). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as “0010000”. If the slave address matches that of the AK4377A, the AK4377A generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 28). A R/W bit value of “1” indicates that the read operation is to be executed, and “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4377A. The format is MSB first 8 bits (Figure 23). The data after the second byte contains control data. The format is MSB first, 8 bits (Figure 24). The AK4377A generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 27).

The AK4377A can perform more than one byte write operation per sequence. After receipt of the third byte the AK4377A generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “15H” prior to generating a stop condition, the address counter will “roll over” to “00H” and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 29) except for the START and STOP conditions.

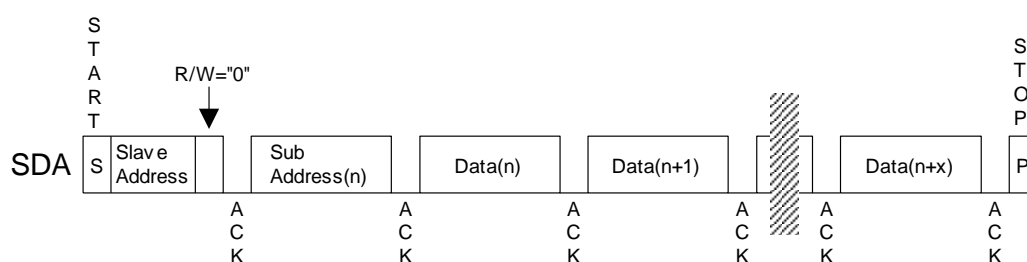


Figure 21. Data Transfer Sequence in I²C Bus Mode

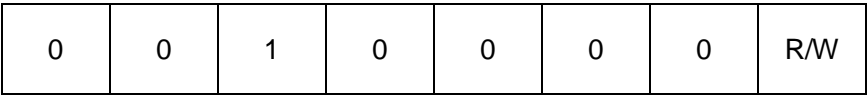


Figure 22. The First Byte

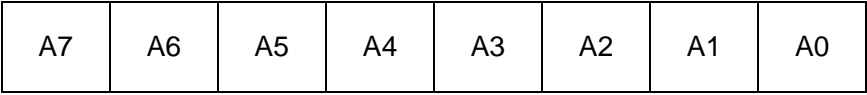


Figure 23. The Second Byte

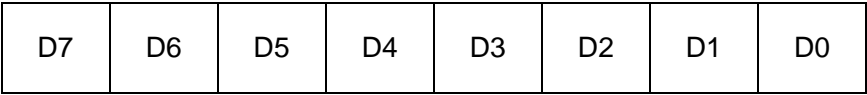


Figure 24. The Third Byte

2. READ Operation

Set the R/W bit = “1” for the READ operation of the AK4377A. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “15H” prior to generating stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.

The AK4377A supports two basic read operations: Current Address READ and Random Address READ.

2-1. Current Address READ

The AK4377A has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next Current READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4377A generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4377A ceases the transmission.

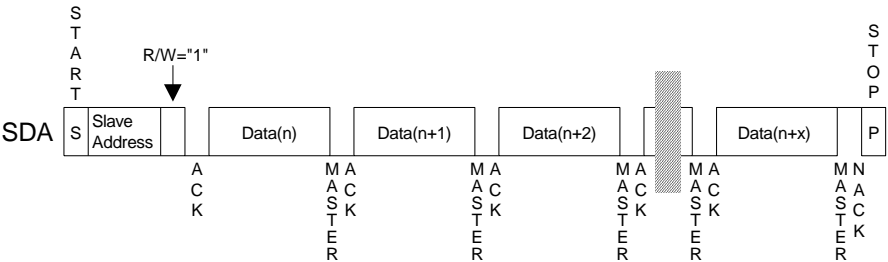


Figure 25. Current Address READ

2-2. Random Address READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4377A then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4377A ceases the transmission.

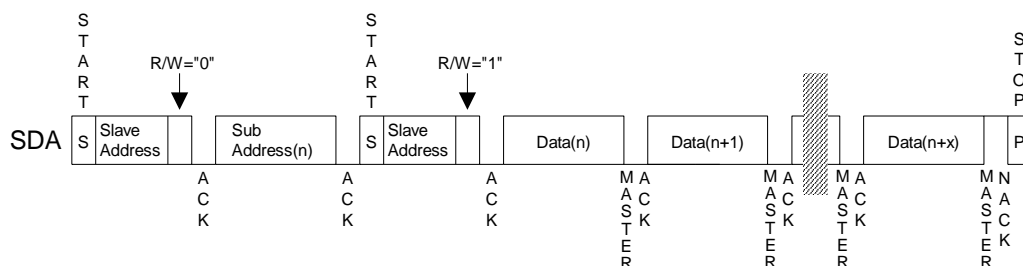


Figure 26. Random Address READ

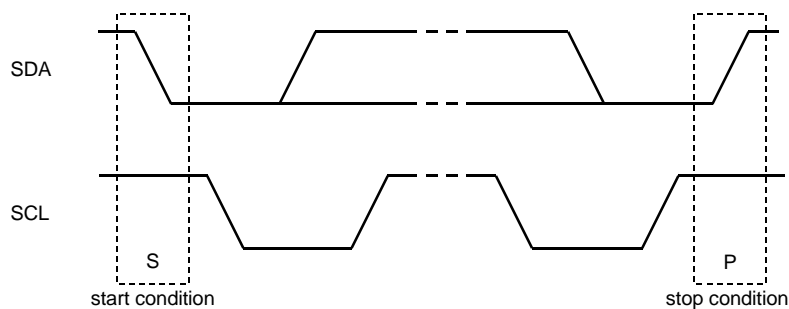


Figure 27. Start Condition and Stop Condition

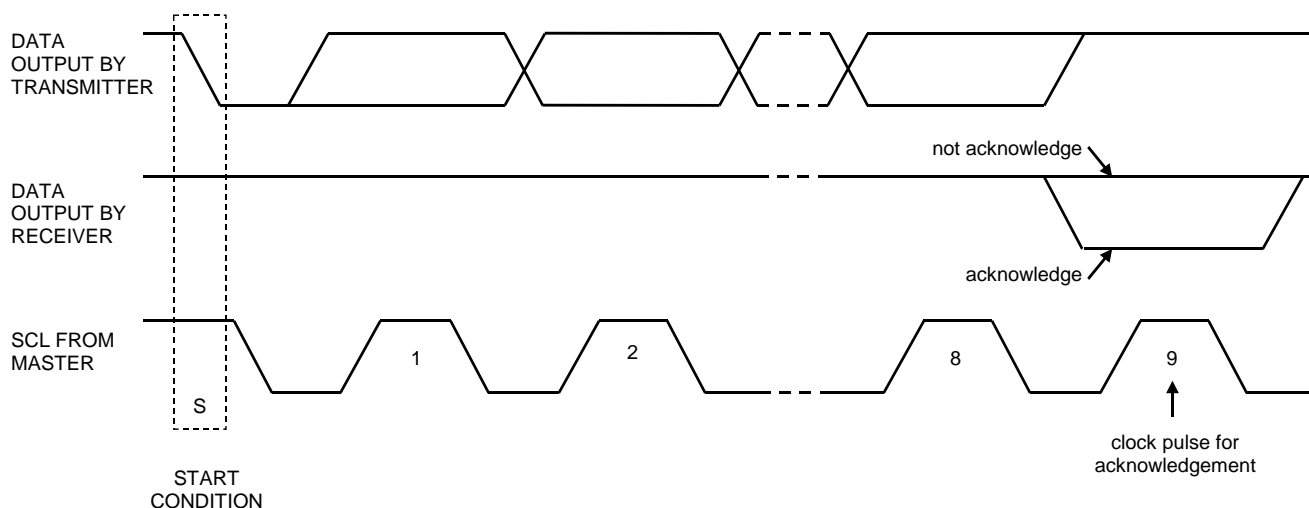


Figure 28. Acknowledge (I²C Bus)

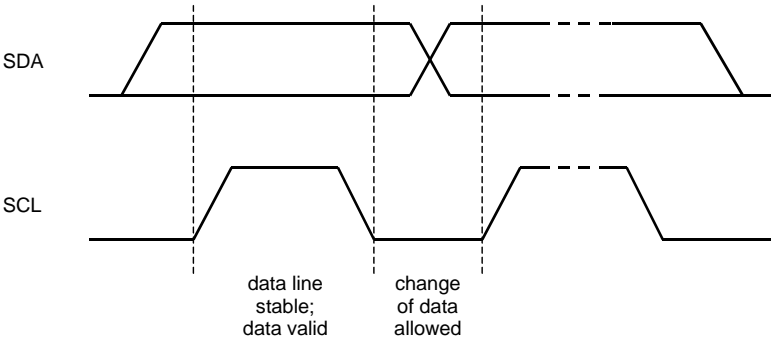


Figure 29. Bit Transfer (I²C Bus)

■ Control Sequence

Figure 30 shows power up sequence of the headphone amplifier.

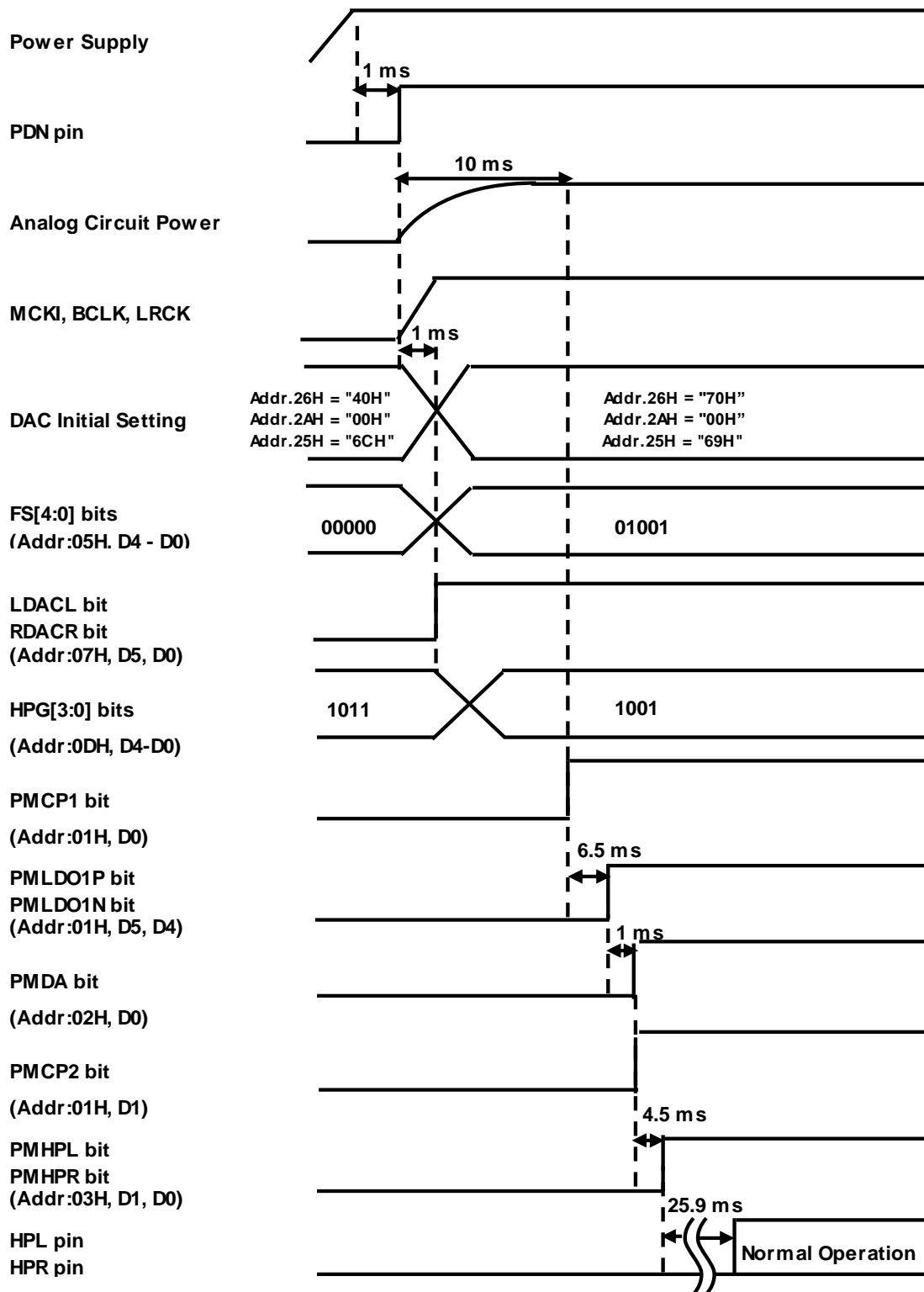


Figure 30. Power Up Sequence Example of Headphone Amplifier

<Sequence>

1. Set the PDN pin “L” → “H” after the AK4377A is powered up. In this case, 1ms or more “L” time is needed for a certain reset. (MCKI, BCLK, LRCK, SDATA, SCL and SDA should be input after all power supplies are ON.)
2. Set the PDN pin = “H” to release the power down. Register access will be valid after 1 ms. However, a wait time of 10 ms is needed to access power management bits of the analog circuit (PMCP1 bit, PMCP2 bit, PMLDO1P bit, PMLDO1N bit, PMDAC bit, PMHPL bit, PMHPR bit, PMPLL bit) until the analog circuit is powered up. Execute register write after analog circuit is powered up.
3. Input MCKI, BCLK and LRCK.
4. Set sampling frequency (FS[4:0] bits) and the input signal path of the DAC (LDACL bit = RDACR bit = “0” → “1”).
5. Set Headphone volume by HPG[3:0] bits.
6. In case of using PLL, power-up PLL (PMPLL bit = “0” → “1”) and wait 2 ms for PLL output stabilization.
7. Power up CP1 (PMCP1 bit= “0” → “1”) LDO1P and LDO1N should be powered up (PMLDO1P bit = PMLDO1N bit = “0”→“1”) after 6.5 ms (Note 78) from CP1 power-up.
8. Power up DAC (PMDA bit = “0” → “1”) DAC must be powered up after 1 ms (Note 78) from LDO1P and LDO2P power up.
9. Power up CP2 (PMCP2 bit = “0” → “1”) CP2 must be powered up after LDO1P and LDO1N are powered up.
10. Power up HPL and HPR (PMHPL bit = PMHPR bit = “0” → “1”) HPL and HPR should be powered up after 4.5 ms (Note 78) from CP2 power up. The power-up time of HP-Amp is 25.9 ms (@ fs = 44.1 kHz). The HPL pin and the HPR pin output 0 V until the HP-Amp is powered up.

Note 78. Refer to “■ Charge Pump & LDO Circuit Power-up Time”

■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|---------------|------------|------------|----------|-------------|-------------|-------------|-------|
| 00H | Power Management 1 | 0 | 0 | 0 | PMOSC | 0 | 0 | 0 | PMPLL |
| 01H | Power Management 2 | 0 | 0 | PMLDO1N | PMLDO1P | 0 | 0 | PMCP2 | PMCP1 |
| 02H | Power Management 3 | 0 | 0 | 0 | LPMODE | 0 | 0 | 0 | PMDA |
| 03H | Power Management 4 | 0 | LVDTM[2:0] | | | CPMODE[1:0] | | PMHPR | PMHPL |
| 04H | Output Mode Setting | 0 | 0 | VDDTM[3:0] | | | | HPRHZ | HPLHZ |
| 05H | Clock Mode Select | 0 | CM[1:0] | | | FS[4:0] | | | |
| 06H | Digital Filter Select | DASD | DASL | 0 | 0 | T1 | 0 | NGT | NGDIS |
| 07H | DAC Mono Mixing | INVR | MDACR | RDACR | LDACR | INVL | MDACL | RDACL | LDACL |
| 08H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0AH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0BH | Lch Output Volume | OVOLCN | 0 | 0 | OVL[4:0] | | | | |
| 0CH | Rch Output Volume | 0 | 0 | 0 | OVR[4:0] | | | | |
| 0DH | HP Volume Control | 0 | 0 | 0 | 0 | HPG[3:0] | | | |
| 0EH | PLL CLK Source Select | 0 | 0 | T2 | 0 | 0 | 0 | PLS[1:0] | |
| 0FH | PLL Ref CLK Divider 1 | PLD[15:8] | | | | | | | |
| 10H | PLL Ref CLK Divider 2 | PLD[7:0] | | | | | | | |
| 11H | PLL FB CLK Divider 1 | PLM[15:8] | | | | | | | |
| 12H | PLL FB CLK Divider 2 | PLM[7:0] | | | | | | | |
| 13H | DAC CLK Source | 0 | 0 | 0 | 0 | 0 | 0 | DACCKS[1:0] | |
| 14H | DAC CLK Divider | MDIV[7:0] | | | | | | | |
| 15H | Audio I/F Format | DEVICEID[2:0] | | | MS | BCKO | DIF | DL[1:0] | |
| 21H | CHIP ID | 0 | T101 | T100 | 0 | 0 | CHIPID[2:0] | | |
| 24H | Mode Control | 0 | DSMLP | 0 | T3 | 0 | 0 | 0 | 0 |
| 25H | DAC Adjustment3 | T109 | T108 | T107 | T106 | T105 | T104 | T103 | T102 |
| 26H | DAC Adjustment1 | T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 |
| 2AH | DAC Adjustment2 | T19 | T18 | T17 | T16 | T15 | T14 | T13 | T12 |

Note 79. PDN pin = "L" resets the registers to their default values.

Note 80. The bits defined as "0" must contain a "0" value.

Note 81. Writing accesses from 16H to 20H, 22H, 23H, 27H to 29H and 2BH to FFH are prohibited.

■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|----|----|----|-------|----|----|----|-------|
| 00H | Power Management 1 | 0 | 0 | 0 | PMOSC | 0 | 0 | 0 | PMPLL |
| | R/W | R | R | R | R/W | R | R | R | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMPLL: PLL Power Management

0: Power-Down (default)

1: Power-Up

PMOSC: Crystal Oscillator Power Management

0: Power-Down (default)

1: Power-Up

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|----|----|---------|---------|----|----|-------|-------|
| 01H | Power Management 2 | 0 | 0 | PMLDO1N | PMLDO1P | 0 | 0 | PMCP2 | PMCP1 |
| | R/W | R | R | R/W | R/W | R | R | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMCP1: Charge Pump 1 Power Management

0: Power-Down (default)

1: Power-Up

PMCP2: Charge Pump 2 Power Management

0: Power-Down (default)

1: Power-Up

PMLDO1P: LDO1P Power Management

0: Power-Down (default)

1: Power-Up

PMLDO1N: LDO1N Power Management

0: Power-Down (default)

1: Power-Up

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|----|----|----|--------|----|----|----|------|
| 02H | Power Management 3 | 0 | 0 | 0 | LPMODE | 0 | 0 | 0 | PMDA |
| | R/W | R | R | R | R/W | R | R | R | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMDA: DACDIG Power Management

0: Power-Down (default)

1: Power-Up

LPMODE: DAC & HP-Amp Low Power Mode Setting

0: High Performance Mode (default)

1: Low Power Mode

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|----|------------|----|----|-------------|----|-------|-------|
| 03H | Power Management 4 | 0 | LVDTM[2:0] | | | CPMODE[1:0] | | PMHPR | PMHPL |
| | R/W | R | R/W | | | R/W | | R/W | R/W |
| | Default | 0 | 000 | | | 00 | | 0 | 0 |

PMHPL/R: HP-Amp L/Rch Power Management

0: Power-Down (default)

1: Power-Up

CPMODE[1:0]: Charge Pump Mode Control ([Table 18](#))

Default: "00" (Automatic Switching Mode)

LVDTM[2:0]: Class-G 1/2VDD Mode Detection Time Setting ([Table 20](#))

Default: "000" (64/fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------|----|----|------------|----|----|----|-------|-------|
| 04H | Output Mode Setting | 0 | 0 | VDDTM[3:0] | | | | HPRHZ | HPLHZ |
| | R/W | R | R | R/W | | | | R/W | R/W |
| | Default | 0 | 0 | 0000 | | | | 0 | 0 |

HPRHZ/HPLHZ: GND Switch Setting for HP-Amp Output

0: Pull-Down by 6 Ω (Typ.) (default)

1: Pull-Down by 200 k Ω (Typ.)

VDDTM[3:0]: Class-G VDD Mode Hold Time Setting ([Table 19](#))

Default: "0000" (1024/fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|----|---------|----|---------|----|----|----|----|
| 05H | Clock Mode Select | 0 | CM[1:0] | | FS[4:0] | | | | |
| | R/W | R | R/W | | R/W | | | | |
| | Default | 0 | 00 | | 0 0000 | | | | |

FS[4:0]: Sampling Frequency Setting ([Table 5](#))

Default: "00000" (fs = 8 kHz)

CM[1:0]: Master Clock Setting ([Table 3](#), [Table 4](#))

Default: "00" (256fs @Normal/Double Speed Mode / 32fs @Oct Speed Mode)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|------|------|----|----|-----|----|-----|-------|
| 06H | Digital Filter Select | DASD | DASL | 0 | 0 | T1 | 0 | NGT | NGDIS |
| | R/W | R/W | R/W | R | R | R/W | R | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

NGDIS: Noise Gate Setting

0: Noise Gate Enable (default)

1: Noise Gate Disable

NGT: Noise Gate Timer Setting ([Table 26](#))

Default: "0"

T1: Write "0" into this bit.

DASD, DASL: DAC Digital Filter Mode Setting ([Table 14](#))

Default: "0, 0" (Sharp Roll-Off Filter)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|------|-------|-------|-------|------|-------|-------|-------|
| 07H | DAC Mono Mixing | INVR | MDACR | RDACR | LDACR | INVL | MDACL | RDACL | LDACL |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MDACL, RDACL, LDACL: DAC Lch Input Signal Select ([Table 15](#))

Default: "0, 0, 0" (MUTE)

MDACR, RDACR, LDACR: DAC Rch Input Signal Select ([Table 15](#))

Default: "0, 0, 0" (MUTE)

INVL/R: DAC Input Signal Polarity Select

0: Normal (default)

1: Inverting

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 08H 09H 0AH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Write "0" to the addresses from 08H to 0AH.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|--------|----|----|----|----|----------|----|----|
| 0BH | Lch Output Volume | OVOLCN | 0 | 0 | | | OVL[4:0] | | |
| 0CH | Rch Output Volume | 0 | 0 | 0 | | | OVR[4:0] | | |
| | R/W | R/W | R | R | | | R/W | | |
| | Default | 0 | 0 | 0 | | | 19H | | |

OVL[4:0]: DAC Lch Digital Volume Control; +3 dB to –12 dB & Mute, 0.5 dB step ([Table 17](#))

OVR[4:0]: DAC Rch Digital Volume Control; +3 dB to –12 dB & Mute, 0.5 dB step ([Table 17](#))

Default: “19H” (0 dB)

OVOLCN: Digital Volume Control

0: Dependent (default)

1: Independent

OVL[4:0] bits control digital volume of both L and R channels when OVOLCN bit = “0”. In this case, the value of OVL[4:0] bits will not be written to OVR[4:0] bits.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|----|----|----|----|----|----------|----|----|
| 0DH | HP Volume Control | 0 | 0 | 0 | 0 | | HPG[3:0] | | |
| | R/W | R | R | R | R | | R/W | | |
| | Default | 0 | 0 | 0 | 0 | | BH | | |

HPG[3:0]: HP-Amp Analog Volume Control; +6 dB to –20 dB, 2 dB step ([Table 21](#))

Default: BH (0 dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|----|----|-----|----|----|----|----------|----|
| 0EH | PLL CLK Source Select | 0 | 0 | T2 | 0 | 0 | 0 | PLS[1:0] | |
| | R/W | R | R | R/W | R | R | R | R/W | |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 00 | |

PLS[1:0]: PLL Clock Source Select ([Table 7](#))

Default: “00” (MCKI pin)

T2: Write “0” into this bit.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|----|----|----|----|----|----|----|----|
| 0FH | PLL Ref CLK Divider 1 | | | | | | | | |
| 10H | PLL Ref CLK Divider 2 | | | | | | | | |
| | R/W | | | | | | | | |
| | Default | | | | | | | | |

PLD[15:0]: PLL Reference Clock Divider Setting ([Table 8](#))

Default: 0000H (Divided by 1)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------|-----------|----|----|----|----|----|----|----|
| 11H | PLL FB CLK Divider 1 | PLM[15:8] | | | | | | | |
| 12H | PLL FB CLK Divider 2 | PLM[7:0] | | | | | | | |
| | R/W | R/W | | | | | | | |
| | Default | 0000H | | | | | | | |

PLM[15:0]: PLL Feedback Clock Divider Setting ([Table 9](#))

Default: 0000H (Clock Stop)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|----|----|----|----|----|----|-------------|----|
| 13H | DAC CLK Source | 0 | 0 | 0 | 0 | 0 | 0 | DACCKS[1:0] | |
| | R/W | R | R | R | R | R | R | R/W | |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 00 | |

DACCKS[1:0]: DAC Master Clock Source Select ([Table 1](#))

Default: "00" (MCKI pin)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|-----------|----|----|----|----|----|----|----|
| 14H | DAC CLK Divider | MDIV[7:0] | | | | | | | |
| | R/W | R/W | | | | | | | |
| | Default | 00H | | | | | | | |

MDIV[7:0]: DACMCLK Divider Setting ([Table 13](#))

Default: 00H (Divided by 1)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------|---------------|----|----|-----|------|-----|---------|----|
| 15H | CODEC I/F Format | DEVICEID[2:0] | | | MS | BCKO | DIF | DL[1:0] | |
| | R/W | R | R | R | R/W | R/W | R/W | R/W | |
| | Default | 0 | 1 | 0 | 0 | 0 | 0 | 00 | |

DL[1:0]: Data Length Setting ([Table 31](#))

Default: "00" (24-bit linear)

DIF: Digital I/F Format Setting ([Table 30](#))

Default: "0" (I²S Compatible)

BCKO: BCLK Output Frequency

0: 64fs (default)

1: 32fs

MS: Master/Slave Mode Setting

0: Slave Mode (default)

1: Master Mode

DEVICEID[2:0]: Device ID

Default: "010" (AK4377, AK4376A: "010")

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|------|------|----|----|-------------|----|----|
| 21H | CHIPID | 0 | T101 | T100 | 0 | 0 | CHIPID[2:0] | | |
| | R/W | R | R/W | R/W | R | R | R | R | R |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

CHIPID[2:0]: CHIPID

Default: "001" (AK4376: "000", AK4376A: "001", AK4377A: "010")

T101, T100: Write "0" into these bits.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|-------|----|-----|----|----|----|----|
| 24H | Mode Control | 0 | DSMLP | 0 | T3 | 0 | 0 | 0 | 0 |
| | R/W | R | R/W | R | R/W | R | R | R | R |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DSMLP: DAC Operation Mode Setting ([Table 3](#), [Table 4](#))

Default: "0"

T3: Write "0" into this bit.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|------|------|------|------|------|------|------|------|
| 25H | DAC Adjustment3 | T109 | T108 | T107 | T106 | T105 | T104 | T103 | T102 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

*"69H" data must be written to DAC Adjustment3 (Addr.25H) before analog blocks (CP1, CP2, LDO1, DAC, HP-Amp, PLL) are powered up.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 26H | DAC Adjustment1 | T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

*"70H" data must be written to DAC Adjustment1 (Addr.26H) before analog blocks (CP1, CP2, LDO1, DAC, HP-Amp, PLL) are powered up

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 2AH | DAC Adjustment2 | T19 | T18 | T17 | T16 | T15 | T14 | T13 | T12 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

T19, T18, T17, T16: Write "0" into these bits

T15, T14, T13, T12: DAC Adjustment Setting

Default: "0000"

*Write "00H" to DAC Adjustment2 (Addr.2AH) before the analog block (CP1, CP2, LDO1, DAC, HP-Amp, PLL) is powered up.

*Recommended setting of DAC Adjustment2 (Addr.2AH) is "00H" data.

However, T[15:12] bits setting should be changed appropriately since the optimum setting for T[15:12] bits varies depending on the PCB layout.

10. Recommended External Circuits

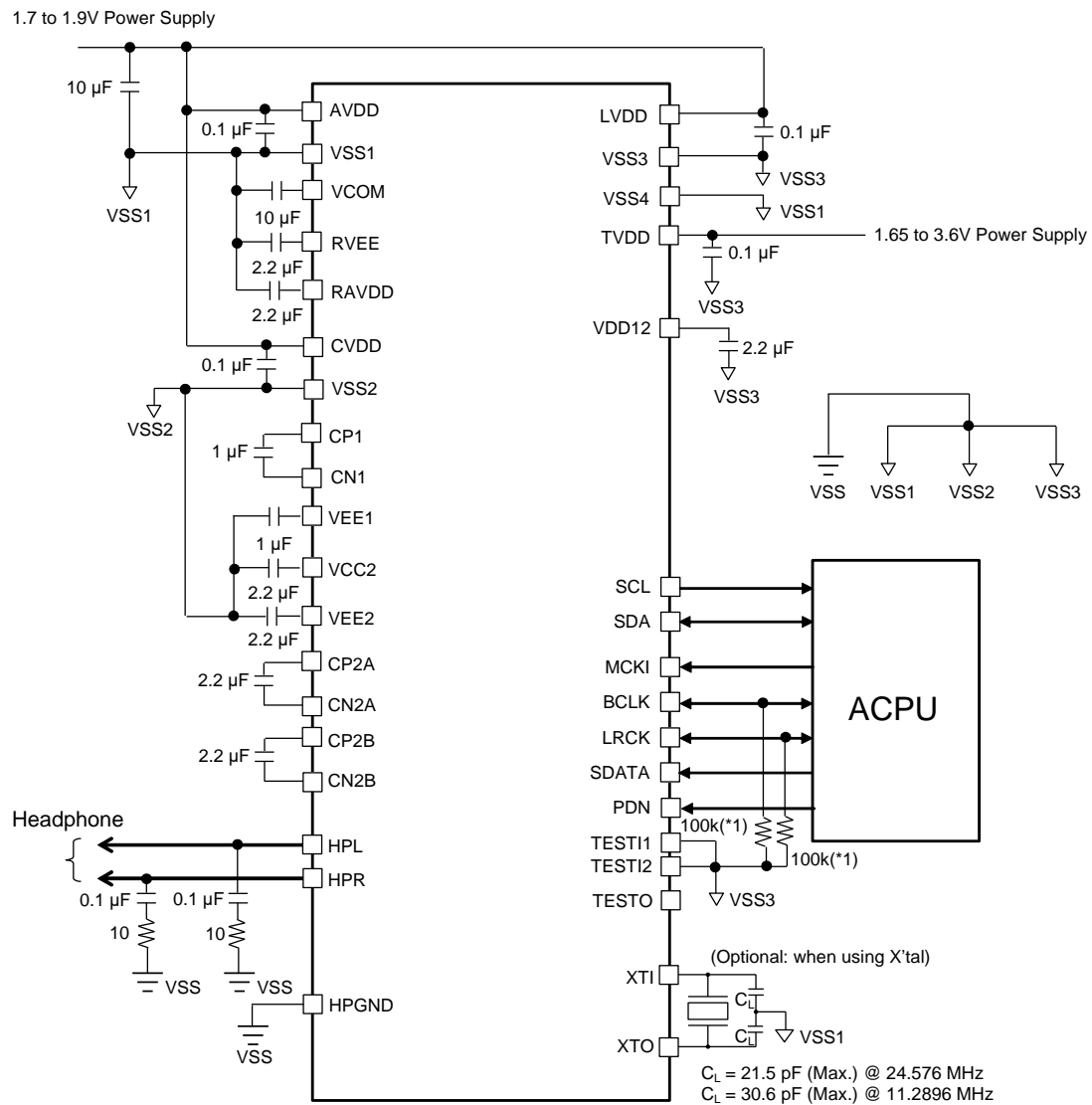


Figure 31. System Connection Diagram

*1: When the AK4377A is in master mode, a pull-down resistor (e.g. 100 k Ω) is needed.

1. Grounding and Power Supply Decoupling

The AK4377A requires careful attention to power supply and grounding arrangements. The PDN pin should be held “L” when power supplies are tuning on. AVDD should be powered up before or at the same time of CVDD. Power-up sequence of TVDD and LVDD is not critical. The PDN pin is allowed to be “H” after all power supplies are applied and settled. To power down the AK4377A, set the PDN pin to “L” and power down CVDD before or at the same time of AVDD. Power-down sequence of LVDD and TVDD is not critical.

To avoid pop noise on analog output when power up/down, the AK4377A should be operated along the following recommended power-up/down sequence.

1) Power-up

- The PDN pin should be held “L” when power supplies are turning on. The AK4377A can be reset by keeping the PDN pin “L” for 1 ms or longer after all power supplies are applied and settled. Then release the reset by setting the PDN pin to “H”.

2) Power-down

- Each of power supplies can be powered OFF after the PDN pin is set to “L”.

VSS1, VSS2, VSS3 and VSS4 of the AK4377A should be connected to the analog ground plane. System analog ground and digital ground should be connected together near where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close the power supply pins as possible. Especially, the small value ceramic capacitor is to be closest.

2. Voltage Reference

VCOM is a common voltage of this chip. A 10 μ F ceramic capacitor attached between the VCOM pin eliminates the effects of high frequency noise. No load current is allowed to be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4377A.

3. Charge Pump and LDO Circuits

Capacitors for CP1 block (connected between the CP1 pin and the CN1 pin, between the VEE1 pin and the VSS2 pin) should be low ESR 1.0 μ F \pm 50%. Capacitors for LDO1 block (connected between the RAVDD pin and the VSS1 pin, between the RVEE pin and the VSS1 pin) should be low ESR from 1.0 μ F \pm 50 % to 4.7 μ F \pm 50 %.

Capacitors for CP2 block (connected between the CP2A pin and the CN2A pin, between the CP2B pin and the CN2B pin, between the VCC2 pin and the VSS2 pin, between the VEE2 pin and the VSS2 pin) should be low ESR 2.2 μ F \pm 50 %. These capacitors must be connected as close as possible to the pins. No load current may be drawn from the Positive / Negative Power Output pin (VEE1, RAVDD, RVEE, VCC2 and VEE2 pins).

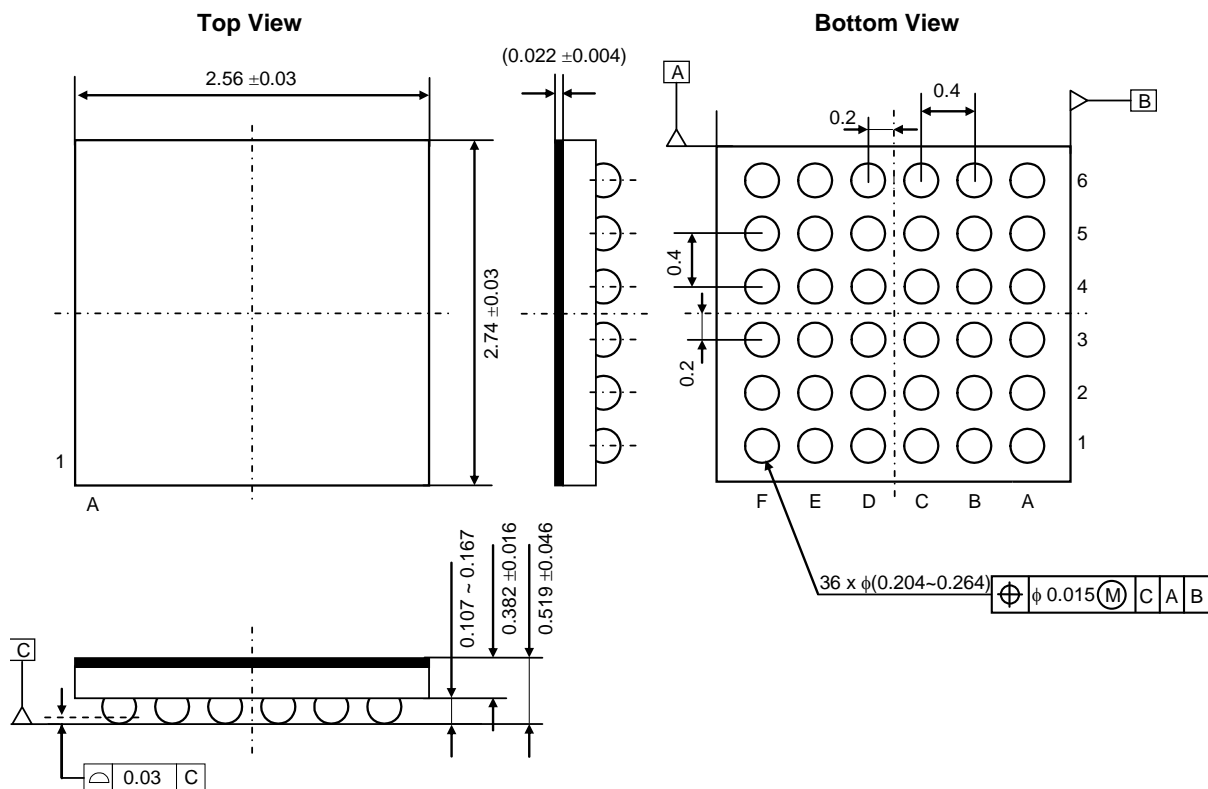
4. Analog Outputs

Headphone outputs are single-ended and centered at HPGND (0 V). A headphone can be driven directly since a capacitor for AC coupling is not necessary.

11. Package

■ Outline Dimensions

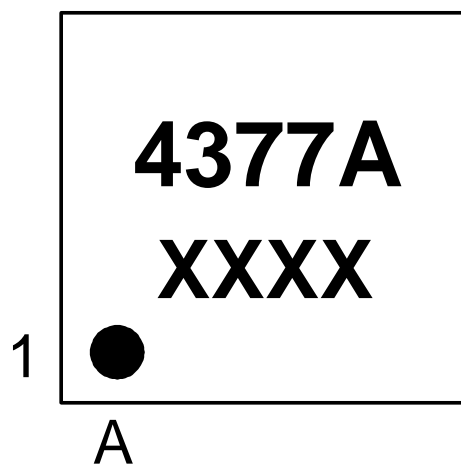
36-pin CSP (Unit: mm)



■ Material and Lead Finish

Package molding compound: Epoxy Resin, Halogen Free
Lead frame material: SnAgCu

■ Marking



XXXX: Date code (4 digits)
Pin #A1 indication

12. Ordering Guide

AK4377AECB −40 to 85 °C 36-pin CSP (0.4 mm pitch)
AKD4377A Evaluation board for AK4377A

| |
|-----------------------------|
| 13. Revision History |
|-----------------------------|

| Date (Y/M/D) | Revision | Reason | Page | Contents |
|--------------|----------|---------------|------|----------|
| 18/02/15 | 00 | First Edition | | |

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