AK4133

192kHz 24bit Sample Rate Converter

1. General Description

The AK4133 is an 2ch digital sample rate converter (SRC). It converts sample rate of the input audio source (from 8kHz to 192kHz) to 44.1kHz or 48kHz. It is possible also to convert 8kHz, 16kHz or 24kHz into 8kHz, 16kHz or 24kHz. The AK4133 has an internal Oscillator and does not need any external master clocks. It contributes simplifying a system configuration. The AK4133 is suitable for the application interfacing to different sample rates such as Car Audio Systems and DVD recorders.

2. Features

- ☐ 2 channels Input/Output
- ☐ Asynchronous Sample Rate Converter
- ☐ Input Sample Rate Range (FSI): 8k ~ 192kHz
- ☐ Output Sample Rate (FSO): 44.1kHz, 48kHz (@FSI=8k~192kHz)
  8kHz, 16kHz, 24kHz (@FSI=8kHz, 16kHz, 24kHz)
- ☐ Input to Output Sample Rate Ratio: FSO/FSI= 44.1/192~6
- ☐ THD+N: Up to -100dB
- ☐ Dynamic Range: 110dB (A-weighted, Typ.)
- ☐ I/F format: MSB justified, I^2S compatible
- ☐ Oscillator for Internal Operation Clock
- ☐ Clock for Master Mode: 128/256/512fso
- ☐ Soft Mute Function
- ☐ Power Supply: DVDD= 3.0 ~ 3.6V or 1.7 ~ 1.9V(LDO OFF Mode)
- ☐ Operating Temperature: –40 ~ 105ºC
- ☐ Package: 20-pin QFN 4mm x 4mm (0.5mm pitch)

3. Table of Contents

4. Block Diagram

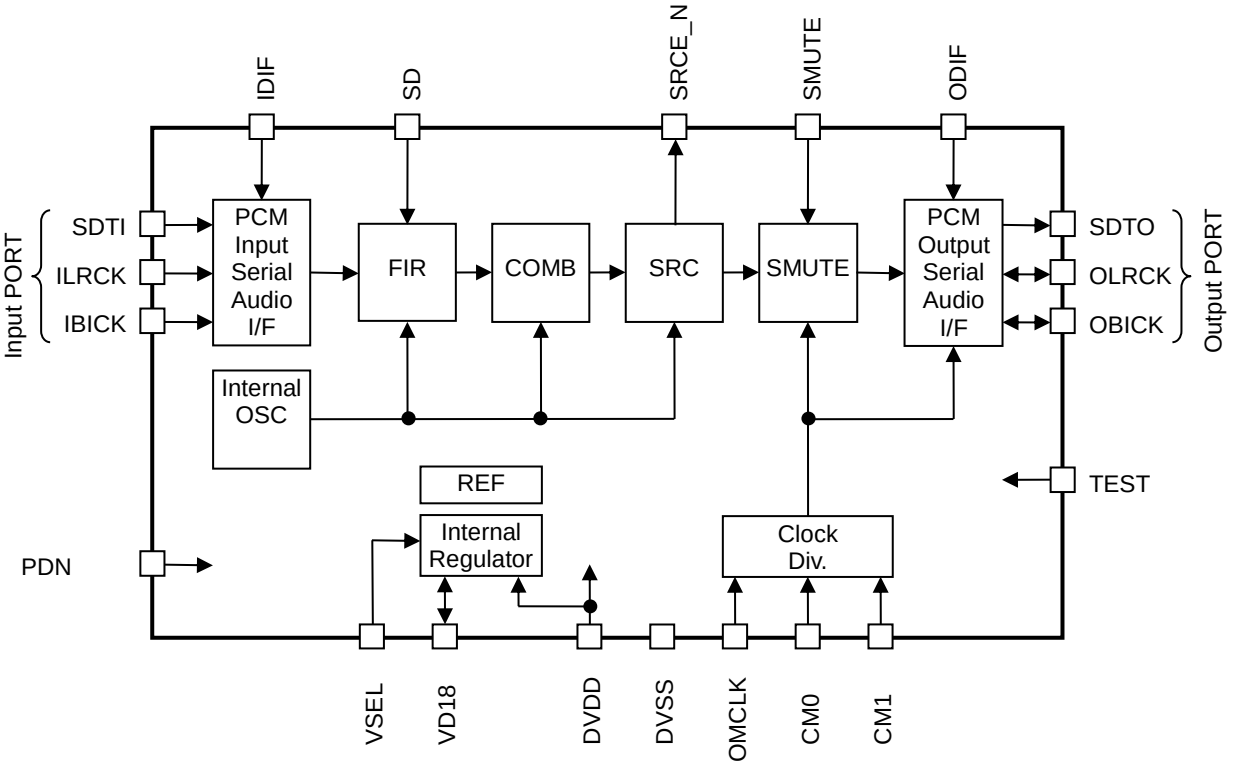


Figure 1. AK4133 Block Diagram

5. Pin Configulations and Functions

■ Pin Layout

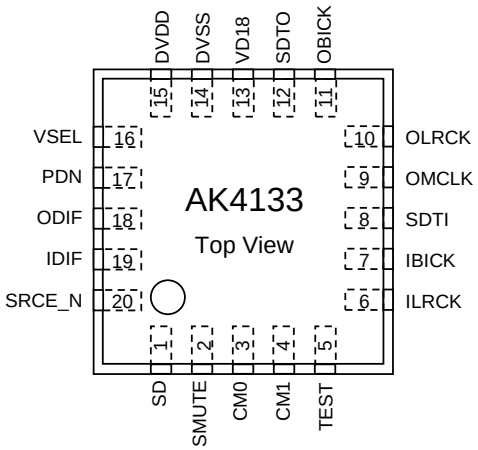


Figure 2. Pin Layout

■ Functions

No.	Pin Name	I/O	Function	PDN= "L" Status
1	SD	I	Digital Filter Select Pin "H": Short Delay Sharp Roll-off Filter "L": Sharp Roll-off Filter	-
2	SMUTE	I	Soft Mute Pin When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.	-
3	CM0	I	Output Port Mode and OMCLK Frequency Select #0 Pin	-
4	CM1	I	Output Port Mode and OMCLK Frequency Select #1 Pin	-
5	TEST	I	Test pin. Must be connected to DVSS in normal use. It has a pull-down resister 100kΩ.	-
6	ILRCK	I	Channel Clock Input Pin for Input PORT	-
7	IBICK	I	Audio Serial Clock Input Pin for Input PORT	-
8	SDTI	I	Audio Serial Data Input Pin for Input PORT	-
9	OMCLK	I	External Master Clock Input	-
10	OLRCK	O	Channel Clock Output Pin for Output PORT in Master Mode	"L"
		I	Channel Clock Input Pin for Output PORT in Slave Mode	-
11	OBICK	O	Audio Serial Clock Output Pin for Output PORT in Master Mode	"L"
		I	Audio Serial Clock Input Pin for Output PORT in Slave Mode	-
12	SDTO	O	Audio Serial Data Output Pin for Output PORT	"L"
13	VD18	I	Internal Digital Power Supply Pin, 1.7 ~ 1.9V (VSEL= "H")	-
		O	Regulator Output Pin, Typ. 1.8V (VSEL= "L") Current must not be taken from this pin. A 10μF (±30%; including the temperature characteristics) capacitor should be connected between this pin and DVSS. When this capacitor is polarized, the positive polarity pin should be connected to the VD18 pin.	"L"
14	DVSS	-	Digital Ground Pin	-
15	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V or 1.7 ~ 1.9V	-
16	VSEL	I	Internal Digital Power Supply Select Pin "H": External Power Supply "L": Internal Regulator	-
17	PDN	I	Power-Down Mode Pin "H": Power up "L": Power down and reset The AK4133 should be reset once by bringing PDN pin = "L" upon power-up.	-
18	ODIF	I	Audio Interface Format Select Pin for Output PORT	-
19	IDIF	I	Audio Interface Format Select Pin for Input PORT	-
20	SRCE_N	O	Unlock Status Pin	"H"

Note:
* 1. All input pins should not be allowed to float.
* 2. CM1-0, ODIF and IDIF pins must be changed when the PDN pin = "L".

■ Handling of Unused Pin

Classification	Pin Name	Setting
Digital	SMUTE	Connect to DVSS
	OMCLK	Connect to DVSS
	SRCE_N	Open

6. Absolute Maximum Ratings

(DVSS=0V;* 3)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Digital	DVDD	−0.3	4.3	V
	Internal Digital	VD18	−0.3	2.5	V
Input Current, Any Pin Except Supplies		IIN	−10	10	mA
Digital Input Voltage (* 4)		VDIN	−0.3	DVDD+0.3 or 4.3	V
Ambient Temperature (Power applied) (* 5)		Ta	−40	105	ºC
Storage Temperature		Tstg	−65	150	ºC

Note:
* 3. All voltages with respect to ground.
* 4. ILRCK, IBICK, SDTI, IDIF, SD, PDN, TEST, OMCLK, CM1-0, ODIF, OBICK (Slave Mode), OLRCK (Slave Mode), SMUTE and VSEL pins
* 5. PCB drawing density should be 100% or more.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(DVSS=0V; * 3; VSEL= “L”)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Digital	DVDD	3.0	3.3	3.6	V

Note:
* 3. All voltages with respect to ground.

(DVSS=0V;* 3; VSEL= “H”)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (* 6)	Digital	DVDD	1.7	1.8	1.9	V
	Internal Digital	VD18	1.7	1.8	1.9	V
	Difference	DVDD-VD18	-	0		V

Note:
* 3. All voltages with respect to ground.
* 6. DVDD and VD18 must be connected externally.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. SRC Characteristics

(Ta= -40 ~ 105ºC; DVDD= 3.0 ~ 3.6V at VSEL pin= "L" or DVDD= VD18= 1.7 ~ 1.9V at VSEL pin= "H"; DVSS= 0V; Signal Frequency= 1kHz; measurement bandwidth = 20Hz ~ FSO/2; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Sample Rate	FSI	8	-	192	kHz
Output Sample Rate	FSO	44.1	-	48	kHz
Output Sample Rate (FSI: 8kHz, 16kHz, 24kHz)	FSO	8	-	24	kHz
THD+N (Input= 1kHz, 0dBFS, * 7)					
FSO/FSI= 48kHz/48kHz		-	-111	-	dB
FSO/FSI= 44.1kHz/48kHz		-	-106	-	dB
FSO/FSI= 48kHz/192kHz		-	-111	-	dB
Worst Case (FSO/FSI= 44.1kHz/96kHz)		-	-	-105	dB
Dynamic Range (Input= 1kHz, -60dBFS, * 7)					
FSO/FSI= 48kHz/48kHz		-	112	-	dB
FSO/FSI= 44.1kHz/48kHz		-	112	-	dB
FSO/FSI= 48kHz/192kHz		-	112	-	dB
Worst Case (FSO/FSI= 44.1kHz/192kHz)		111	-	-	dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted, * 7)					
FSO/FSI= 48kHz/48kHz		-	115	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	44.1/192	-	6	-

Note:

* 7. Measured by Audio Precision, System Two.

9. Consumption Current

■ Internal Regurator (VSEL pin= "L")

(Ta= -40 ~ 105ºC)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Current					
Normal operation:					
FSI= FSO= 48kHz at Master Mode :					
DVDD= 3.3V		-	6	-	mA
DVDD= 3.6V		-	-	8	mA
FSI= 96kH, FSO= 48kHz at Master Mode :					
DVDD=3.3V		-	10	-	mA
DVDD=3.6V		-	-	12	mA
FSI= 192kH, FSO= 48kHz at Master Mode :					
DVDD=3.3V		-	16	-	mA
DVDD=3.6V		-	-	18	mA
Power down: PDN = "L" (* 8)					
DVDD=3.6V		-	10	100	μA

Note:

* 8. All digital input pins including clock pins are connected to DVSS.

■ External VD18 (VSEL pin= "H")

(Ta= -40 ~ 105ºC)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Current					
Normal operation:					
FSI=FSO=48kHz at Master Mode:					
DVDD=VD18=1.8V		-	6	-	mA
DVDD=VD18=1.9V		-	-	8	mA
FSI=96kH, FSO=48kHz at Master Mode:			-		
DVDD=VD18=1.8V		-	10	-	mA
DVDD=VD18=1.9V		-	-	12	mA
FSI=192kH, FSO=48kHz at Master Mode:					
DVDD=VD18=1.8V		-	16	-	mA
DVDD=VD18=1.9V		-	-	18	mA
Power down: PDN = "L" (* 9) DVDD=VD18=1.9V		-	10	100	μA

Note:

* 9. Except the VSELL pin, all digital input pins including clock pins are connected to DVSS.

10. Filter Characteristics

■ Sharp Roll-Off Characteristics (SD pin= "L")

(Ta= -40 ~ 105ºC; DVDD= 3.0 ~ 3.6V at VSEL pin= "L" or DVDD= VD18= 1.7 ~ 1.9V at VSEL pin= "H"; DVSS= 0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband −0.01dB	0.985 ≤ FSO/FSI ≤ 6.000	PB	0	-	0.4583FSI	kHz
	0.714 ≤ FSO/FSI < 0.985	PB	0	-	0.4167FSI	kHz
	0.536 ≤ FSO/FSI < 0.714	PB	0	-	0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0	-	0.2177FSI	kHz
	0.324 ≤ FSO/FSI < 0.492	PB	0	-	0.1948FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0	-	0.0917FSI	kHz
	0.1667≤ FSO/FSI < 0.246	PB	0	-	0.0826FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI	-	-	kHz
	0.714 ≤ FSO/FSI < 0.985	SB	0.5021FSI	-	-	kHz
	0.536 ≤ FSO/FSI < 0.714	SB	0.2974FSI	-	-	kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI	-	-	kHz
	0.324 ≤ FSO/FSI < 0.492	SB	0.2604FSI	-	-	kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI	-	-	kHz
	0.1667≤ FSO/FSI < 0.246	SB	0.1471FSI	-	-	kHz
Passband Ripple	0.1667≤ FSO/FSI ≤ 6.000	PR	-	-	±0.01	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 6.000	SA	-92.2	-	-	dB
	0.714 ≤ FSO/FSI < 0.985	SA	-92.2	-	-	dB
	0.536 ≤ FSO/FSI < 0.714	SA	-92.8	-	-	dB
	0.492 ≤ FSO/FSI < 0.536	SA	-91.9	-	-	dB
	0.324 ≤ FSO/FSI < 0.492	SA	-92.7	-	-	dB
	0.246 ≤ FSO/FSI < 0.324	SA	-93.9	-	-	dB
	0.1667≤ FSO/FSI < 0.246	SA	-92.1	-	-	dB
Group Delay (* 10)		GD	-	60	-	1/fs

Note:

* 10. This value is the time from a rising edge of LRCK after L/R data is input to a rising edge of LRCK before the L/R data is output when there is no phase difference between the input and the output data.

■ **Short Delay Sharp Roll-Off Filter Characteristics (SD pin= "H")**

(Ta= -40 ~ 105ºC; DVDD= 3.0 ~ 3.6V at VSEL pin= "L" or DVDD= VD18= 1.7 ~ 1.9V at VSEL pin= "H"; DVSS= 0V)

Parameter		Symbol	Min.	Typ.	Max	Unit
Digital Filter						
Passband –0.01dB	0.985 ≤ FSO/FSI ≤ 6.000	PB	0	-	0.4583FSI	kHz
	0.714 ≤ FSO/FSI < 0.985	PB	0	-	0.4167FSI	kHz
	0.536 ≤ FSO/FSI < 0.714	PB	0	-	0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0	-	0.2177FSI	kHz
	0.324 ≤ FSO/FSI < 0.492	PB	0	-	0.1948FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0	-	0.0917FSI	kHz
	0.1667≤ FSO/FSI < 0.246	PB	0	-	0.0826FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI	-	-	kHz
	0.714 ≤ FSO/FSI < 0.985	SB	0.5021FSI	-	-	kHz
	0.536 ≤ FSO/FSI < 0.714	SB	0.2974FSI	-	-	kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI	-	-	kHz
	0.324 ≤ FSO/FSI < 0.492	SB	0.2604FSI	-	-	kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI	-	-	kHz
	0.1667≤ FSO/FSI < 0.246	SB	0.1471FSI	-	-	kHz
Passband Ripple	0.1667≤ FSO/FSI ≤ 6.000	PR	-	-	±0.01	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 6.000	SA	-92.8	-	-	dB
	0.714 ≤ FSO/FSI < 0.985	SA	-93.5	-	-	dB
	0.536 ≤ FSO/FSI < 0.714	SA	-94.5	-	-	dB
	0.492 ≤ FSO/FSI < 0.536	SA	-92.9	-	-	dB
	0.324 ≤ FSO/FSI < 0.492	SA	-92.0	-	-	dB
	0.246 ≤ FSO/FSI < 0.324	SA	-94.4	-	-	dB
	0.1667≤ FSO/FSI < 0.246	SA	-93.8	-	-	dB
Group Delay (* 10)		GD	-	18	-	1/fs

Note:

* 10. This value is the time from a rising edge of LRCK after L/R data is input to a rising edge of LRCK before the L/R data is output when there is no phase difference between the input and the output data.

11. DC Characteristics

(Ta= -40 ~ 105ºC; DVDD= 3.0 ~ 3.6V at VSEL pin= "L" or DVDD= VD18= 1.7 ~ 1.9V at VSEL pin= "H"; DVSS= 0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage	(* 11)	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	(* 11)	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=–400μA)	(* 12)	VOH	DVDD–0.4	-	-	V
Low-Level Output Voltage (Iout= 400μA)	(* 12)	VOL	-	-	0.4	V
Input Leakage Current	(* 11, Except TEST pin)	Iin	–10	-	10	μA
	TEST pin 100kΩ Pull down		–10	-	72	μA

Notes:

* 11. ILRCK, IBICK, SDTI, IDIF, SD, PDN, TEST, OMCLK, CM0, CM1, ODIF, OBICK (Slave Mode), OLRCK (Slave Mode), SMUTE and VSEL pins

* 12. SRCE_N, SDTO, OBICK (Master Mode) and OLRCK (Master Mode) pins

12. Switching Characteristics

■ **Clock**

(Ta= -40 ~ 105ºC; DVDD= 3.0 ~ 3.6V at VSEL pin= “L” or DVDD= VD18= 1.7 ~ 1.9V at VSEL pin= “H”; C_L= 20pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Master Clock Input (OMCLK)						
128 FSO:						
Frequency		fCLK	1.024	-	6.144	MHz
Pulse Width Low		tCLKL	80	-	-	ns
Pulse Width High		tCLKH	80	-	-	ns
256 FSO:						
Frequency		fCLK	2.048	-	12.288	MHz
Pulse Width Low		tCLKL	40	-	-	ns
Pulse Width High		tCLKH	40	-	-	ns
512 FSO:						
Frequency		fCLK	4.096	-	24.576	MHz
Pulse Width Low		tCLKL	20	-	-	ns
Pulse Width High		tCLKH	20	-	-	ns
Channel Clock for Input Port (ILRCK)						
Frequency						
Normal speed Mode		FSIN	8	-	54	kHz
Double speed Mode		FSID	54	-	108	kHz
Quad speed Mode		FSIQ	108	-	192	kHz
Duty Cycle		dILRCK	48	50	52	%
Channel Clock for Output Port (OLRCK)						
Slave Mode						
Frequency	(FSI: 8kHz~192kHz)	FSO	44.1	-	48	kHz
Frequency	(FSI: 8kHz, 16kHz, 24kHz)	FSO	8	-	24	kHz
Duty Cycle		dOLRCK	48	50	52	%
Master Mode						
Frequency	(FSI: 8kHz~192kHz)	FSO	44.1	-	48	kHz
Frequency	(FSI: 8kHz, 16kHz, 24kHz)	FSO	8	-	24	kHz
Duty Cycle		dOLRCK	-	50	-	%

■ Timing

(Ta=-40~ +105°C; DVDD=3.0~3.6V at VSEL pin="L" or DVDD=VD18=1.7V~1.9V at VSEL pin="H"; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max	Unit
Audio Interface Timing					
Input PORT					
IBICK Period Normal speed Mode	tIBCK	1/256 FSIN	-	-	ns
Double speed Mode	tIBCK	1/128 FSID	-	-	ns
Quad speed Mode	tIBCK	1/64 FSIQ	-	-	ns
IBICK Pulse Width Low	tIBCKL	27	-	-	ns
IBICK Pulse Width High	tIBCKH	27	-	-	ns
ILRCK Edge to IBICK "↑" (* 13)	tILRB	15	-	-	ns
IBICK "↑" to ILRCK Edge (* 13)	tIBLR	15	-	-	ns
SDTI Hold Time from IBICK "↑"	tISDH	15	-	-	ns
SDTI Setup Time to IBICK "↑"	tISDS	15	-	-	ns
Output PORT (Slave Mode)					
OBICK Period Normal speed Mode	tOBCK	1/256 FSON	-	-	ns
OBICK Pulse Width Low	tOBCKL	27	-	-	ns
OBICK Pulse Width High	tOBCKH	27	-	-	ns
OLRCK Edge to OBICK "↑" (* 13)	tOLRB	20	-	-	ns
OBICK "↑" to OLRCK Edge (* 13)	tOBLR	20	-	-	ns
OLRCK to SDTO(MSB) (Except I^2S Mode)	tOLRS	-	-	20	ns
OBICK "↓" to SDTO	tOBSD	-	-	20	ns
Output PORT (Master Mode)					
OBICK Frequency	fOBCK	-	64 FSO	-	Hz
OBICK Duty	dOBCK	-	50	-	%
OBICK "↓" to OLRCK Edge	tOMBLR	-20	-	20	ns
OBICK "↓" to SDTO	tOBSD	-20	-	20	ns
Reset Timing					
PDN Pulse Width (* 14)	tPD	150	-	-	ns
PDN pin Pulse Width of Spike Noise Suppressed by Input Filter (* 15)	tPDS	0	-	50	ns

Notes:

* 13. BICK rising edge must not occur at the same time as LRCK edge.
* 14. The AK4133 can be rest by bringing the PDN pin = "L".
* 15. Spike noise width of "L" pulse suppressed by input filter of the PDN pin.

■ Timing Diagram

Master Clock

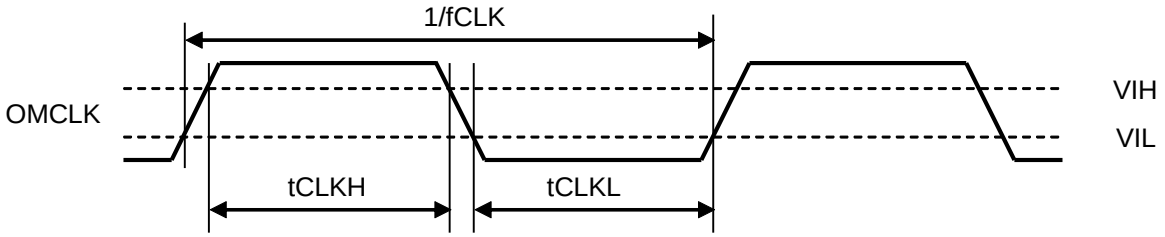


Figure 3. OMCLK Clock Timing

Input Port Clock

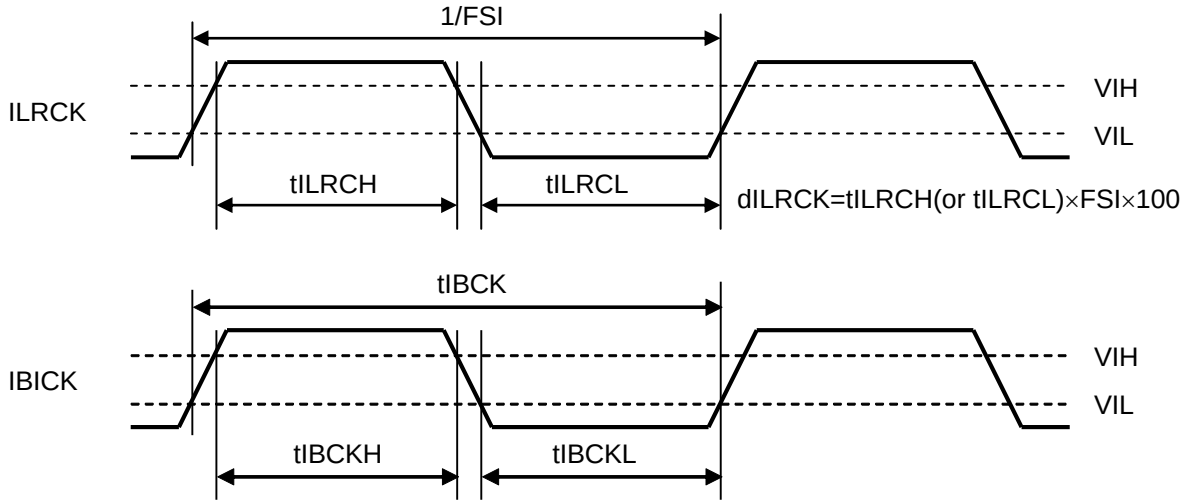


Figure 4. ILRCK, IBICK Clock Timing

Input Port Timing

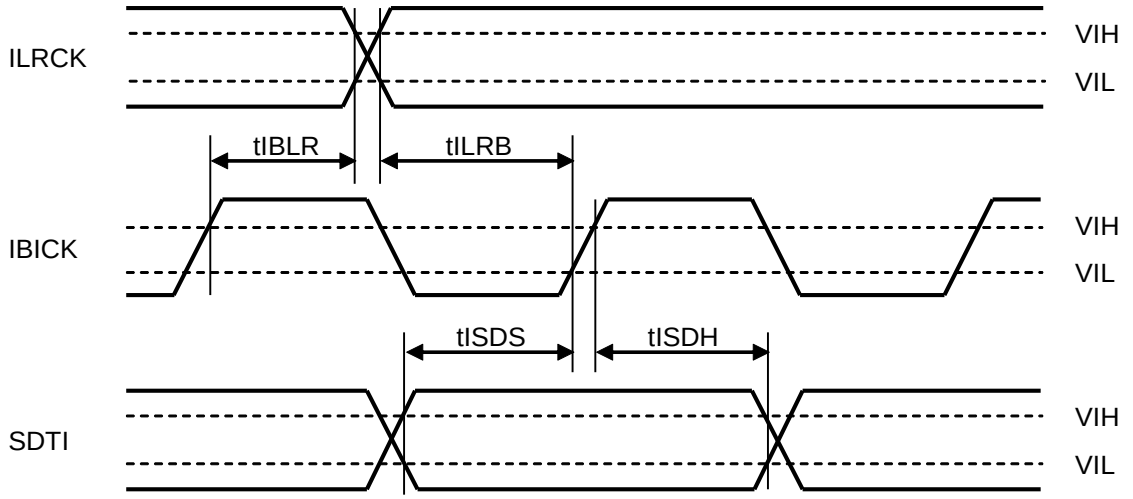


Figure 5. Input PORT Audio Interface Timing (Slave Mode)

Output Port Clock (Slave Mode)

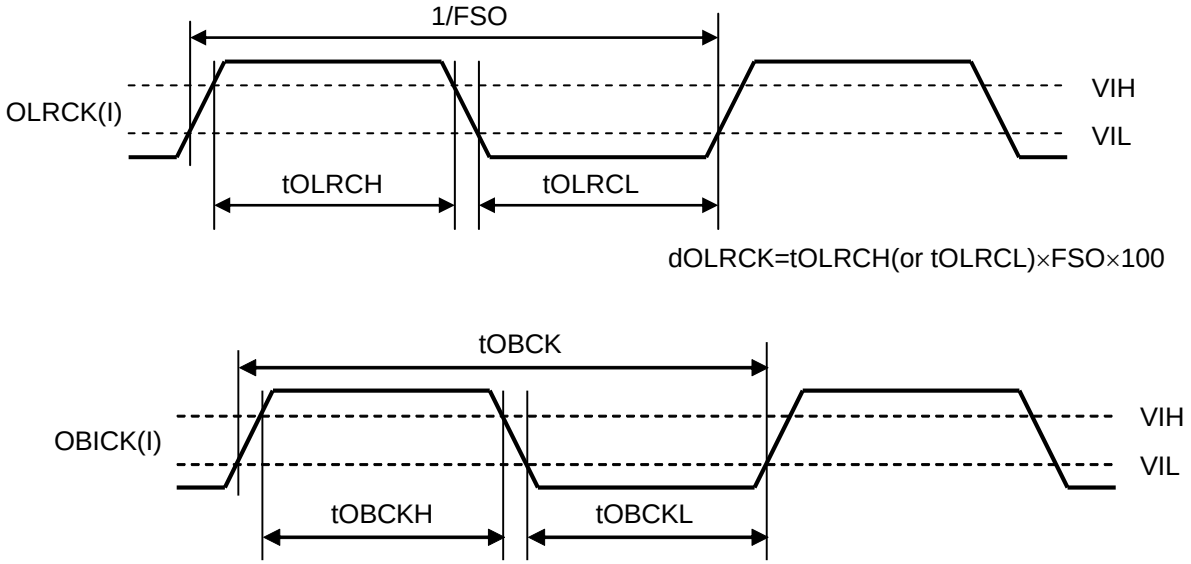


Figure 6. OLRCK, OBICK Clock Timing (Slave Mode)

Output Port Timing (Slave Mode)

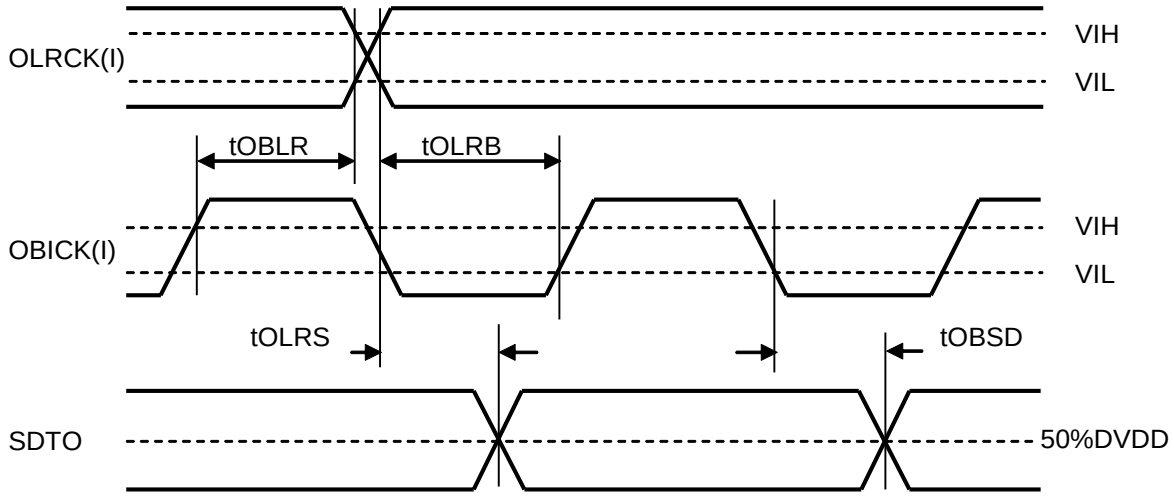


Figure 7. Output PORT Audio Interface Timing (Slave Mode)

Output Port Clock (Master Mode)

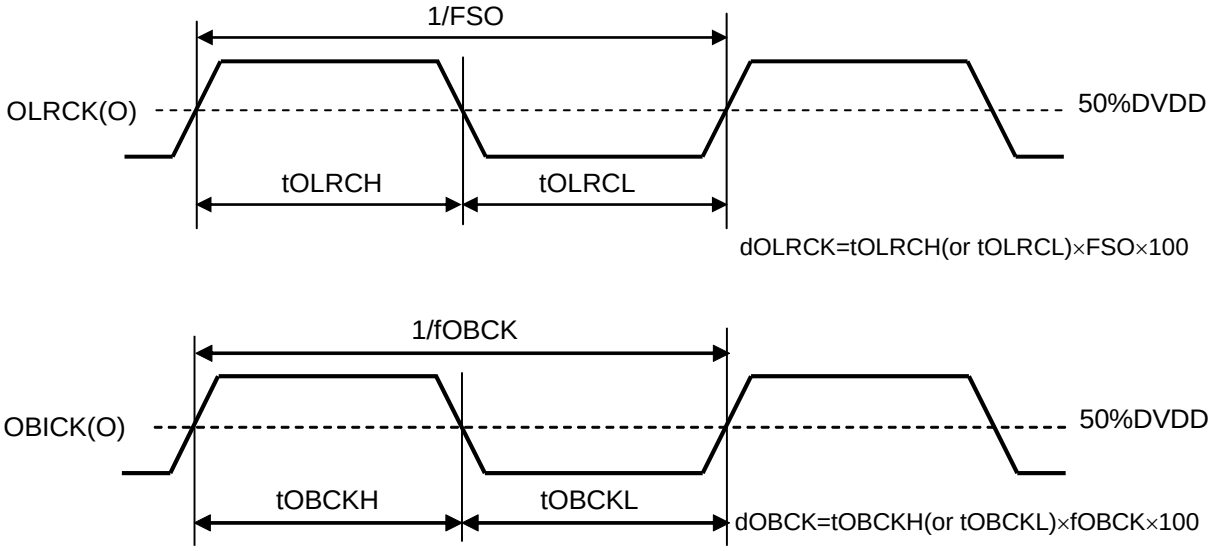


Figure 8. OLRCK, OBICK Clock Timing (Master Mode)

Output Port Timing (Master Mode)

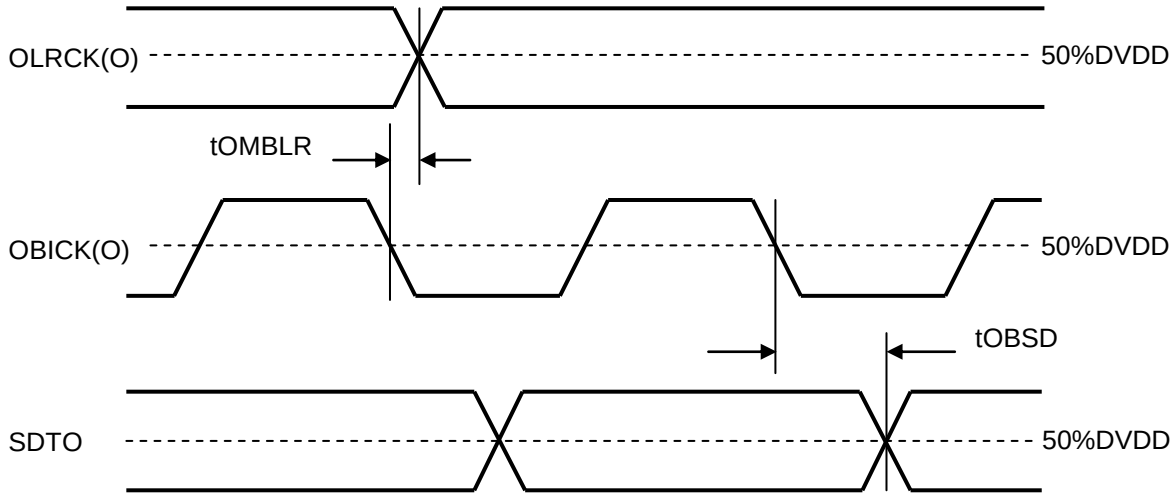


Figure 9. Output PORT Audio Interface Timing (Master Mode)

Power-down Timing

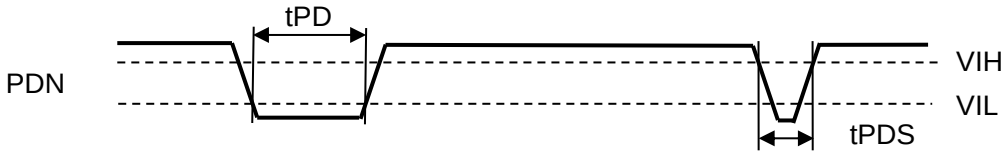


Figure 10. Power Down and Reset Pulse

13. Functional Description

■ Input and Output sampling rate combination

The table below shows the possible combination of the input sampling rate and output sampling rate.

Table 1. Combinations of FSI and FSO

FSI [kHz]	FSO [kHz]								
	8	11.025	12	16	22.05	24	32	44.1	48
8	Y	-	-	Y	-	Y	-	Y	Y
11.025	-	-	-	-	-	-	-	Y	Y
12	-	-	-	-	-	-	-	Y	Y
16	Y	-	-	Y	-	Y	-	Y	Y
22.05	-	-	-	-	-	-	-	Y	Y
24	Y	-	-	Y	-	Y	-	Y	Y
32	-	-	-	-	-	-	-	Y	Y
44.1	-	-	-	-	-	-	-	Y	Y
48	-	-	-	-	-	-	-	Y	Y
88.2	-	-	-	-	-	-	-	Y	Y
96	-	-	-	-	-	-	-	Y	Y
176.4	-	-	-	-	-	-	-	Y	Y
192	-	-	-	-	-	-	-	Y	Y

Y: Available
-: Not Available

■ System Clock and Audio Interface Format for Input Port

The audio interface format is controlled by the IDIF pin. The data format is MSB first in 2's complement. The SDTI input data is clocked in on a rising edge of the IBICK. The audio interface format of the input port should be changed while the PDN pin = “L”.

Table 2. Input PORT Audio Interface Format

Mode	IDIF Pin	SDTI Format	ILRCK	IBICK	IBICK Frequency
0	L	24-bit, MSB justified	Input	Input	256FSI≥ or ≥ 64FSI
1	H	24 or 16-bit, I^2S Compatible			256FSI≥ or ≥ 64FSI
		16-bit, I^2S Compatible			32FSI (* 16)

Note:
* 16. When IBICK = 32FSI, only 16-bit I^2S Compatible is supported.

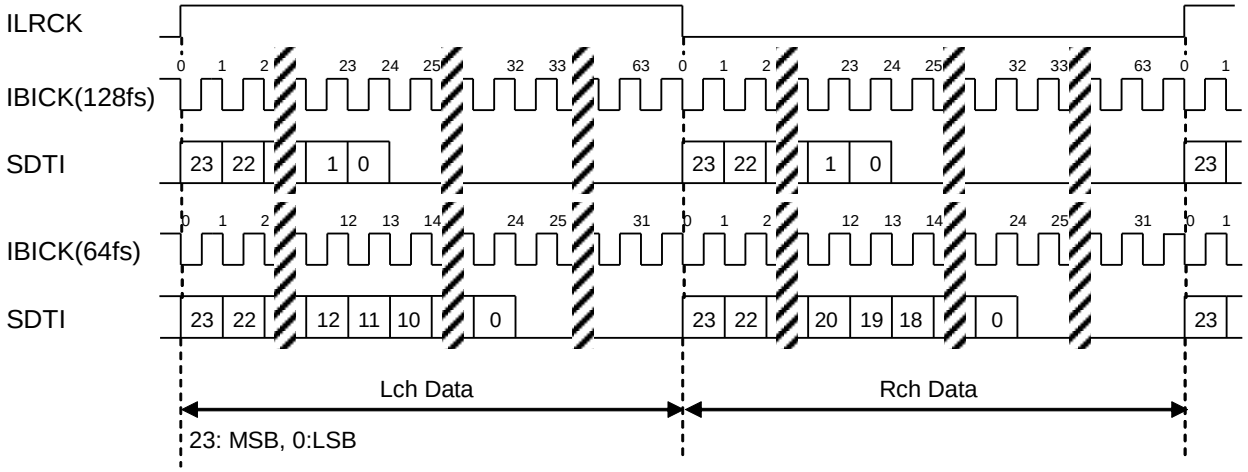


Figure 11. Mode0 Timing (24-bit MSB)

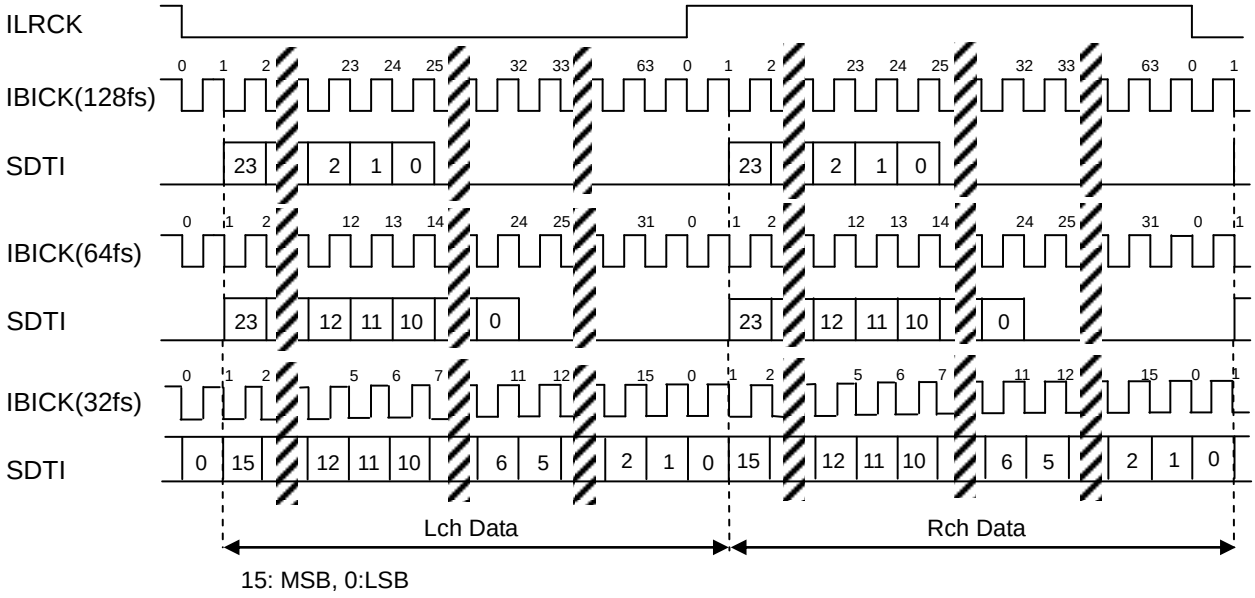


Figure 12. Mode1 Timing (24-bit/16-bit I^2S)

■ System Clock for Output PORT

The output ports work in both master mode and slave mode. In master mode, the output port is operated with OLRCK and OBICK generated from OMCLK. OLRCK and OBICK clocks are output from the OLRCK pin and OBICK pin, respectively. In slave mode, the output port is operated by input clocks from the OLRCK pin and the OBICK pin. The OMCLK pin is not used in slave mode. It must be connected to DVSS.

The CM1-0 pins select master or slave mode.

Table 3. Output PORT Master/Slave Mode Control (AK4133)

Mode	CM1 pin	CM0 pin	Master / Slave	OMCLK Frequency
0	L	L	Master	256FSO
1	L	H	Slave	Not used. (* 17)
2	H	L	Master	512FSO
3	H	H	Master	128FSO

Note:
* 17. The OMCLK pin must be connected to DVSS in slave mode.

■ Audio Interface Format of the Output Port

The ODIF pin controls the audio interface mode of the output port. The data format is MSB first in 2's complement. The data is output on a falling edge of OBICK from the SDTO pin. The audio interface format of the output port should be changed while the PDN pin = “L”.

Table 4. Output PORT Audio Interface Format

Mode	ODIF pin	SDTO Format	OBICK (Slave)	OBICK (Master)
0	L	MSB justified	≥ 48fs or 32fs	64fs
1	H	I^2S Compatible	≥ 48fs or 32fs	64fs

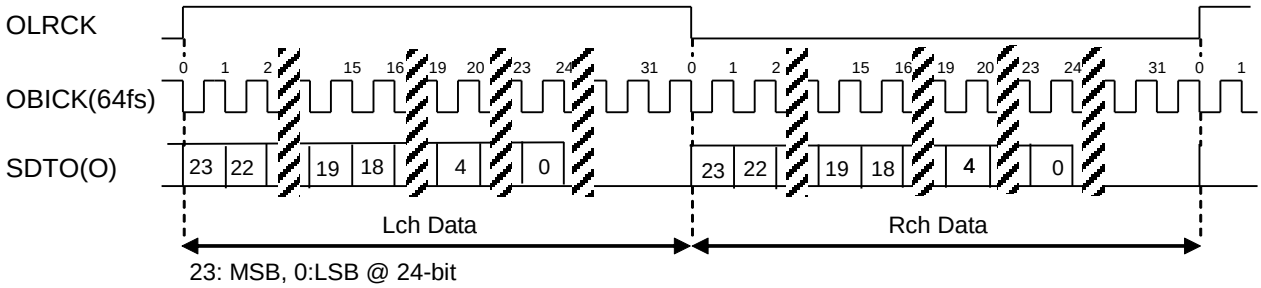


Figure 13. Mode 0 MSB Justified Timing

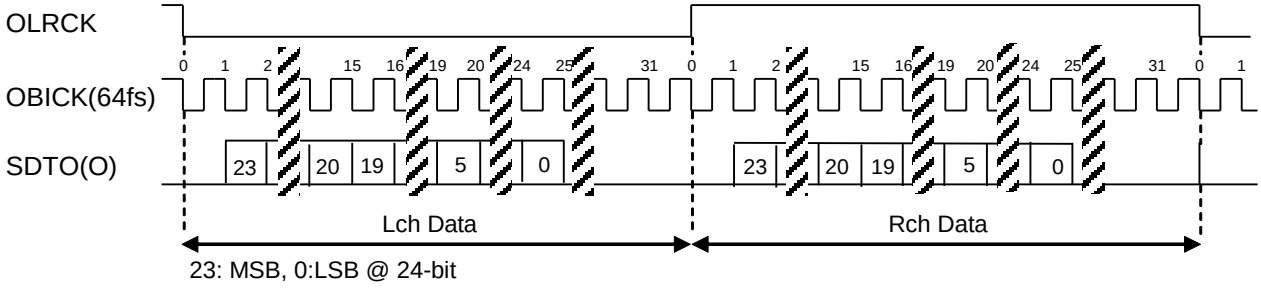


Figure 14. Mode1 I^2S Compatible Timing

■ Soft Mute Function

The AK4133 has soft mute function. Soft mute operation is controlled by the SMUTE pin. If the SMUTE pin is set to “H”, the SRC output data is attenuated to −∞dB (“0”) in 1024 OLRCK cycles. When the SMUTE pin is returned to “L”, the mute is cancelled and the output attenuation level gradually changes to 0dB in 1024 OLRCK cycles. If the soft mute is cancelled before attenuating to −∞dB after starting soft mute operation, attenuation is discontinued and the attenuation level is returned to 0dB by the same cycle. Soft mute is effective for changing the signal source without stopping the signal transmission.

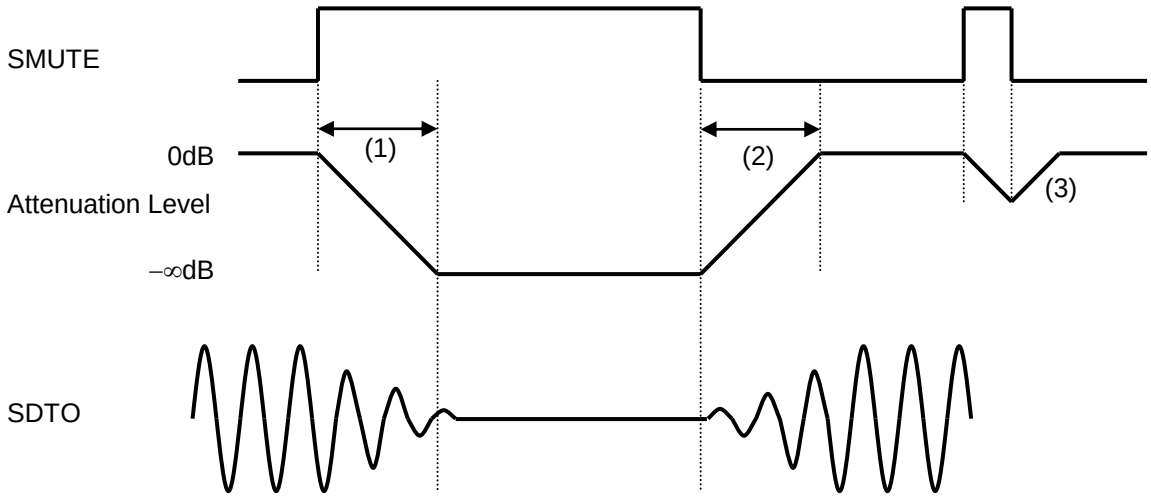


Figure 15. Soft Mute

(1) The output data is attenuated to −∞ (“0”) in 1024 OLRCK cycles by setting the SMUTE pin= “H”.
(2) The attenuation level returns to 0dB in 1024 OLRCK cycles by setting the SMUTE pin= “L”.
(3) If the soft mute is cancelled within 1024 OLRCK cycles, attenuation is discontinued and the attenuation level is returned to 0dB by the same cycle.

■ Regulator

The AK4133 has an internal regulator which suppresses the voltage to 1.8V from DVDD (3.3V). The generated 1.8V power is used as power supply for internal circuit. When over-current is flowed to the regulator output, over-current detection circuit works. When over-voltage is flowed to the regulator output, over-voltage detection circuit works. The regulator block is powered-down and the AK4133 becomes reset state when over-current detection circuit or over-voltage detection circuit is operated. The AK4133 does not return to normal operation without a reset by the PDN pin when these detection circuits are worked. When over-current or over-voltage is detected, the PDN pin should be brought into “L” at once, and should be set to “H” again to recover normal operation.

The SRCE_N pin indicates the internal status of the device. It outputs “L” in SRC normal operation, and outputs “H” when over-current or over-voltage is detected.

■ Power Supply

The AK4133 supports 1.8V and 3.3V power supply voltages. Set the VSEL pin according to applying voltage. The VSEL pin should be set to “L” when using a 3.3V power supply. The internal regulator is turned ON and 1.8V power for internal circuits will be generated using 3.3V power from the DVDD pin. The VSEL pin should be set to “H” when using a 1.8V power supply. The internal regulator is turned OFF and the V18 pin becomes power supply pin for internal circuits.

■ System Reset

Bringing the PDN pin = “L” sets the AK4133 power-down mode and initializes the digital filters. The AK4133 should be reset once by bringing the PDN pin to “L” upon power-up. The internal SRC circuit is powered-up on ILRCK and OLRCK input after a power-up period of the internal regulator (PDN pin = “H”). The data output time of the SDTO pin depends on the LRCK and OLRCK input when the PDN pin = “H”. (Figure 16, Figure 17)

Case 1: ILRCK and OLRCK are input when the PDN pin= “H”

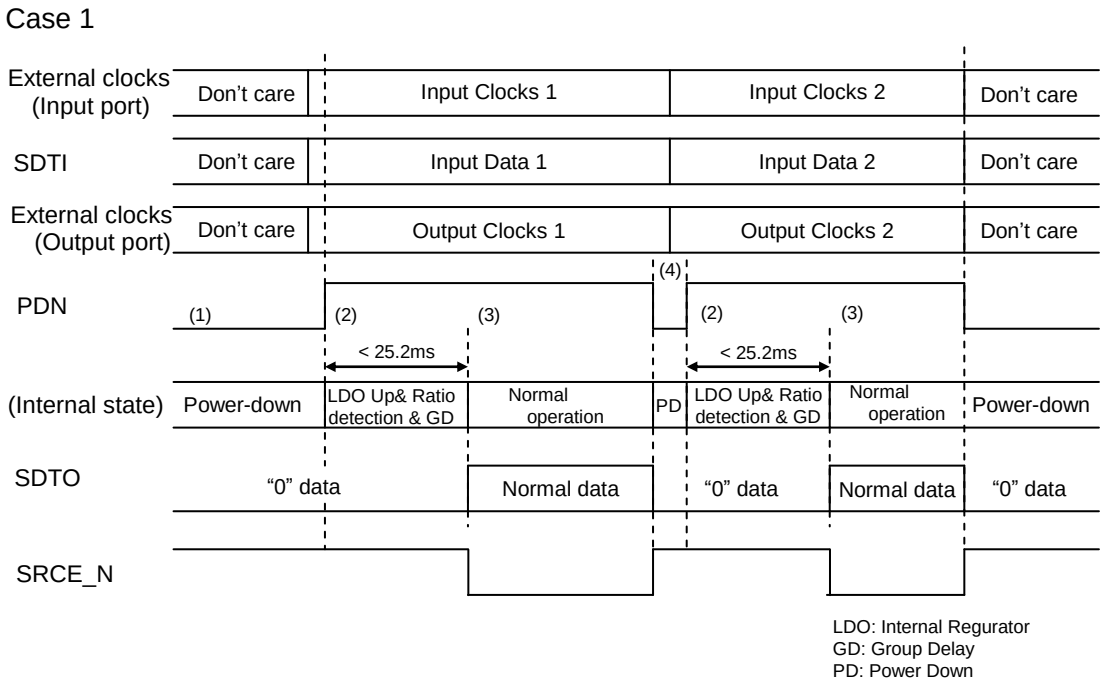


Figure 16. System Reset Case1

(1) The SDTO pin outputs “L” and the SRCE_N pin outputs “H” when the PDN pin= “L”.
(2) The Internal regulator is powered up by bringing the PDN pin = “H” after operation clock is input. Then, SRC circuit is powered up and starts Ratio detection by ILRCK and OLTCK. SDTO is output after group delay period when Ratio detection is completed. Until then the SDTO outputs “L” and the SRCE_N pin outputs “H”. The time until SDTO output become enabled after setting the PDN pin to “H” is 25.2msec (Max.).
(3) The SRCE_N pin outputs “L” when SDTO data output becomes enabled.
(4) The statuses of the CM1-0, ODIF and IDIF pins should be changed while the PDN pin= “L”.

Case2: ILRCK and OLRCK are not input when the PDN pin= “H”

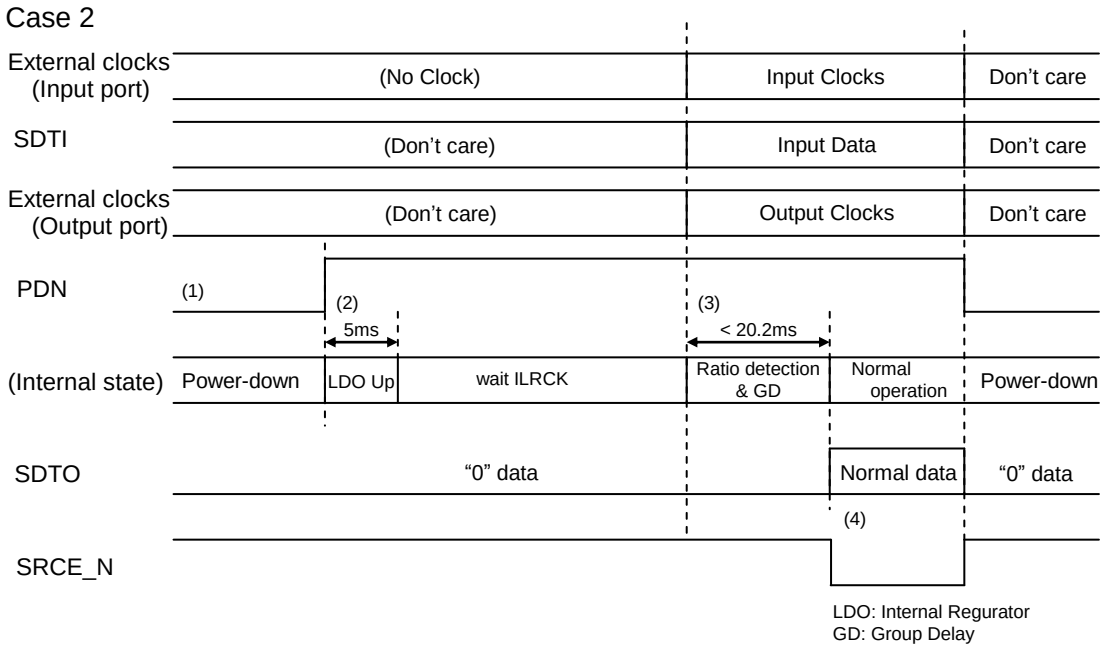


Figure 17. System Reset Case2

(1) The SDTO pin outputs “L” and the SRCE_N pin outputs “H” when the PDN pin= “L”.
(2) The internal regulator is powered up by PDN pin = “H” and wait for ILRCK and OLRCK.
(3) SRC circuit is powered up and sampling frequency ratio detection starts when ILRCK and OLRCK are input. SDTO output starts after group delay period when the frequency ratio detection is completed. Until then, the SDTO output is “L” and the SRCE_N pin outputs “H”. The time until SDTO output becomes enabled after ILRCK and OLPCK input is 20.2msec (Max.).
(4) The SRCE_N pin outputs “L” when SDTO data output becomes enabled.

■ Clock Switch Sequence

The AK4133 must be reset by bringing the PDN pin to “L” when changing operation clocks. Clock change sequence is shown in Figure 18.

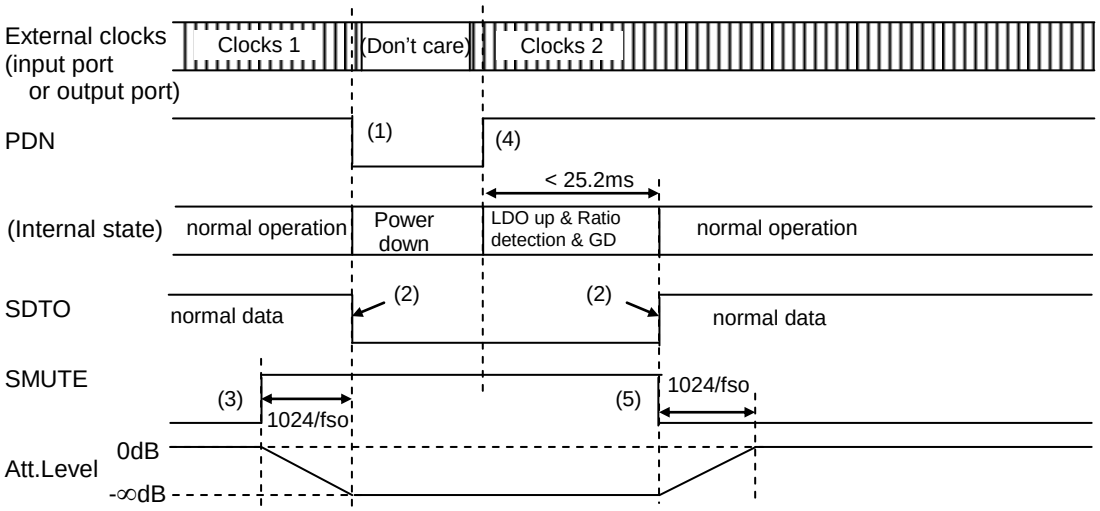


Figure 18. Clock Change Sequence

(1) Set the PDN pin to “L”, and change clock frequencies of the IDIF pin, ODIF pin and CM1-0 pins.
(2) Click noise may occur when the STDO output is changed.
(3) Mute the SDTO output by setting the SMUTE pin to “H” before setting the PDN pin to “L” if the click noise influences system applications. This click noise can also be prevented by setting “0” to the SDTI from GD before the PDN pin changes to “L”. It makes the data on SDTO remain as “0”.
(4) Set the PDN pin to “H” after changing the clock of the IDIF pin, ODIF pin or CM1-0 pins.
(5) Set the SMUTE pin to “L” to release the soft mute if the soft mute function is enabled.

The AK4133 has automatic internal reset function for when ILRCK or OLRCK frequency is changed. The behavior of the device when ILRCK or OLRCK frequency is changed is shown below.

▪ When the frequency of ILRCK at input port is changed without a reset by the PDN pin.

When the difference of internal oscillator clock number in one ILRCK cycle between before and after changing ILRCK frequency (FSO/FSI ratio should be stabilized) is more than 1/16 for 8cycles (*), an internal reset is made automatically and sampling frequency ratio detection is executed again.
The SDTO pin outputs “L” when the internal reset is made, and SRC data is output after 162FSI(O) (FSI(O) is lower frequency between FSI and FSO).

When the above condition (*) is not satisfied, the internal reset mentioned before will not be executed. It takes 5148/FSO (max. 643.5ms@FSO=8kHz) (* 18) to output normal SRC data. Distorted data may be output until normal SRC output.

When ILRCK is stopped, an internal reset is executed automatically. It takes 162FSI(O) (FSI(O) is lower frequency between FSI and FSO) to output normal SRC data after ILRCK is input again.

▪ When the frequency of OLRCK at output port is changed without a reset by the PDN pin

When the difference of internal oscillator clock number in one OLRCK cycle between before and after changing OLRCK frequency (FSO/FSI ratio should be stabilized) is more than 1/16 for 8cycles (*), an internal reset is made automatically and sampling frequency ratio detection is executed again. SDTO outputs “L” when the internal reset is made, and SRC data is output after 162FSI(O) (FSI(O) is lower frequency between FSI and FSO).

When the above condition (*) is not satisfied, the internal reset mentioned before will not be executed. It takes 5148/FSO (max. 643.5ms@FSO=8kHz) (* 18) to output normal SDTO data. Distorted data may be output until normal SDTO output.

When OLRCK is stopped, an internal reset is executed automatically. It takes 162FSI(O) (FSI(O) is lower frequency between FSI and FSO) [sec] to output normal SDTO data after ILRCK is input again.

Notes:
* 18. When FSO=8kHz and FSO/FSI ratio is changed from 1/6 to 1/5.99.

■ Internal Status Pin

The SRCE_N pin outputs internal state of the device. It outputs “H” while the PDN pin = “L”.
SRC data is output from the SDTO pin when the PDN pin = “H” and the sampling frequency ratio detection is completed if the internal regulator is operated normally.

An internal limit flag is set when an over current or over voltage flows at the internal regulator. An ORed result of the internal limit flag and an inverted flag of the ratio detection completion of SRC is output from the SRCE_N pin.

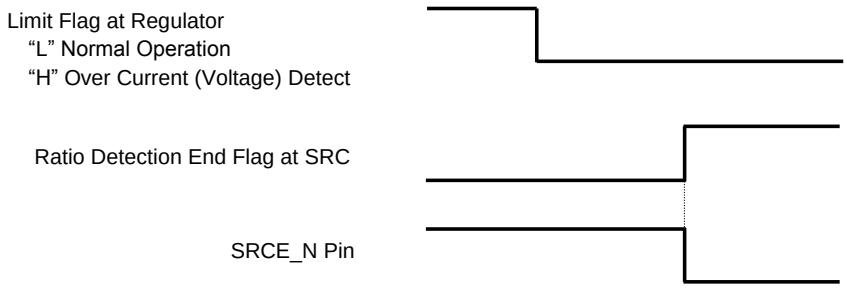


Figure 19. Internal Flag and SRCE_N Pin Output

■ Grounding ans Power Supply Decoupling

The AK4133 requires careful attention to power supply and grounding arrangements. Decoupling capacitors should be placed as near as possible to the supply pins.

14. Jitter Tolerance

Figure 20 shows the jitter tolerance to ILRCK and IBICK. The jitter quantity is defined by the jitter frequency and the jitter amplitude. When the jitter amplitude is 0.02UIpp or less, the AK4133 operates normally regardless of the jitter frequency.

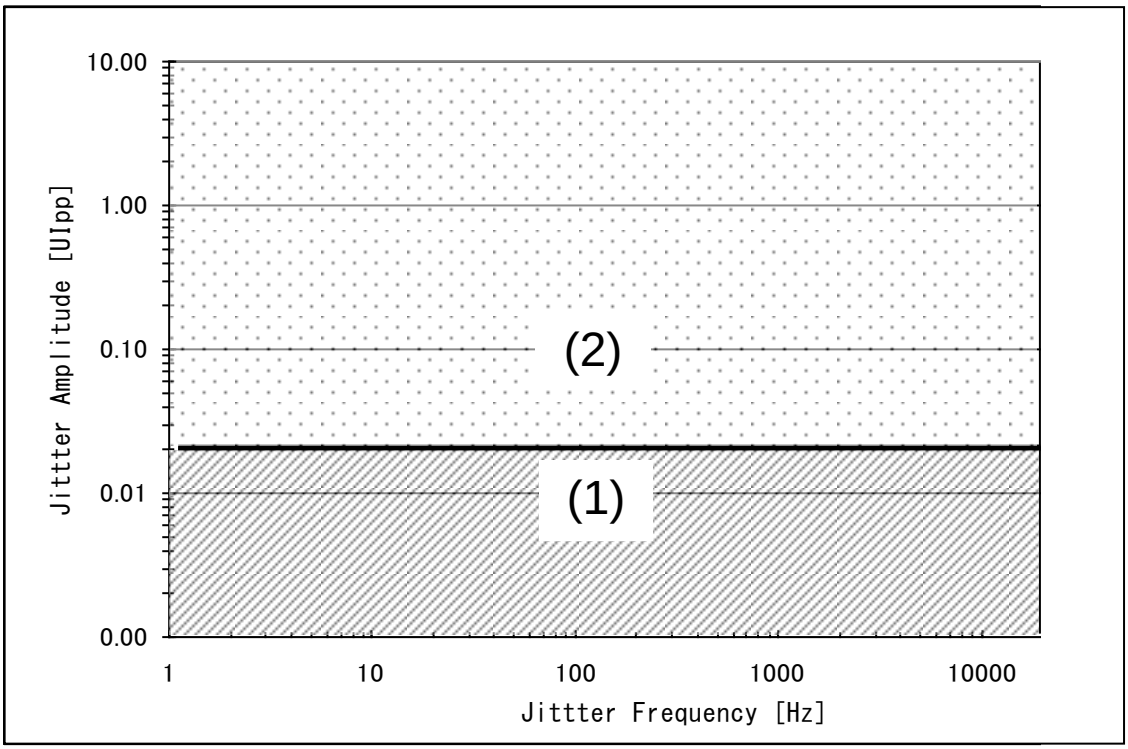


Figure 20. Jitter Tolerance

This is an evaluation result with synchronous input data to ILRCK and IBICK when jitter is added.
The area (1) and (2) border is the the jitter amplitude of ILRCK just before THD+N degradation starts.
Please use the jitter amplitude of the area (1).

(1) Normal Operation
(2) There is a possibility that the output data is lost.

1UI (Unit Interval) is one cycle of IBICK. 1[UIpp] = 1/48kHz = 20.8μsec when FSI is 48kHz.

15. Recommended External Circuits

Figure 21 and Figure 22 show the system connection diagram.

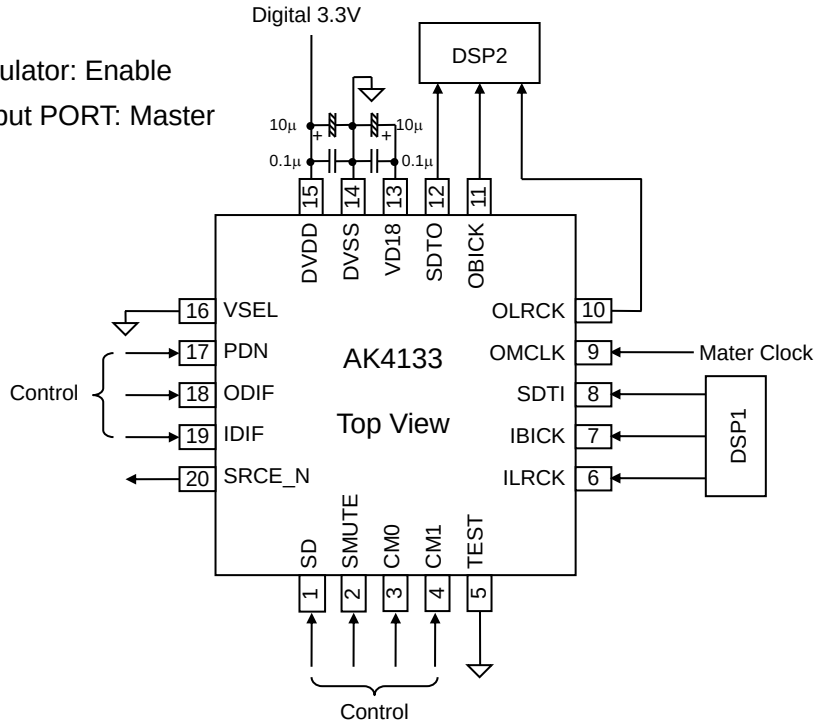


Figure 21. Typical Connection Diagram (Output Port: Master Mode, Regulator: Enable)

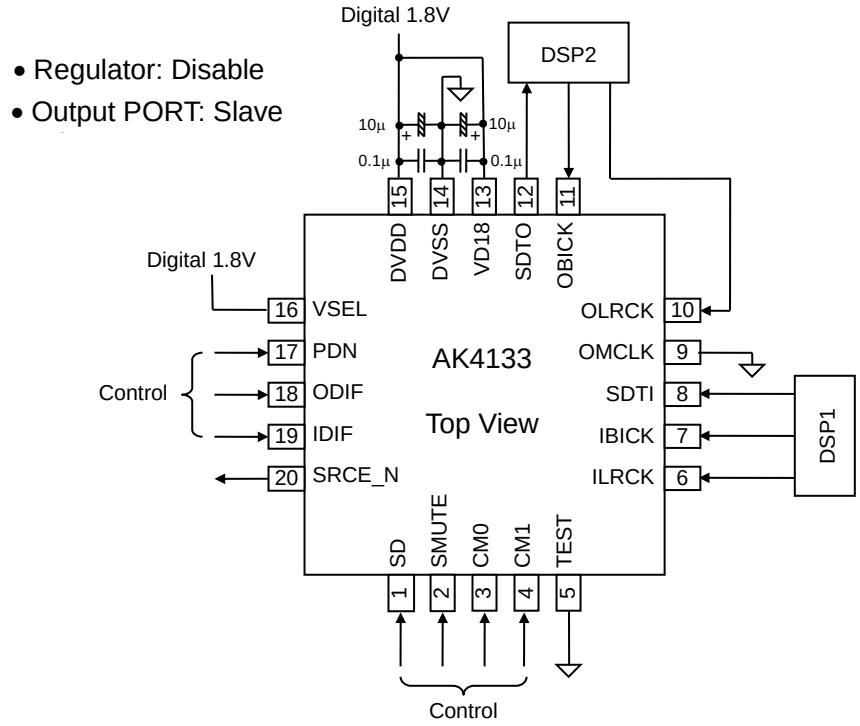
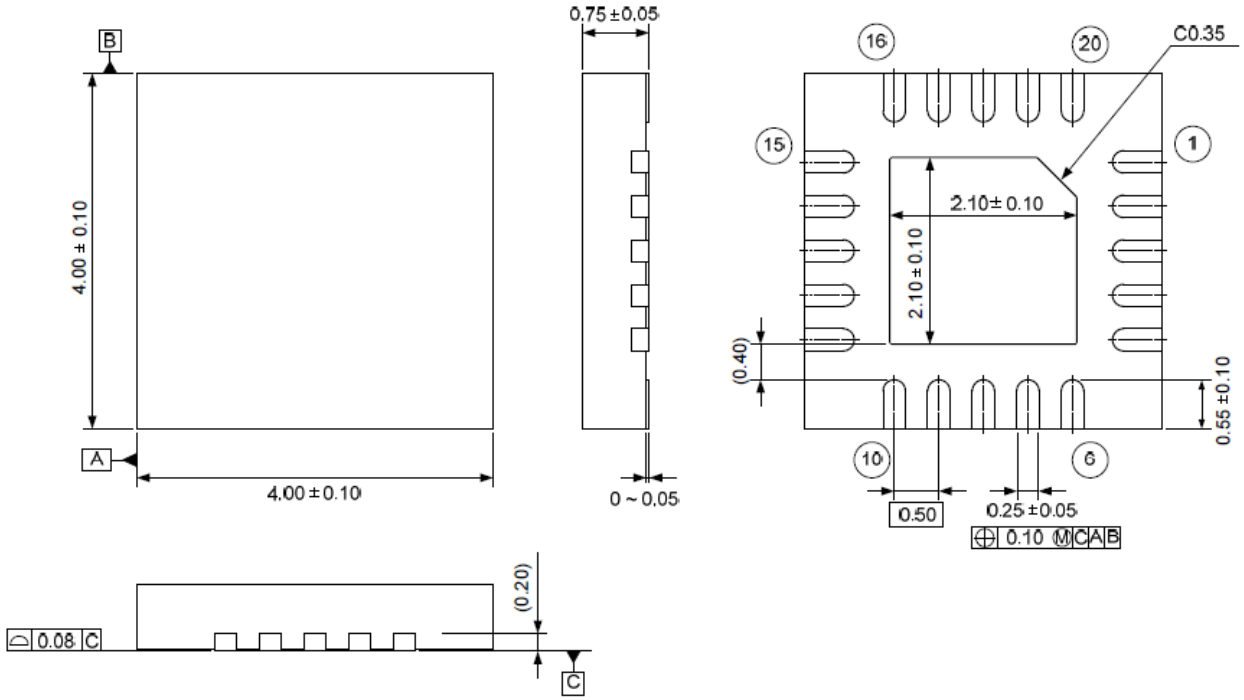


Figure 22. Typical Connection Diagram (Output Port: Slave Mode, Regulator: Disable)

16. Package

■ Outline Dimenstions

20-pin QFN (Unit: mm)

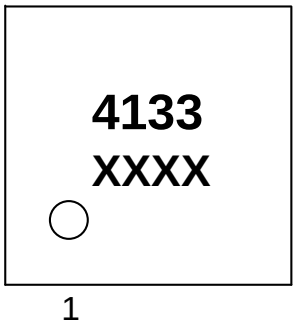


* 19. The exposed pad on the bottom surface of the package must be open or connected to DVSS.

■ Material & Lead Finish

Package Molding Compound:	Epoxy
Lead Frame Material:	Cu
Pin Surface Treatment:	Solder (Pb free) Plate

■ Marking



1) Pin #1 indication
2) Date Code : XXXX (4 digits)
3) Marketing Code : 4133

17. Ordering Guide

AK4133VN	−40 ~ 105ºC	20-pin QFN (0.5mm pitch)
AKD4132	Evaluation Board for AK4132	

18. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
15/12/09	00	First Edition		
16/06/20	01	Spec. Added	1	General Description “It is possible also to convert 8kHz, 16kHz or 24kHz into 8kHz, 16kHz or 24kHz.” added
16/06/20	01	Spec. Added	1	Features Output Sample Rate (FSO): 8kHz, 16kHz, 24kHz (@FSI: 8kHz, 16kHz, 24kHz) added.
16/06/20	01	Spec. Added	6	SRC Characteristics “Output Sample Rate (FSI: 8kHz,16kHz, 24kHz) min. 8kHz, max. 24kHz” added
16/06/20	01	Spec. Added	10	Switching Characteristics Master Clock Input (OMCLK) 128 FSO: min.5.6448MHz → min. 1.024MHz 256 FSO: min.11.2896MHz → min. 2.048MHz 512 FSO: min.22.5792MHz → min. 4.096MHz
16/06/20	01	Spec. Added	10	Switching Characteristics Channel Clock for Output Port (OLRCK) Slave Mode “Frequency (FSI: 8kHz, 16kHz, 24kHz) min.8kHz, max. 24kHz” added Master Mode Frequency (FSI: 8kHz, 16kHz, 24kHz) “min.8kHz, max. 24kHz” added
16/06/20	01	Spec. Added	15	Functional Description ”■Input and Output sampling rate combination” added.
16/06/20	01	Spec. Added	17	■ System Clock for Output PORT The FSO column deleted from Table 3 “Output PORT Master/Slave Mode Control”. (FSO has no meaning in Table 3.)
16/06/20	01	Spec. Added	19	■ System Reset Figure 16 LDO up & Ratio detection & GD 9.6ms → 25.2ms
16/06/20	01	Spec. Added	20	■ System Reset Figure 17 Ratio detection & GD 4.6ms → 20.2ms

Date (Y/M/D)	Revision	Reason	Page	Contents
16/06/20	01	Spec. Added	21	■ Clock Switch Sequence Figure 18 LDO up & Ratio detection & GD 9.6ms → 25.2 ms Description (Max. 116.7ms@FSO=44.1kHz) → (Max. 643ms@FSO=8kHz)
16/06/20	01	Spec. Added	22	■ Clock Switch Sequence Description (Max. 116.7ms@FSO=44.1kHz) → (Max. 643ms@FSO=8kHz)

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