

|                                                                                           |                                    |
|-------------------------------------------------------------------------------------------|------------------------------------|
|          | <h1 style="margin: 0;">AK4114</h1> |
| <h2 style="margin: 0;">High Feature 192kHz 24bit Digital Audio Interface Transceiver</h2> |                                    |

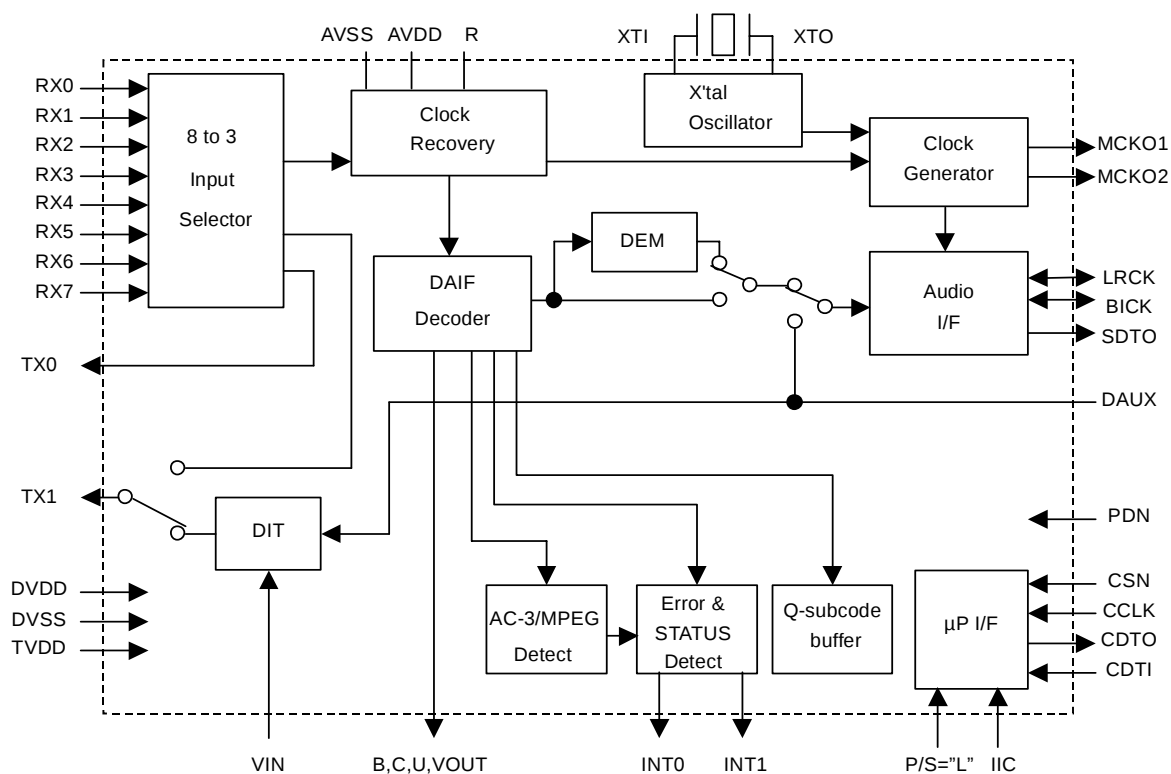
### GENERAL DESCRIPTION

The AK4114 is a digital audio transceiver supporting 192kHz, 24bits. The channel status decoder supports both consumer and professional modes. The AK4114 can automatically detect a Non-PCM bit stream. When combined with the multi channel codec (AK4527B or AK4529), the two chips provide a system solution for AC-3 applications. The dedicated pins or a serial  $\mu$ P I/F can control the mode setting. The small package, 48pin LQFP saves the system space.

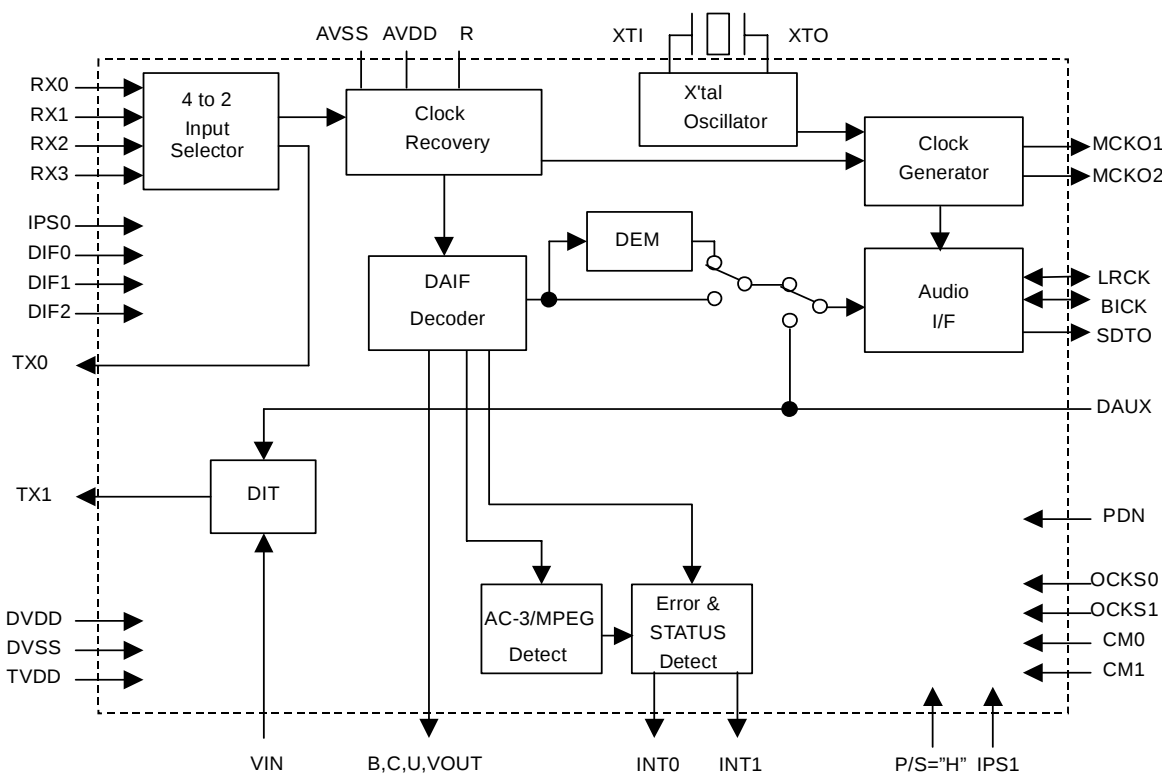
\*AC-3 is a trademark of Dolby Laboratories.

### FEATURES

- ☐ AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible
- ☐ Low jitter Analog PLL
- ☐ PLL Lock Range : 32kHz to 192kHz
- ☐ Clock Source: PLL or X'tal
- ☐ 8-channel Receiver input
- ☐ 2-channel Transmission output (Through output or DIT)
- ☐ Auxiliary digital input
- ☐ De-emphasis for 32kHz, 44.1kHz, 48kHz and 96kHz
- ☐ Detection Functions
  - Non-PCM Bit Stream Detection
  - DTS-CD Bit Stream Detection
  - Sampling Frequency Detection  
(32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz)
  - Unlock & Parity Error Detection
  - Validity Flag Detection
- ☐ Up to 24bit Audio Data Format
- ☐ Audio I/F: Master or Slave Mode
- ☐ 40-bit Channel Status Buffer
- ☐ Burst Preamble bit Pc and Pd Buffer for Non-PCM bit stream
- ☐ Q-subcode Buffer for CD bit stream
- ☐ Serial  $\mu$ P I/F
- ☐ Two Master Clock Outputs: 64fs/128fs/256fs/512fs
- ☐ Operating Voltage: 2.7 to 3.6V with 5V tolerance
- ☐ Small Package: 48pin LQFP
- ☐ Ta: -10 to 70°C



Serial Control Mode

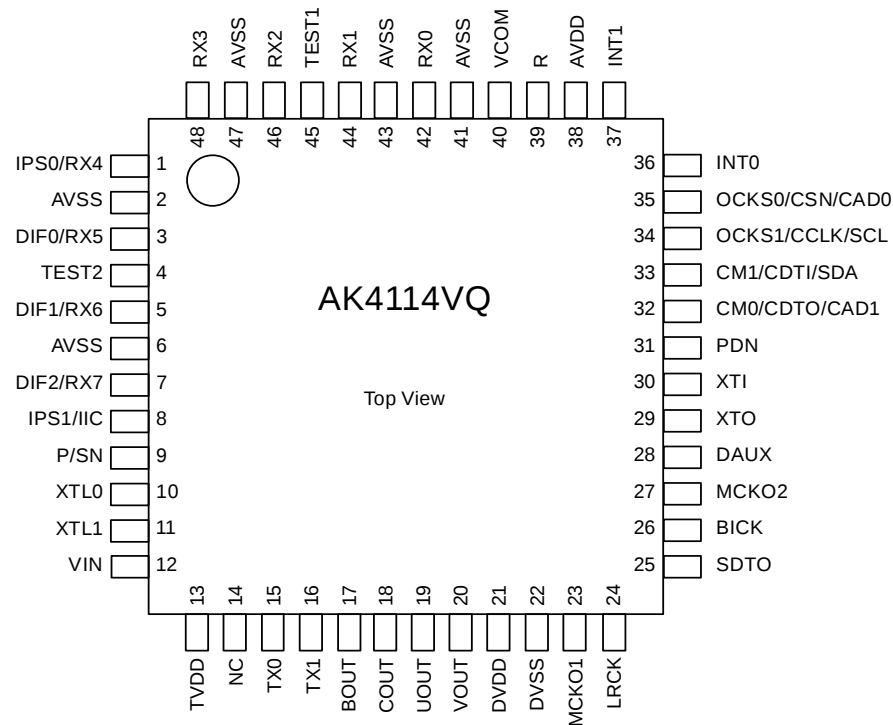


Parallel Control Mode

■ Ordering Guide

AK4114VQ      -10 ~ +70 °C      48pin LQFP (0.5mm pitch)

■ Pin Layout



| PIN/FUNCTION |          |     |                                                                                                                                           |
|--------------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------|
| No.          | Pin Name | I/O | Function                                                                                                                                  |
| 1            | IPS0     | I   | Input Channel Select 0 Pin in Parallel Mode                                                                                               |
|              | RX4      | I   | Receiver Channel 4 Pin in Serial Mode (Internal biased pin)                                                                               |
| 2            | NC(AVSS) | I   | No Connect<br>No internal bonding. This pin should be connected to AVSS.                                                                  |
| 3            | DIF0     | I   | Audio Data Interface Format 0 Pin in Parallel Mode                                                                                        |
|              | RX5      | I   | Receiver Channel 5 Pin in Serial Mode (Internal biased pin)                                                                               |
| 4            | TEST2    | I   | TEST 2 pin<br>This pin should be connect to AVSS.                                                                                         |
| 5            | DIF1     | I   | Audio Data Interface Format 1 Pin in Parallel Mode                                                                                        |
|              | RX6      | I   | Receiver Channel 6 Pin in Serial Mode (Internal biased pin)                                                                               |
| 6            | NC(AVSS) | I   | No Connect<br>No internal bonding. This pin should be connected to AVSS.                                                                  |
| 7            | DIF2     | I   | Audio Data Interface Format 2 Pin in Parallel Mode                                                                                        |
|              | RX7      | I   | Receiver Channel 7 Pin in Serial Mode (Internal biased pin)                                                                               |
| 8            | IPS1     | I   | Input Channel Select 1 Pin in Parallel Mode                                                                                               |
|              | IIC      | I   | IIC Select Pin in Serial Mode.<br>“L”: 4-wire Serial, “H”: IIC                                                                            |
| 9            | P/SN     | I   | Parallel/Serial Select Pin<br>“L”: Serial Mode, “H”: Parallel Mode                                                                        |
| 10           | XTL0     | I   | X'tal Frequency Select 0 Pin                                                                                                              |
| 11           | XTL1     | I   | X'tal Frequency Select 1 Pin                                                                                                              |
| 12           | VIN      | I   | V-bit Input Pin for Transmitter Output                                                                                                    |
| 13           | TVDD     | I   | Input Buffer Power Supply Pin, 3.3V or 5V                                                                                                 |
| 14           | NC       | I   | No Connect<br>No internal bonding. This pin should be open or connected to DVSS.                                                          |
| 15           | TX0      | O   | Transmit Channel (Through Data) Output 0 Pin                                                                                              |
| 16           | TX1      | O   | When TX bit = “0”, Transmit Channel (Through Data) Output 1 Pin.<br>When TX bit = “1”, Transmit Channel (DAUX Data) Output Pin (Default). |
| 17           | BOUT     | O   | Block-Start Output Pin for Receiver Input<br>“H” during first 40 frames.                                                                  |
| 18           | COUT     | O   | C-bit Output Pin for Receiver Input                                                                                                       |
| 19           | UOUT     | O   | U-bit Output Pin for Receiver Input                                                                                                       |
| 20           | VOUT     | O   | V-bit Output Pin for Receiver Input                                                                                                       |
| 21           | DVDD     | I   | Digital Power Supply Pin, 3.3V                                                                                                            |
| 22           | DVSS     | I   | Digital Ground Pin                                                                                                                        |
| 23           | MCKO1    | O   | Master Clock Output 1 Pin                                                                                                                 |
| 24           | LRCK     | I/O | Channel Clock Pin                                                                                                                         |
| 25           | SDTO     | O   | Audio Serial Data Output Pin                                                                                                              |
| 26           | BICK     | I/O | Audio Serial Data Clock Pin                                                                                                               |
| 27           | MCKO2    | O   | Master Clock Output 2 Pin                                                                                                                 |
| 28           | DAUX     | I   | Auxiliary Audio Data Input Pin                                                                                                            |
| 29           | XTO      | O   | X'tal Output Pin                                                                                                                          |
| 30           | XTI      | I   | X'tal Input Pin                                                                                                                           |

**PIN/FUNCTION (Continued)**

| No. | Pin Name | I/O | Function                                                                                     |
|-----|----------|-----|----------------------------------------------------------------------------------------------|
| 31  | PDN      | I   | Power-Down Mode Pin<br>When "L", the AK4114 is powered-down and reset.                       |
| 32  | CM0      | I   | Master Clock Operation Mode 0 Pin in Parallel Mode                                           |
|     | CDTO     | O   | Control Data Output Pin in Serial Mode, IIC= "L".                                            |
|     | CAD1     | I   | Chip Address 1 Pin in Serial Mode, IIC= "H".                                                 |
| 33  | CM1      | I   | Master Clock Operation Mode 1 Pin in Parallel Mode                                           |
|     | CDTI     | I   | Control Data Input Pin in Serial Mode, IIC= "L".                                             |
|     | SDA      | I/O | Control Data Pin in Serial Mode, IIC= "H".                                                   |
| 34  | OCKS1    | I   | Output Clock Select 1 Pin in Parallel Mode                                                   |
|     | CCLK     | I   | Control Data Clock Pin in Serial Mode, IIC= "L"                                              |
|     | SCL      | I   | Control Data Clock Pin in Serial Mode, IIC= "H"                                              |
| 35  | OCKS0    | I   | Output Clock Select 0 Pin in Parallel Mode                                                   |
|     | CSN      | I   | Chip Select Pin in Serial Mode, IIC="L".                                                     |
|     | CAD0     | I   | Chip Address 0 Pin in Serial Mode, IIC= "H".                                                 |
| 36  | INT0     | O   | Interrupt 0 Pin                                                                              |
| 37  | INT1     | O   | Interrupt 1 Pin                                                                              |
| 38  | AVDD     | I   | Analog Power Supply Pin, 3.3V                                                                |
| 39  | R        | -   | External Resistor Pin<br>18k $\Omega$ +/-1% resistor should be connected to AVSS externally. |
| 40  | VCOM     | -   | Common Voltage Output Pin<br>0.47 $\mu$ F capacitor should be connected to AVSS externally.  |
| 41  | AVSS     | I   | Analog Ground Pin                                                                            |
| 42  | RX0      | I   | Receiver Channel 0 Pin (Internal biased pin)<br>This channel is default in serial mode.      |
| 43  | NC(AVSS) | I   | No Connect<br>No internal bonding. This pin should be connected to AVSS.                     |
| 44  | RX1      | I   | Receiver Channel 1 Pin (Internal biased pin)                                                 |
| 45  | TEST1    | I   | TEST 1 pin.<br>This pin should be connected to AVSS.                                         |
| 46  | RX2      | I   | Receiver Channel 2 Pin (Internal biased pin)                                                 |
| 47  | NC(AVSS) | I   | No Connect<br>No internal bonding. This pin should be connected to AVSS.                     |
| 48  | RX3      | I   | Receiver Channel 3 Pin (Internal biased pin)                                                 |

Note 1. All input pins except internal biased pins should not be left floating.

**ABSOLUTE MAXIMUM RATINGS**

(AVSS, DVSS=0V; Note 2)

| Parameter                                |                     | Symbol | min  | max      | Units |
|------------------------------------------|---------------------|--------|------|----------|-------|
| Power Supplies:                          | Analog              | AVDD   | -0.3 | 4.6      | V     |
|                                          | Digital             | DVDD   | -0.3 | 4.6      | V     |
|                                          | Input Buffer        | TVDD   | -0.3 | 6.0      | V     |
|                                          | AVSS-DVSS  (Note 3) | ΔGND   |      | 0.3      | V     |
| Input Current (Any pins except supplies) |                     | IIN    | -    | ±10      | mA    |
| Input Voltage (Except XTI pin)           |                     | VIN    | -0.3 | TVDD+0.3 | V     |
| Input Voltage (XTI pin)                  |                     | VINX   | -0.3 | DVDD+0.3 | V     |
| Ambient Temperature (Power applied)      |                     | Ta     | -10  | 70       | °C    |
| Storage Temperature                      |                     | Tstg   | -65  | 150      | °C    |

Note 2. All voltages with respect to ground.

Note 3. AVSS and DVSS must be connected to the same ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS**

(AVSS, DVSS=0V; Note 2)

| Parameter       |              | Symbol | min  | typ | max  | Units |
|-----------------|--------------|--------|------|-----|------|-------|
| Power Supplies: | Analog       | AVDD   | 2.7  | 3.3 | 3.6  | V     |
|                 | Digital      | DVDD   | 2.7  | 3.3 | AVDD | V     |
|                 | Input Buffer | TVDD   | DVDD | 3.3 | 5.5  | V     |

Note 2. All voltages with respect to ground.

**S/PDIF RECEIVER CHARACTERISTICS**

(Ta=25°C; AVDD, DVDD=2.7~3.6V;TVDD=2.7~5.5V)

| Parameter              | Symbol | min | typ | max | Units |
|------------------------|--------|-----|-----|-----|-------|
| Input Resistance       | Zin    |     | 10  |     | kΩ    |
| Input Voltage          | VTH    | 200 |     |     | mVpp  |
| Input Hysteresis       | VHY    |     | 50  |     | mV    |
| Input Sample Frequency | fs     | 32  | -   | 192 | kHz   |

**DC CHARACTERISTICS**

(Ta=25°C; AVDD, DVDD=2.7~3.6V;TVDD=2.7~5.5V; unless otherwise specified)

| Parameter                               | Symbol | min      | typ | max     | Units |
|-----------------------------------------|--------|----------|-----|---------|-------|
| Power Supply Current                    |        |          |     |         |       |
| Normal operation: PDN = "H" (Note 4)    |        |          | 28  | 56      | mA    |
| Power down: PDN = "L" (Note 5)          |        |          | 10  | 100     | μA    |
| High-Level Input Voltage                | VIH    | 70%DVDD  | -   | TVDD    | V     |
| Low-Level Input Voltage                 | VIL    | DVSS-0.3 | -   | 30%DVDD | V     |
| High-Level Output Voltage (Iout=-400μA) | VOH    | DVDD-0.4 | -   | -       | V     |
| Low-Level Output Voltage                |        |          |     |         |       |
| (Except SDA pin: Iout=400μA)            | VOL    | -        | -   | 0.4     | V     |
| ( SDA pin: Iout= 3mA)                   | VOL    | -        | -   | 0.4     | V     |
| Input Leakage Current                   | Iin    | -        | -   | ± 10    | μA    |

Note 4. AVDD, DVDD=3.3V, TVDD=5.0V, CL=20pF, fs=192kHz, X'tal=24.576MHz, Clock Operation Mode 2,

OCS1=1, OCS0=1. AVDD=11mA (typ), DVDD=17mA (typ), TVDD=10μA (typ).

DVDD=28mA (typ) when the circuit of Figure 22 is attached to both TX0 and TX1 pins.

Note 5. RX inputs are open and all digital input pins are held DVDD or DVSS.

| SWITCHING CHARACTERISTICS                             |           |        |         |      |        |       |
|-------------------------------------------------------|-----------|--------|---------|------|--------|-------|
| (Ta=25°C; DVDD, AVDD2.7~3.6V, TVDD=2.7~5.5V; CL=20pF) |           |        |         |      |        |       |
| Parameter                                             |           | Symbol | min     | typ  | max    | Units |
| <b>Master Clock Timing</b>                            |           |        |         |      |        |       |
| Crystal Resonator                                     | Frequency | fXTAL  | 11.2896 |      | 24.576 | MHz   |
| External Clock                                        | Frequency | fECLK  | 11.2896 |      | 24.576 | MHz   |
|                                                       | Duty      | dECLK  | 40      | 50   | 60     | %     |
| MCKO1 Output                                          | Frequency | fMCK1  | 4.096   |      | 24.576 | MHz   |
|                                                       | Duty      | dMCK1  | 40      | 50   | 60     | %     |
| MCKO2 Output                                          | Frequency | fMCK2  | 2.048   |      | 24.576 | MHz   |
|                                                       | Duty      | dMCK2  | 40      | 50   | 60     | %     |
| PLL Clock Recover Frequency (RX0-7)                   |           | fpLL   | 32      | -    | 192    | kHz   |
| LRCK Frequency                                        |           | fs     | 32      |      | 192    | kHz   |
| Duty Cycle                                            |           | dLCK   | 45      |      | 55     | %     |
| <b>Audio Interface Timing</b>                         |           |        |         |      |        |       |
| <b>Slave Mode</b>                                     |           |        |         |      |        |       |
| BICK Period                                           |           | tBCK   | 80      |      |        | ns    |
| BICK Pulse Width Low                                  |           | tBCKL  | 30      |      |        | ns    |
| Pulse Width High                                      |           | tBCKH  | 30      |      |        | ns    |
| LRCK Edge to BICK “↑”                                 |           | tLRB   | 20      |      |        | ns    |
| BICK “↑” to LRCK Edge                                 |           | tBLR   | 20      |      |        | ns    |
| LRCK to SDTO (MSB)                                    |           | tLRM   |         |      | 30     | ns    |
| BICK “↓” to SDTO                                      |           | tBSD   |         |      | 30     | ns    |
| DAUX Hold Time                                        |           | tDXH   | 20      |      |        | ns    |
| DAUX Setup Time                                       |           | tDXS   | 20      |      |        | ns    |
| <b>Master Mode</b>                                    |           |        |         |      |        |       |
| BICK Frequency                                        |           | fBCK   |         | 64fs |        | Hz    |
| BICK Duty                                             |           | dBCK   |         | 50   |        | %     |
| BICK “↓” to LRCK                                      |           | tMBLR  | -20     |      | 20     | ns    |
| BICK “↓” to SDTO                                      |           | tBSD   |         |      | 10     | ns    |
| DAUX Hold Time                                        |           | tDXH   | 20      |      |        | ns    |
| DAUX Setup Time                                       |           | tDXS   | 20      |      |        | ns    |
| <b>Control Interface Timing (4-wire serial mode)</b>  |           |        |         |      |        |       |
| CCLK Period                                           |           | tCCK   | 200     |      |        | ns    |
| CCLK Pulse Width Low                                  |           | tCCKL  | 80      |      |        | ns    |
| Pulse Width High                                      |           | tCCKH  | 80      |      |        | ns    |
| CDTI Setup Time                                       |           | tCDS   | 50      |      |        | ns    |
| CDTI Hold Time                                        |           | tCDH   | 50      |      |        | ns    |
| CSN “H” Time                                          |           | tCSW   | 150     |      |        | ns    |
| CSN “↓” to CCLK “↑”                                   |           | tCSS   | 50      |      |        | ns    |
| CCLK “↑” to CSN “↑”                                   |           | tCSH   | 50      |      |        | ns    |
| CDTO Delay                                            |           | tDCD   |         |      | 45     | ns    |
| CSN “↑” to CDTO Hi-Z                                  |           | tCCZ   |         |      | 70     | ns    |

Note 6. BICK rising edge must not occur at the same time as LRCK edge.

**SWITCHING CHARACTERISTICS (Continued)**

(Ta=25°C; DVDD, AVDD2.7~3.6V, TVDD=2.7~5.5V; CL=20pF)

| Parameter                                                  | Symbol  | min | typ | max  | Units |
|------------------------------------------------------------|---------|-----|-----|------|-------|
| <b>Control Interface Timing (I<sup>2</sup>C Bus mode):</b> |         |     |     |      |       |
| SCL Clock Frequency                                        | fSCL    | -   |     | 100  | kHz   |
| Bus Free Time Between Transmissions                        | tBUF    | 4.7 |     | -    | μs    |
| Start Condition Hold Time<br>(prior to first clock pulse)  | tHD:STA | 4.0 |     | -    | μs    |
| Clock Low Time                                             | tLOW    | 4.7 |     | -    | μs    |
| Clock High Time                                            | tHIGH   | 4.0 |     | -    | μs    |
| Setup Time for Repeated Start Condition                    | tSU:STA | 4.7 |     | -    | μs    |
| SDA Hold Time from SCL Falling (Note 7)                    | tHD:DAT | 0   |     | -    | μs    |
| SDA Setup Time from SCL Rising                             | tSU:DAT | 250 |     | -    | ns    |
| Rise Time of Both SDA and SCL Lines                        | tR      | -   |     | 1000 | ns    |
| Fall Time of Both SDA and SCL Lines                        | tF      | -   |     | 300  | ns    |
| Setup Time for Stop Condition                              | tSU:STO | 4.0 |     | -    | μs    |
| Capacitive load on bus                                     | Cb      | -   |     | 400  | pF    |
| <b>Reset Timing</b>                                        |         |     |     |      |       |
| PDN Pulse Width                                            | tPW     | 150 |     |      | ns    |

Note 7. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 8. I<sup>2</sup>C is a registered trademark of Philips Semiconductors.

Purchase of Asahi Kasei Microsystems Co., Ltd I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system, provided the system conform to the I<sup>2</sup>C specifications defined by Philips.

## ■ Timing Diagram

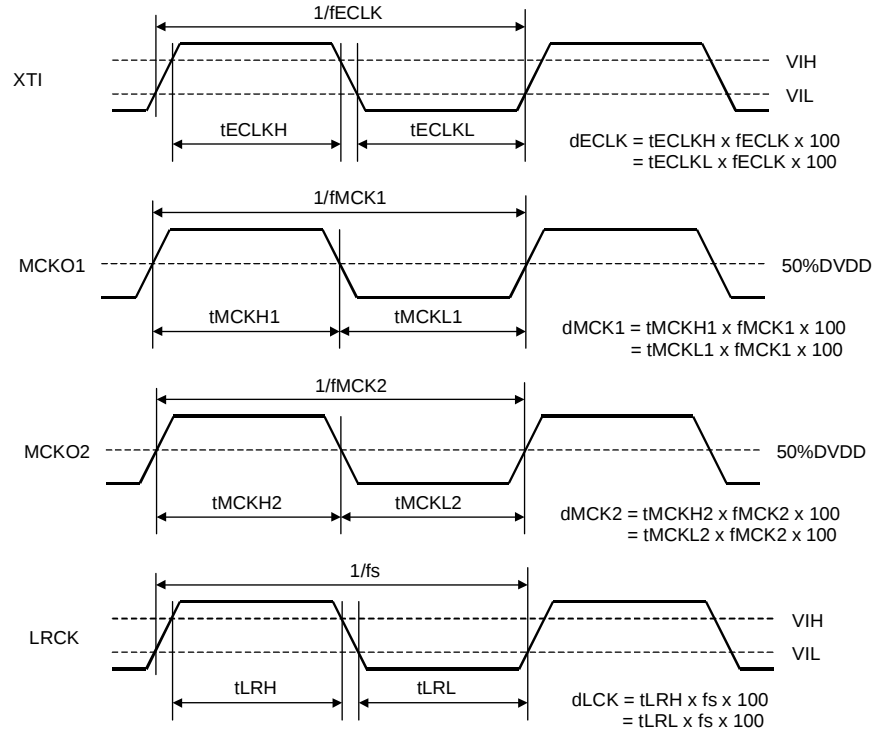


Figure 1. Clock Timing

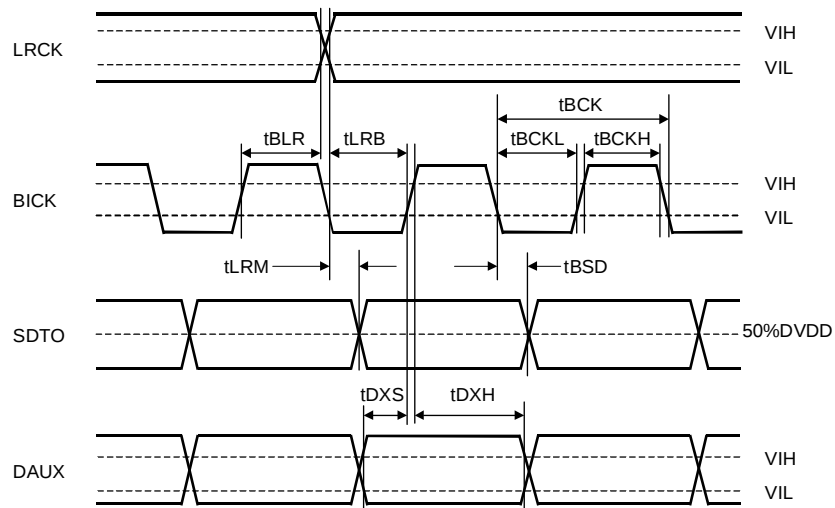


Figure 2. Serial Interface Timing (Slave Mode)

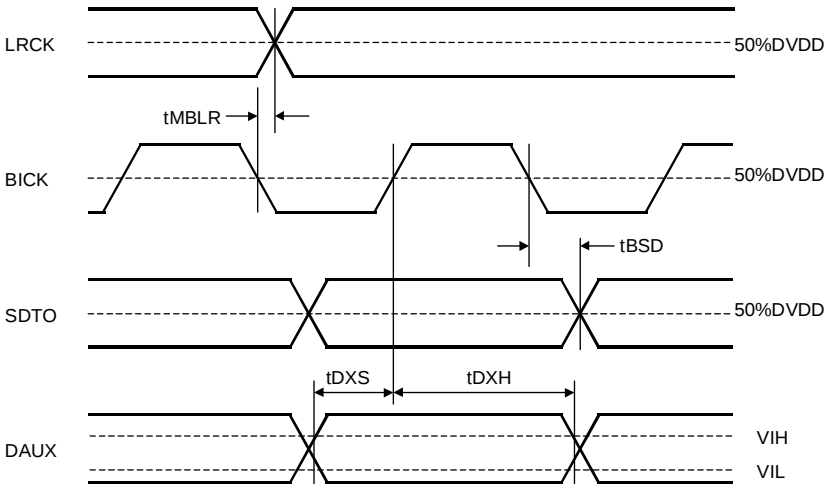


Figure 3. Serial Interface Timing (Master Mode)

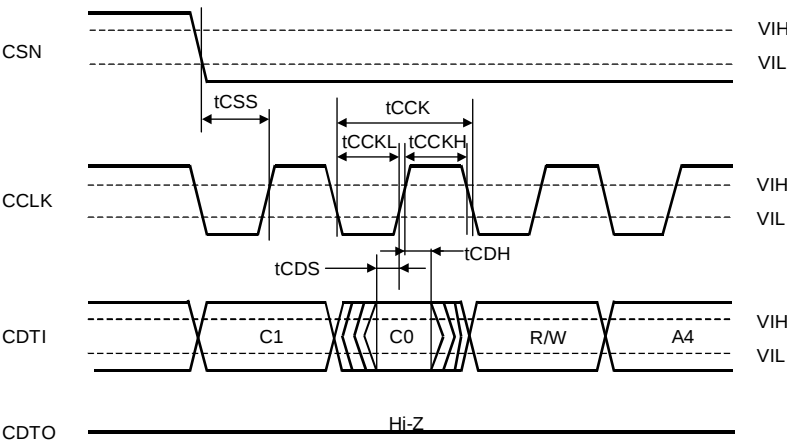


Figure 4. WRITE/READ Command Input Timing in 4-wire serial mode

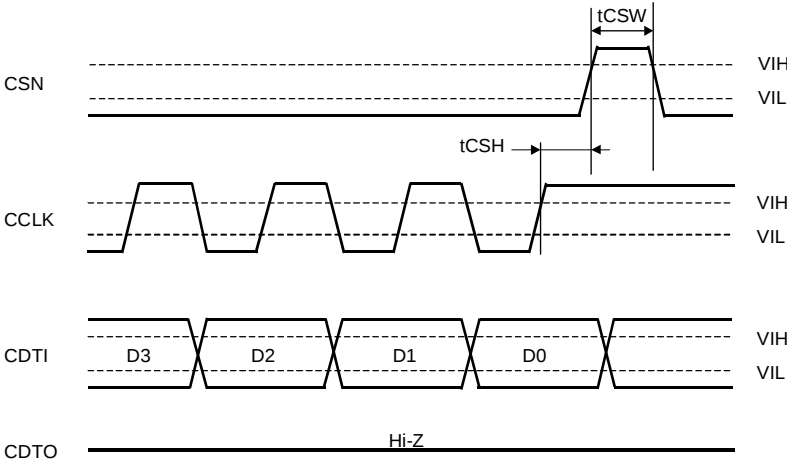


Figure 5. WRITE Data Input Timing in 4-wire serial mode

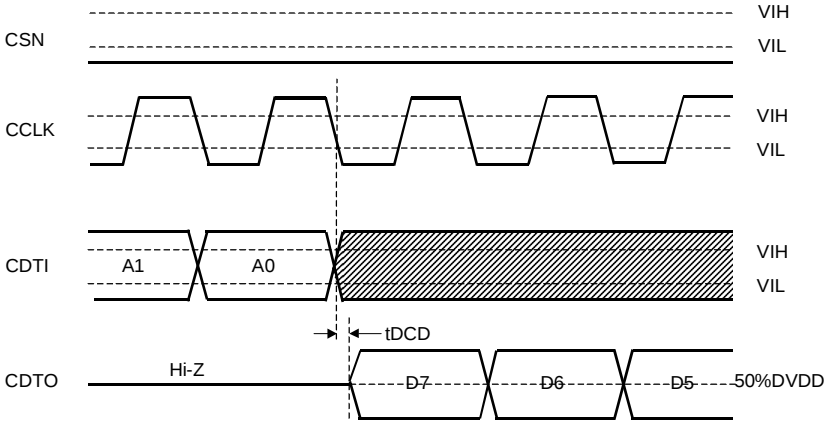


Figure 6. READ Data Output Timing 1 in 4-wire serial mode

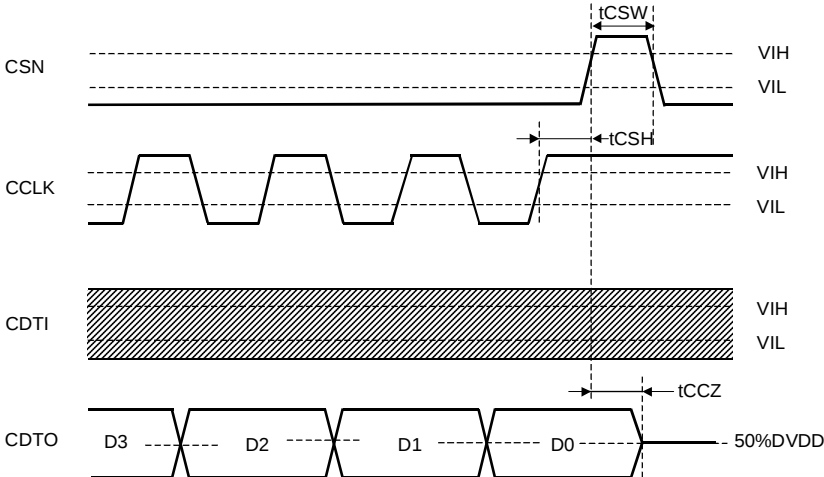


Figure 7. READ Data Input Timing 2 in 4-wire serial mode

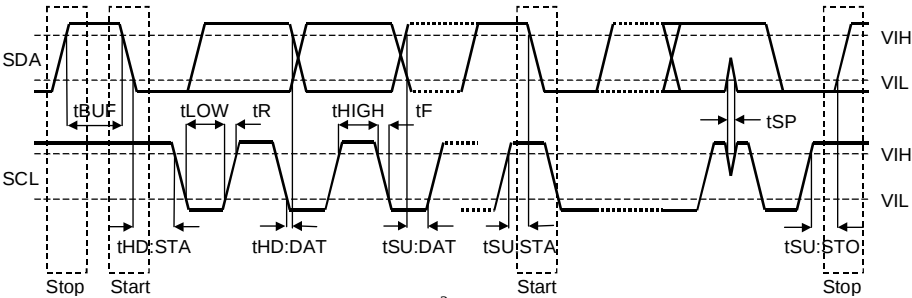


Figure 8. I²C Bus mode Timing

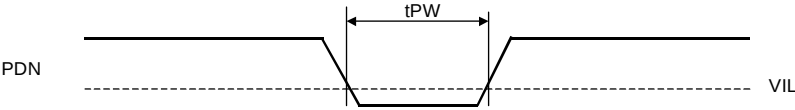


Figure 9. Power Down & Reset Timing

## OPERATION OVERVIEW

### ■ Non-PCM (AC-3, MPEG, etc.) and DTS-CD Bitstream Detection

The AK4114 has a Non-PCM stream auto-detection function. When the 32bit mode Non-PCM preamble based on Dolby "AC-3 Data Stream in IEC60958 Interface" is detected, the AUTO bit goes "1". The 96bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the AUTO "1". Once the AUTO is set "1", it will remain "1" until 4096 frames pass through the chip without additional sync pattern being detected. When those preambles are detected, the burst preambles Pc and Pd that follow those sync codes are stored to registers. The AK4114 also has the DTS-CD bitstream auto-detection function. When AK4114 detects DTS-CD bitstreams, DTSCD bit goes to "1". When the next sync code does not come within 4096 frames, DTSCD bit goes to "0" until when AK4114 detects the stream again.

### ■ 192kHz Clock Recovery

On chip low jitter PLL has a wide lock range with 32kHz to 192kHz and the lock time is less than 20ms. The AK4114 has the sampling frequency detect function. By either the clock comparison against X'tal oscillator or using the channel status, AK4114 detects the sampling frequency (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz). The PLL loses lock when the received sync interval is incorrect.

### ■ Master Clock

The AK4114 has two clock outputs, MCKO1 and MCKO2. These clocks are derived from either the recovered clock or from the X'tal oscillator. The frequencies of the master clock outputs (MCKO1 and MCKO2) are set by OCKS0 and OCKS1 as shown in Table 1. The 512fs clock will not output when 96kHz and 192kHz. The 256fs clock will not output when 192kHz.

| No. | OCKS1 | OCKS0 | MCKO1 | MCKO2 | X'tal | fs (max) | Default |
|-----|-------|-------|-------|-------|-------|----------|---------|
| 0   | 0     | 0     | 256fs | 256fs | 256fs | 96 kHz   |         |
| 1   | 0     | 1     | 256fs | 128fs | 256fs | 96 kHz   |         |
| 2   | 1     | 0     | 512fs | 256fs | 512fs | 48 kHz   |         |
| 3   | 1     | 1     | 128fs | 64fs  | 128fs | 192 kHz  |         |

Table 1. Master Clock Frequency Select (Stereo mode)

### ■ Clock Operation Mode

The CM0/CM1 pins (or bits) select the clock source and the data source of SDTO. In Mode 2, the clock source is switched from PLL to X'tal when PLL goes unlock state. In Mode3, the clock source is fixed to X'tal, but PLL is also operating and the recovered data such as C bits can be monitored. For Mode2 and 3, it is recommended that the frequency of X'tal is different from the recovered frequency from PLL.

| Mode | CM1 | CM0 | UNLOCK | PLL | X'tal    | Clock source | SDTO | Default |
|------|-----|-----|--------|-----|----------|--------------|------|---------|
| 0    | 0   | 0   | -      | ON  | ON(Note) | PLL          | RX   |         |
| 1    | 0   | 1   | -      | OFF | ON       | X'tal        | DAUX |         |
| 2    | 1   | 0   | 0      | ON  | ON       | PLL          | RX   |         |
|      |     |     | 1      | ON  | ON       | X'tal        | DAUX |         |
| 3    | 1   | 1   | -      | ON  | ON       | X'tal        | DAUX |         |

ON: Oscillation (Power-up), OFF: STOP (Power-down)

Note : When the X'tal is not used as clock comparison for fs detection (i.e. XTL1,0= "1,1"), the X'tal is off.

Table 2. Clock Operation Mode select

## ■ Clock Source

The following circuits are available to feed the clock to XTI pin of AK4114.

### 1) X'tal

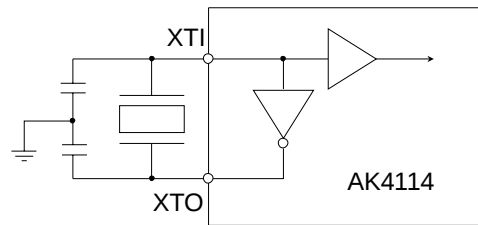


Figure 10. X'tal mode

Note: External capacitance depends on the crystal oscillator (Typ. 10-40pF)

### 2) External clock

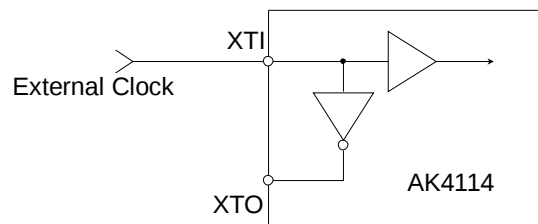


Figure 11. External clock mode

Note: Input clock must not exceed DVDD.

### 3) Fixed to the Clock Operation Mode 0

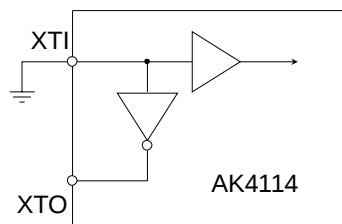


Figure 12. off mode

## ■ Sampling Frequency and Pre-emphasis Detection

The AK4114 has two methods for detecting the sampling frequency as follows.

1. Clock comparison between recovered clock and X'tal oscillator
2. Sampling frequency information on channel status

Those could be selected by XTL1, 0 bits. And the detected frequency is reported on FS3-0 bits.

| XTL1 | XTL0 | X'tal Frequency      | Default |
|------|------|----------------------|---------|
| 0    | 0    | 11.2896MHz           |         |
| 0    | 1    | 12.288MHz            |         |
| 1    | 0    | 24.576MHz            |         |
| 1    | 1    | (Use channel status) |         |

Table 3. Reference X'tal frequency

| Register output |     |     |     | fs       | Except XTL1,0= "1,1"         | XTL1,0= "1,1"             |                   |                     |
|-----------------|-----|-----|-----|----------|------------------------------|---------------------------|-------------------|---------------------|
|                 |     |     |     |          | Clock comparison<br>(Note 1) | Consumer mode<br>(Note 2) | Professional mode |                     |
| FS3             | FS2 | FS1 | FS0 |          |                              | Byte3<br>Bit3,2,1,0       | Byte0<br>Bit7,6   | Byte4<br>Bit6,5,4,3 |
| 0               | 0   | 0   | 0   | 44.1kHz  | 44.1kHz                      | 0 0 0 0                   | 0 1               | 0 0 0 0             |
| 0               | 0   | 0   | 1   | Reserved | Reserved                     | 0 0 0 1                   | (Others)          |                     |
| 0               | 0   | 1   | 0   | 48kHz    | 48kHz                        | 0 0 1 0                   | 1 0               | 0 0 0 0             |
| 0               | 0   | 1   | 1   | 32kHz    | 32kHz                        | 0 0 1 1                   | 1 1               | 0 0 0 0             |
| 1               | 0   | 0   | 0   | 88.2kHz  | 88.2kHz                      | (1 0 0 0)                 | 0 0               | 1 0 1 0             |
| 1               | 0   | 1   | 0   | 96kHz    | 96kHz                        | (1 0 1 0)                 | 0 0               | 0 0 1 0             |
| 1               | 1   | 0   | 0   | 176.4kHz | 176.4kHz                     | (1 1 0 0)                 | 0 0               | 1 0 1 1             |
| 1               | 1   | 1   | 0   | 192kHz   | 192kHz                       | (1 1 1 0)                 | 0 0               | 0 0 1 1             |

Note1: At least  $\pm 3\%$  range is identified as the value in the Table 4. In case of intermediate frequency of those two, FS3-0 bits indicate nearer value. When the frequency is much bigger than 192kHz or much smaller than 32kHz, FS3-0 bits may indicate "0001".

Note2: When consumer mode, Byte3 Bit3-0 are copied to FS3-0.

Table 4. fs Information

The pre-emphasis information is detected and reported on PEM bit. These information are extracted from channel 1 at default. It can be switched to channel 2 by CS12 bit in control register.

| PEM | Pre-emphasis | Byte 0<br>Bits 3-5 |
|-----|--------------|--------------------|
| 0   | OFF          | $\neq 0X100$       |
| 1   | ON           | 0X100              |

Table 5. PEM in Consumer Mode

| PEM | Pre-emphasis | Byte 0<br>Bits 2-4 |
|-----|--------------|--------------------|
| 0   | OFF          | $\neq 110$         |
| 1   | ON           | 110                |

Table 6. PEM in Professional Mode

## ■ De-emphasis Filter Control

The AK4114 includes the digital de-emphasis filter ( $t_c=50/15\mu s$ ) by IIR filter corresponding to four sampling frequencies (32kHz, 44.1kHz, 48kHz and 96kHz). When DEAU bit="1", the de-emphasis filter is enabled automatically by sampling frequency and pre-emphasis information in the channel status. The AK4114 goes this mode at default. Therefore, in Parallel Mode, the AK4114 is always placed in this mode and the status bits in channel 1 control the de-emphasis filter. In Serial Mode, DEM0/1 and DFS bits can control the de-emphasis filter when DEAU is "0". The internal de-emphasis filter is bypassed and the recovered data is output without any change if either pre-emphasis or de-emphasis Mode is OFF.

| PEM | FS3      | FS2 | FS1 | FS0 | Mode    |
|-----|----------|-----|-----|-----|---------|
| 1   | 0        | 0   | 0   | 0   | 44.1kHz |
| 1   | 0        | 0   | 1   | 0   | 48kHz   |
| 1   | 0        | 0   | 1   | 1   | 32kHz   |
| 1   | 1        | 0   | 1   | 0   | 96kHz   |
| 1   | (Others) |     |     |     | OFF     |
| 0   | x        | x   | x   | x   | OFF     |

Table 7. De-emphasis Auto Control at DEAU = "1" (Default)

| PEM | DFS | DEM1 | DEM0 | Mode    | Default |
|-----|-----|------|------|---------|---------|
| 1   | 0   | 0    | 0    | 44.1kHz |         |
| 1   | 0   | 0    | 1    | OFF     |         |
| 1   | 0   | 1    | 0    | 48kHz   |         |
| 1   | 0   | 1    | 1    | 32kHz   |         |
| 1   | 1   | 0    | 0    | OFF     |         |
| 1   | 1   | 0    | 1    | OFF     |         |
| 1   | 1   | 1    | 0    | 96kHz   |         |
| 1   | 1   | 1    | 1    | OFF     |         |
| 0   | x   | x    | x    | OFF     |         |

Table 8. De-emphasis Manual Control at DEAU = "0"

## ■ System Reset and Power-Down

The AK4114 has a power-down mode for all circuits by PDN pin can be partially powerd-down by PWN bit. The RSTN bit initializes the register and resets the internal timing. In Parallel Mode, only the control by PDN pin is enabled. The AK4114 should be reset once by bringing PDN pin = "L" upon power-up.

PDN Pin:

All analog and digital circuit are placed in the power-down and reset mode by bringing PDN= "L". All the registers are initialized, and clocks are stopped. Reading/Writing to the register are disabled.

RSTN Bit (Address 00H; D0):

All the registers except PWN and RSTN are initialized by bringing RSTN bit = "0". The internal timings are also initialized. Writing to the register is not available except PWN and RSTN. Reading to the register is disabled.

PWN Bit (Address 00H; D1):

The clock recovery part is initialized by bringing PWN bit = "0". In this case, clocks are stopped. The registers are not initialized and the mode settings are kept. Writing and Reading to the registers are enabled.

## ■ Biphase Input and Through Output

Eight receiver inputs (RX0-7) are available in Serial Control Mode. Each input includes amplifier corresponding to unbalance mode and can accept the signal of 200mV or more. IPS2-0 selects the receiver channel. When BCU bit = "1", the Block start signal, C bit and U bit can output from each pins.

| IPS2 | IPS1 | IPS0 | INPUT Data | Default |
|------|------|------|------------|---------|
| 0    | 0    | 0    | RX0        |         |
| 0    | 0    | 1    | RX1        |         |
| 0    | 1    | 0    | RX2        |         |
| 0    | 1    | 1    | RX3        |         |
| 1    | 0    | 0    | RX4        |         |
| 1    | 0    | 1    | RX5        |         |
| 1    | 1    | 0    | RX6        |         |
| 1    | 1    | 1    | RX7        |         |

Table 9. Recovery Data Select

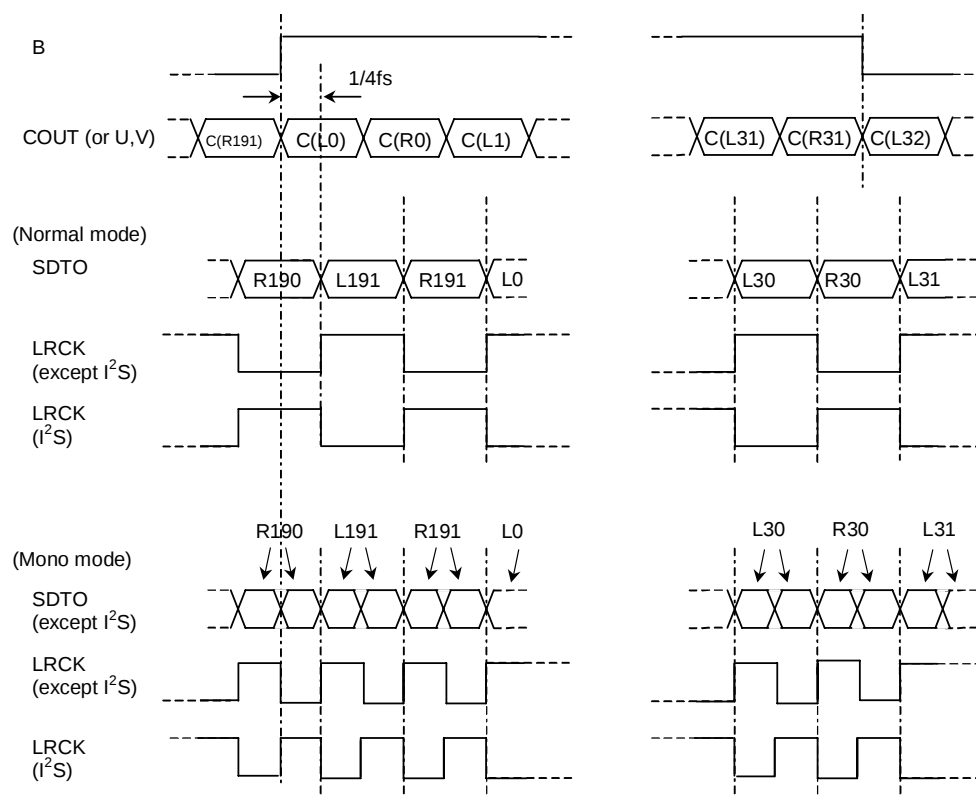


Figure 13. B, C, U, V output/input timings

## ■ Biphase Output

The AK4114 can output either the through output(from DIR) or transmitter output(DIT; the data from DAUX is transformed to IEC60958 format.) from TX1/0 pins. Those could be selected by DIT bit. The source of the through output from TX0 could be selected among RX0-8 by OPS00,01 and 02 bits, for TX1, by OPS10,11 and 12 bits respectively. When output DAUX data, V bit could be controlled by VIN pin and first 5 bytes of C bit could be controlled by CT39-CT0 bits in control registers. When bit0= "0"(consumer mode), bit20-23(Audio channel) could not be controlled directly but be controlled by CT20 bit. When the CT20 bit is "1", AK4114 outputs "1000" as C20-23 for left channel and output "0100" at C20-23 for right channel automatically. When CT20 bit is "0", AK4114 outputs "0000" set as "1000" for sub frame 1, and "0100" for sub frame 2. U bits are fixed to "0".as C20-23 for both channel. U bit could be controlled by UDIT bit as follows; When UDIT bit is "0", U bit is always "L". When UDIT bit is "1", the recovered U bits are used for DIT( DIR-DIT loop mode of U bit). This mode is only available when PLL is locked and the master mode.

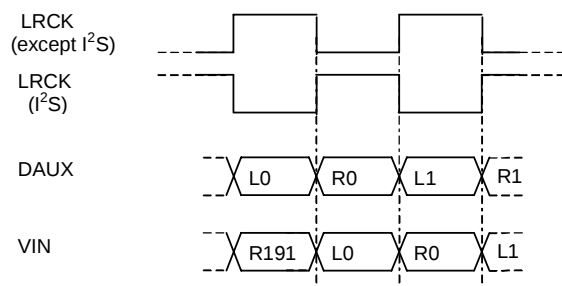
| OPS02 | OPS01 | OPS00 | Output Data | Default |
|-------|-------|-------|-------------|---------|
| 0     | 0     | 0     | RX0         |         |
| 0     | 0     | 1     | RX1         |         |
| 0     | 1     | 0     | RX2         |         |
| 0     | 1     | 1     | RX3         |         |
| 1     | 0     | 0     | RX4         |         |
| 1     | 0     | 1     | RX5         |         |
| 1     | 1     | 0     | RX6         |         |
| 1     | 1     | 1     | RX7         |         |

Table 10. Output Data Select for TX0

| DIT | OPS12 | OPS11 | OPS10 | Output Data | Default |
|-----|-------|-------|-------|-------------|---------|
| 0   | 0     | 0     | 0     | RX0         |         |
| 0   | 0     | 0     | 1     | RX1         |         |
| 0   | 0     | 1     | 0     | RX2         |         |
| 0   | 0     | 1     | 1     | RX3         |         |
| 0   | 1     | 0     | 0     | RX4         |         |
| 0   | 1     | 0     | 1     | RX5         |         |
| 0   | 1     | 1     | 0     | RX6         |         |
| 0   | 1     | 1     | 1     | RX7         |         |
| 1   | x     | x     | x     | DAUX        |         |

Table 11. Output Data Select for TX1

(Normal mode)



(Mono mode)

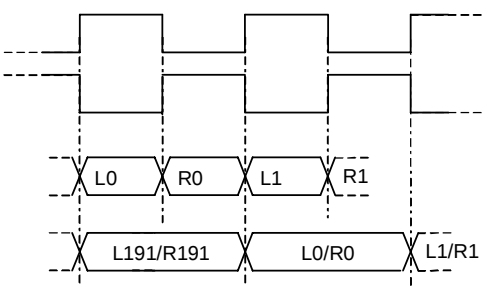


Figure 14. DAUX and VIN input timings

## ■ Double sampling frequency mode

When MONO bit = “1”, the AK4114 outputs data with double speed according to “Single channel double sampling frequency mode” of AES3. For example, when 192kHz mono data is transmitted or received, L/R channels of 96kHz biphas data are used. In this case, 1 frame is 96kHz and LRCK frequency is 192kHz.

### 1) RX

When MONO bit = “1”, AK4114 outputs mono data from SDTO as follows.

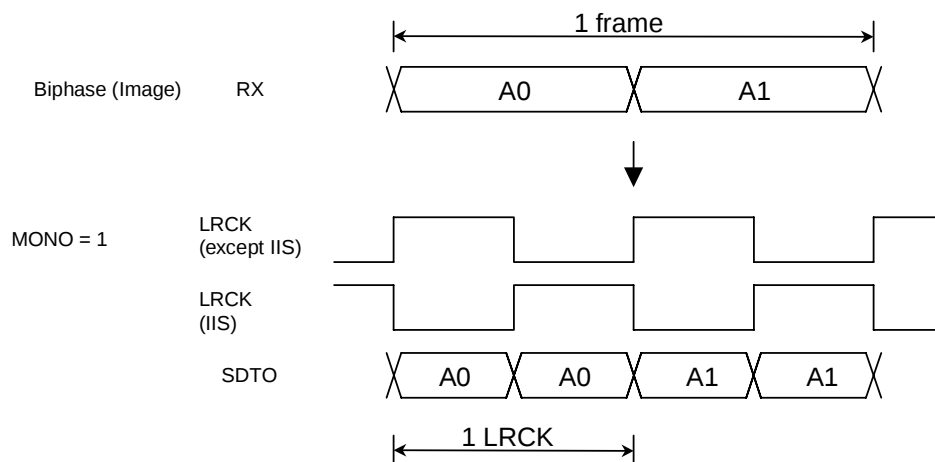


Figure 15. MONO mode (RX)

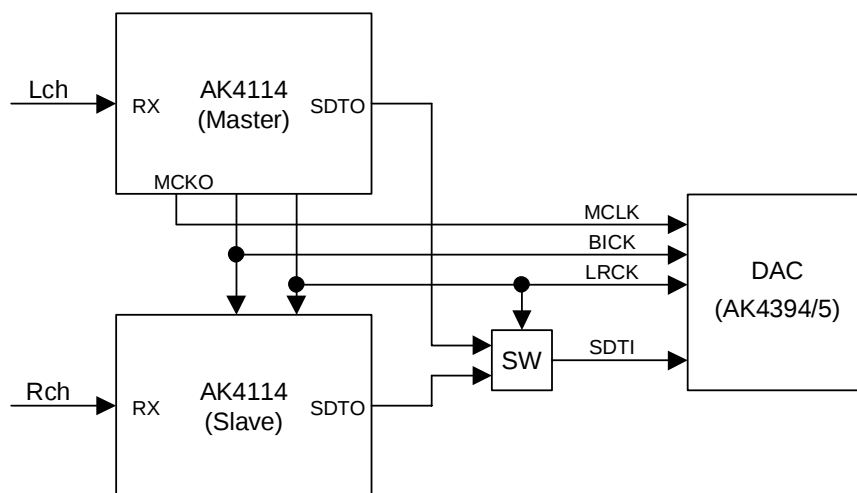


Figure 16. MONO mode Connection Example (RX)

## 2) TX

When MONO bit = "1" and TLR bit = "0", the AK4114 outputs Lch data through TX1 as biphasic signal. When MONO bit = "1" and TLR bit = "1", then Rch data.

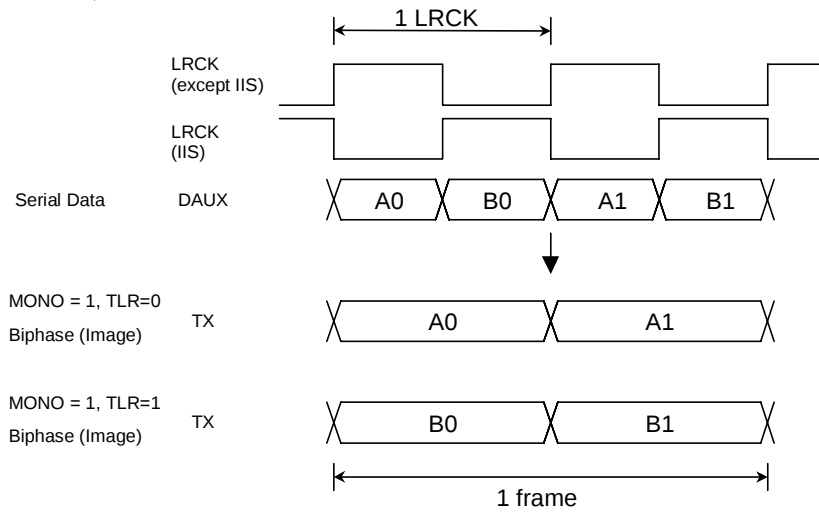


Figure 17. MONO mode (TX)

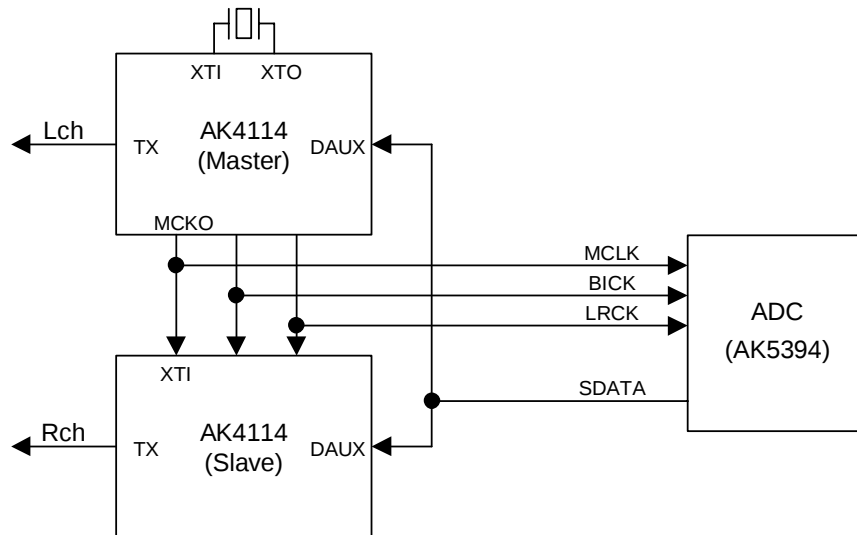
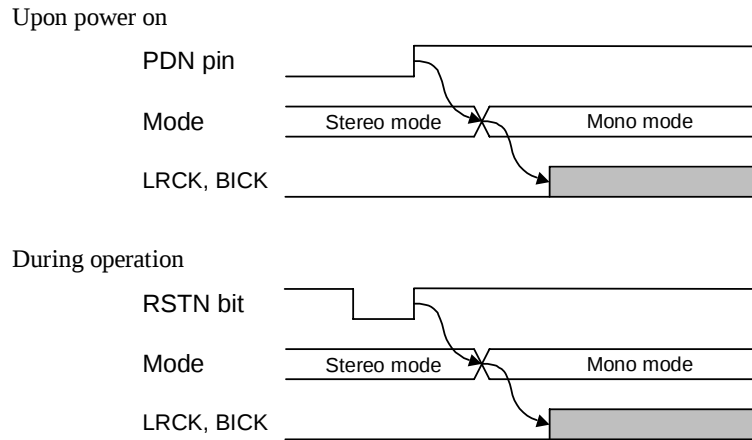


Figure 18. MONO mode Connection Example (TX)

Note: When the connection example (Figure 18) or multiple AK4114s are used, LRCK and BICK should be input after reset so that the phase of TX outputs is aligned. The AK4114s should be set by following sequence (Figure 19).



- (1) Reset all the AK4114s by PDN pin = “L” → “H” or RSTN bit = “0” → “1”.
- (2) Set all the AK4114s to MONO mode while they are still in slave mode.
- (3) Set one of the AK4114s to master mode so that LRCK is input to all other AK4114s at the same time, or LRCK should be input to all the AK4114s at the same time.

Figure 19. MONO mode setup sequence (TX)

## ■ Biphase signal input/output circuit

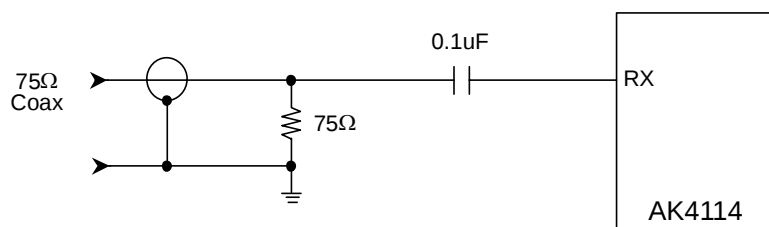


Figure 20. Consumer Input Circuit (Coaxial Input)

Note: In case of coaxial input, if a coupling level to this input from the next RX input line pattern exceeds 50mV, there is a possibility to occur an incorrect operation. In this case, it is possible to lower the coupling level by adding this decoupling capacitor.

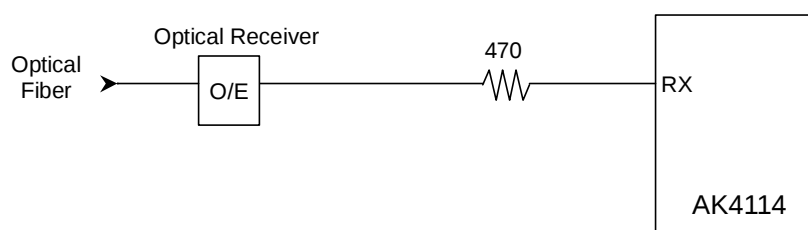


Figure 21. Consumer Input Circuit (Optical Input)

In case of coaxial input, as the input level of RX line is small, in Serial Mode, be careful not to crosstalk among RX input lines. For example, by inserting the shield pattern among them. In Parallel Mode, four channel inputs (RX0,1,2,3) are available and RX4-7 change to other pins for audio format control. Those pins must be fixed to "H" or "L".

The AK4114 includes the TX output buffer. The output level meets combination 0.5V+/-20% using the external resistor network. The T1 in Figure 22 is a transformer of 1:1.

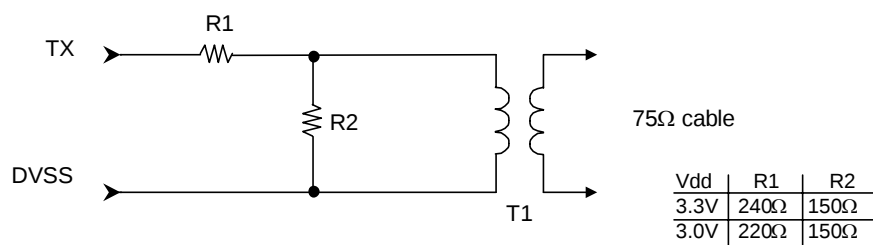
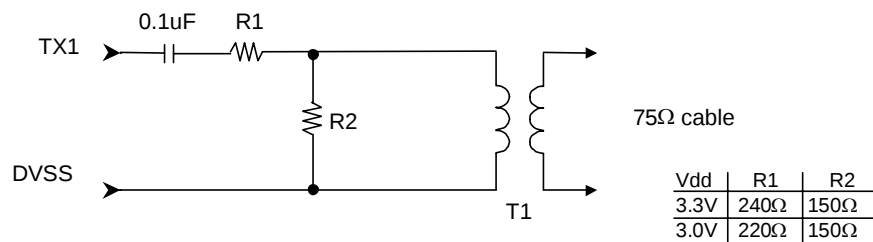


Figure 22. TX External Resistor Network

Note: When the AK4114 is in the power-down mode (PDN= "L"), power supply current can be suppressed by using AC couple capacitor as following figure since TX1 pin output becomes uncertain at power-down mode.



## ■ Q-subcode buffers

The AK4114 has Q-subcode buffer for CD application. The AK4114 takes Q-subcode into registers by following conditions.

1. The sync word (S0,S1) is constructed at least 16 "0"s.
2. The start bit is "1".
3. Those 7bits Q-W follows to the start bit.
4. The distance between two start bits are 8-16 bits.

The QINT bit in the control register goes "1" when the new Q-subcode differs from old one, and goes "0" when QINT bit is read.

|     | 1 | 2   | 3   | 4   | 5   | 6   | 7   | 8   | *    |
|-----|---|-----|-----|-----|-----|-----|-----|-----|------|
| S0  | 0 | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0... |
| S1  | 0 | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0... |
| S2  | 1 | Q2  | R2  | S2  | T2  | U2  | V2  | W2  | 0... |
| S3  | 1 | Q3  | R3  | S3  | T3  | U3  | V3  | W3  | 0... |
| :   | : | :   | :   | :   | :   | :   | :   | :   | :    |
| S97 | 1 | Q97 | R97 | S97 | T97 | U97 | V97 | W97 | 0... |
| S0  | 0 | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0... |
| S1  | 0 | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0... |
| S2  | 1 | Q2  | R2  | S2  | T2  | U2  | V2  | W2  | 0... |
| S3  | 1 | Q3  | R3  | S3  | T3  | U3  | V3  | W3  | 0... |
| :   | : | :   | :   | :   | :   | :   | :   | :   | :    |

(\*) number of "0" : min=0; max=8.

Figure 23. Configuration of U-bit(CD)

|                |     |     |     |      |     |     |     |                 |     |     |     |     |     |     |     |                 |     |     |     |     |     |     |     |
|----------------|-----|-----|-----|------|-----|-----|-----|-----------------|-----|-----|-----|-----|-----|-----|-----|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Q2             | Q3  | Q4  | Q5  | Q6   | Q7  | Q8  | Q9  | Q10             | Q11 | Q12 | Q13 | Q14 | Q15 | Q16 | Q17 | Q18             | Q19 | Q20 | Q21 | Q22 | Q23 | Q24 | Q25 |
| CTRL           |     |     |     | ADRS |     |     |     | TRACK NUMBER    |     |     |     |     |     |     |     | INDEX           |     |     |     |     |     |     |     |
| Q26            | Q27 | Q28 | Q29 | Q30  | Q31 | Q32 | Q33 | Q34             | Q35 | Q36 | Q37 | Q38 | Q39 | Q40 | Q41 | Q42             | Q43 | Q44 | Q45 | Q46 | Q47 | Q48 | Q49 |
| MINUTE         |     |     |     |      |     |     |     | SECOND          |     |     |     |     |     |     |     | FRAME           |     |     |     |     |     |     |     |
| Q50            | Q51 | Q52 | Q53 | Q54  | Q55 | Q56 | Q57 | Q58             | Q59 | Q60 | Q61 | Q62 | Q63 | Q64 | Q65 | Q66             | Q67 | Q68 | Q69 | Q70 | Q71 | Q72 | Q73 |
| ZERO           |     |     |     |      |     |     |     | ABSOLUTE MINUTE |     |     |     |     |     |     |     | ABSOLUTE SECOND |     |     |     |     |     |     |     |
| Q74            | Q75 | Q76 | Q77 | Q78  | Q79 | Q80 | Q81 | Q82             | Q83 | Q84 | Q85 | Q86 | Q87 | Q88 | Q89 | Q90             | Q91 | Q92 | Q93 | Q94 | Q95 | Q96 | Q97 |
| ABSOLUTE FRAME |     |     |     |      |     |     |     | CRC             |     |     |     |     |     |     |     |                 |     |     |     |     |     |     |     |

G(x)=x<sup>16</sup>+x<sup>12</sup>+x<sup>5</sup>+1

Figure 24. Q-subcode

| Addr | Register Name               | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|------|-----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|
|      | Q-subcode Address / Control | Q9  | Q8  | ... | ... | ... | ... | Q3  | Q2  |
|      | Q-subcode Track             | Q17 | Q16 | ... | ... | ... | ... | Q11 | Q10 |
|      | Q-subcode Index             | ... | ... | ... | ... | ... | ... | ... | ... |
|      | Q-subcode Minute            | ... | ... | ... | ... | ... | ... | ... | ... |
|      | Q-subcode Second            | ... | ... | ... | ... | ... | ... | ... | ... |
|      | Q-subcode Frame             | ... | ... | ... | ... | ... | ... | ... | ... |
|      | Q-subcode Zero              | ... | ... | ... | ... | ... | ... | ... | ... |
|      | Q-subcode ABS Minute        | ... | ... | ... | ... | ... | ... | ... | ... |
|      | Q-subcode ABS Second        | ... | ... | ... | ... | ... | ... | ... | ... |
|      | Q-subcode ABS Frame         | Q81 | Q80 | ... | ... | ... | ... | Q75 | Q74 |

Figure 25. Q-subcode register

## ■ Error Handling

There are the following eight events who make INT0/1 pin “H”. INT0/1 pin shows the status of following conditions.

1. UNLOCK : “1” when the PLL loses lock.  
AK4114 loses lock when the distance between two preambles is not correct or when those preambles are not correct.
2. PAR : “1” when parity error or biphase coding error is detected, and keeps “1” until this register is read.  
Updated every sub-frame cycle. Reading this register resets itself.
3. AUTO : “1” when Non-PCM bitstream is detected.  
Updated every 4096 frames cycle.
4. DTSCD : “1” when DTS-CD bitstream is detected.  
Updated every DTS-CD sync cycle.
5. AUDION : “1” when the “AUDIO” bit in recovered channel status indicates “1”.  
Updated every block cycle.
6. PEM : “1” when “PEM” in recovered channel status indicates “1”.  
Updated every block cycle.
7. QINT : “1” when Q-subcode differ from old one, and keeps “1” until this register is read.  
Updated every sync code cycle for Q-subcode. Reading this register resets itself.
8. CINT : “1” when received C bits differ from old one, and keeps “1” until this register is read.  
Updated every block cycle. Reading this register resets itself.

Both INT0/1 are fixed to “L” when the PLL is off (CM1,0= “01”). Once the INT0 pin goes to “H”, this pin holds “H” for 1024/fs cycles(this value can be changed by EFH0/1 bits) after those events are removed. INT1 goes to “L” at the same time when those events are removed. Each INT0/1 pins can mask those eight events individually. Once PAR, QINT and CINT bit goes to “1”, those registers are held to “1” until those registers are read. While the AK4114 loses lock, registers regarding C-bit or U-bits are not initialized and keep previous value.

### 1. Parallel mode

In Parallel Mode, INT0 pin outputs the ORed signal between UNLOCK and PAR, INT1 pin outputs the ORed signal among AUTO, DTSCD and AUDION. Once INT0 pin goes ”H”, it maintains “H” for 1024/fs cycles after the all error events are removed. Table 12 shows the state of each output pins when the INT0/1 pin is “H”.

| Event (State of Internal Register) |     |      |       |        | Pin  |      |               |        |        |
|------------------------------------|-----|------|-------|--------|------|------|---------------|--------|--------|
| UNLOCK                             | PAR | AUTO | DTSCD | AUDION | INT0 | INT1 | SDTO          | V      | TX     |
| 1                                  | x   | x    | x     | x      | “H”  | -    | “L”           | “L”    | Output |
| 0                                  | 1   | x    | x     | x      |      |      | Previous Data | Output |        |
| 0                                  | 0   | x    | x     | x      | “L”  |      | Output        |        |        |
| x                                  | x   | 1    | x     | x      | -    | “H”  | -             | -      |        |
| x                                  | x   | x    | 1     | x      |      |      |               |        |        |
| x                                  | x   | x    | x     | 1      |      |      |               |        |        |
| x                                  | x   | 0    | 0     | 0      |      | “L”  |               |        |        |

Table 12. Error Handling (Parallel Mode) x: Don't care

## 2. Serial mode

In Serial Mode, INT0/1 pin output the ORed signal among those eight events. However, each events can be masked by each mask bits. When each bit masks those events, the event does not affect INT0/1 pin operation (those mask do not affect those registers (UNLOCK, PAR, etc.) themselves. Once INT0 pin goes “H”, it maintains “H” for 1024/fs cycles (this value can be changed by EFH0-1 bits) after the all events are removed. Once those PAR, QINT or CINT bit goes “1”, it holds “1” until reading those registers. While the AK4114 loses lock, the channel status and Q-subcode bits are not updated and holds the previous data. At initial state, INT0 outputs the ORed signal between UNLOCK and PAR, INT1 outputs the ORed signal among AUTO, DTSCD and AUDION.

| Register |     |      |       |        |     |      |      | Pin           |        |        |
|----------|-----|------|-------|--------|-----|------|------|---------------|--------|--------|
| UNLOCK   | PAR | AUTO | DTSCD | AUDION | PEM | QINT | CINT | SDTO          | V      | TX     |
| 1        | x   | x    | x     | x      | x   | x    | x    | “L”           | “L”    | Output |
| 0        | 1   | x    | x     | x      | x   | x    | x    | Previous Data | Output | Output |
| 0        | 0   | 1    | x     | x      | x   | x    | x    | Output        | Output | Output |
| 0        | 0   | x    | 1     | x      | x   | x    | x    | Output        | Output | Output |
| 0        | 0   | x    | x     | 1      | x   | x    | x    | Output        | Output | Output |
| 0        | 0   | x    | x     | x      | 1   | x    | x    | Output        | Output | Output |
| 0        | 0   | x    | x     | x      | x   | 1    | x    | Output        | Output | Output |
| 0        | 0   | x    | x     | x      | x   | x    | 1    | Output        | Output | Output |

Table 13. Error Handling (Serial Mode)

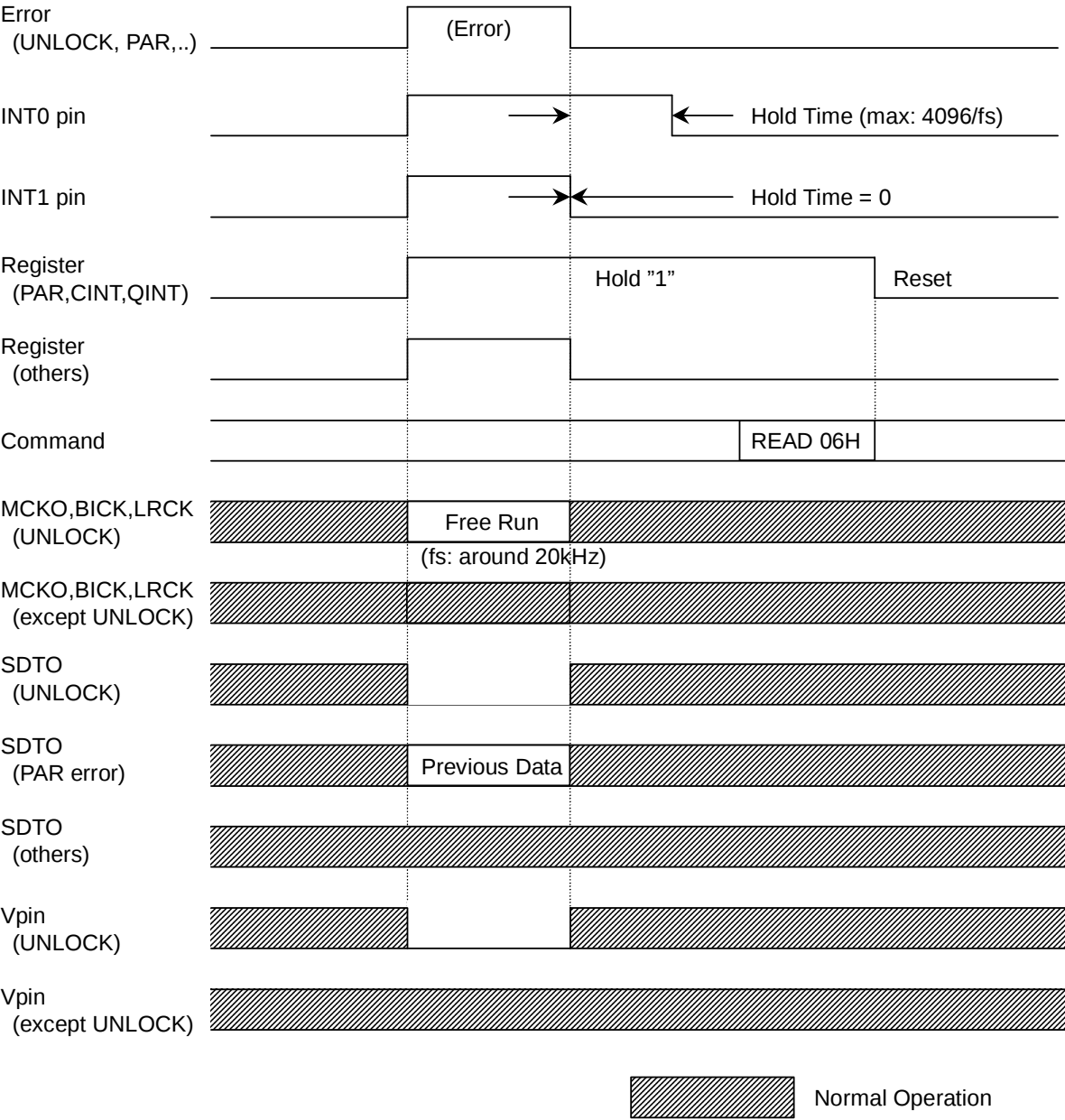


Figure 26. INT0/1 pin timing

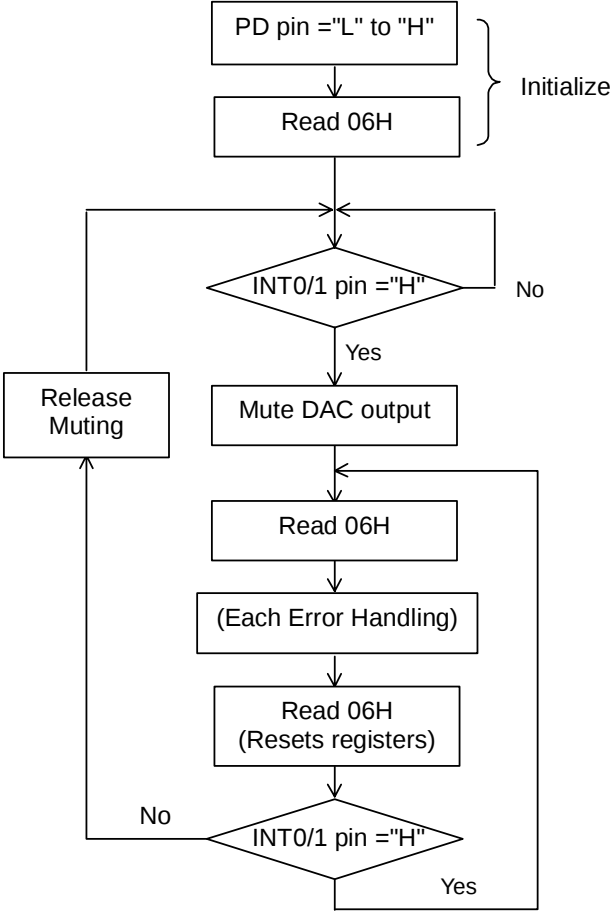


Figure 27. Error Handling Sequence Example 1

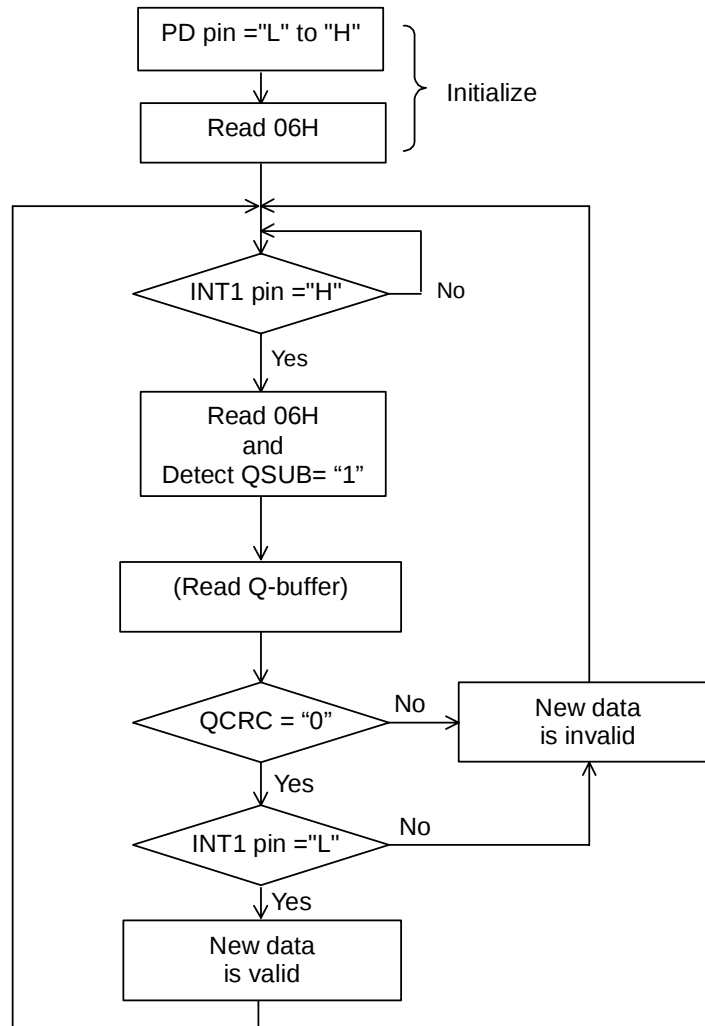


Figure 28. Error Handling Sequence Example (for Q/CINT)

## ■ Audio Serial Interface Format

The DIF0, DIF1 and DIF2 pins can select eight serial data formats as shown in Table 14. In all formats the serial data is MSB-first, 2's complement format. The SDTO is clocked out on the falling edge of BICK and the DAUX is latched on the rising edge of BICK. BICK outputs 64fs clock in Mode 0-5. Mode 6-7 are Slave Modes, and BICK is available up to 128fs at fs=48kHz. In the format equal or less than 20bit (Mode0-2), LSBs in sub-frame are truncated. In Mode 3-7, the last 4LSBs are auxiliary data (see Figure 29).

When the Parity Error, Biphase Error or Frame Length Error occurs in a sub-frame, AK4114 continues to output the last normal sub-frame data from SDTO repeatedly until the error is removed. When the Unlock Error occurs, AK4114 output "0" from SDTO. In case of using DAUX pin, the data is transformed and output from SDTO. DAUX pin is used in Clock Operation Mode 1, 3 and unlock state of Mode 2.

The input data format to DAUX should be left justified except in Mode5 and 7(Table 14). In Mode5 or 7, both the input data format of DAUX and output data format of SDTO are I<sup>2</sup>S. Mode6 and 7 are Slave Mode that is corresponding to the Master Mode of Mode4 and 5. In slave Mode, LRCK and BICK should be fed with synchronizing to MCKO1/2.

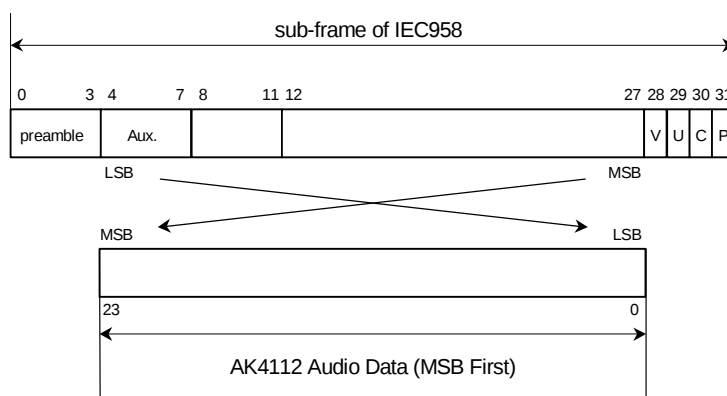


Figure 29. Bit configuration

| Mode | DIF2 | DIF1 | DIF0 | DAUX                    | SDTO                    | LRCK |     | BICK     |     |
|------|------|------|------|-------------------------|-------------------------|------|-----|----------|-----|
|      |      |      |      |                         |                         |      | I/O |          | I/O |
| 0    | 0    | 0    | 0    | 24bit, Left justified   | 16bit, Right justified  | H/L  | O   | 64fs     | O   |
| 1    | 0    | 0    | 1    | 24bit, Left justified   | 18bit, Right justified  | H/L  | O   | 64fs     | O   |
| 2    | 0    | 1    | 0    | 24bit, Left justified   | 20bit, Right justified  | H/L  | O   | 64fs     | O   |
| 3    | 0    | 1    | 1    | 24bit, Left justified   | 24bit, Right justified  | H/L  | O   | 64fs     | O   |
| 4    | 1    | 0    | 0    | 24bit, Left justified   | 24bit, Left justified   | H/L  | O   | 64fs     | O   |
| 5    | 1    | 0    | 1    | 24bit, I <sup>2</sup> S | 24bit, I <sup>2</sup> S | L/H  | O   | 64fs     | O   |
| 6    | 1    | 1    | 0    | 24bit, Left justified   | 24bit, Left justified   | H/L  | I   | 64-128fs | I   |
| 7    | 1    | 1    | 1    | 24bit, I <sup>2</sup> S | 24bit, I <sup>2</sup> S | L/H  | I   | 64-128fs | I   |

Default

Table 14. Audio data format

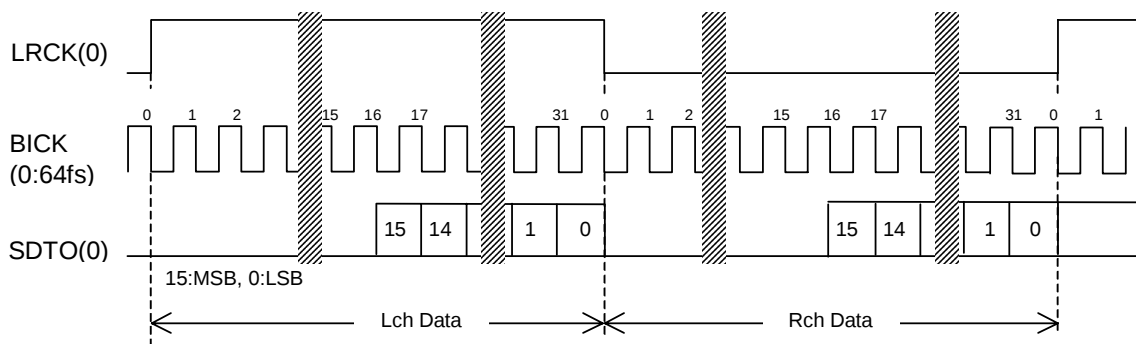


Figure 30. Mode 0 Timing

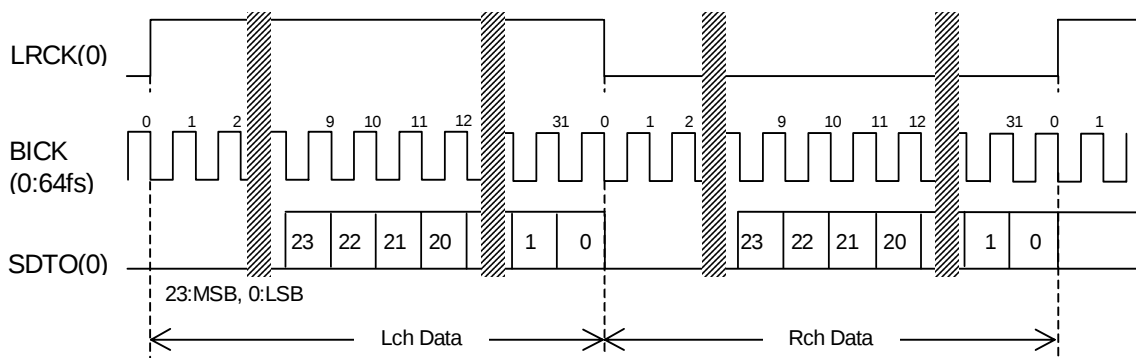


Figure 31. Mode 3 Timing

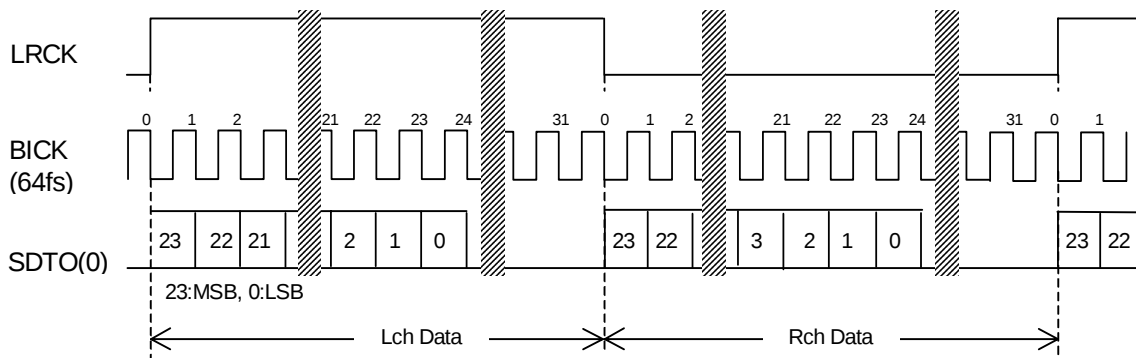


Figure 32. Mode 4, 6 Timing

Mode4 : LRCK, BICK : Output

Mode6 : LRCK, BICK : Input

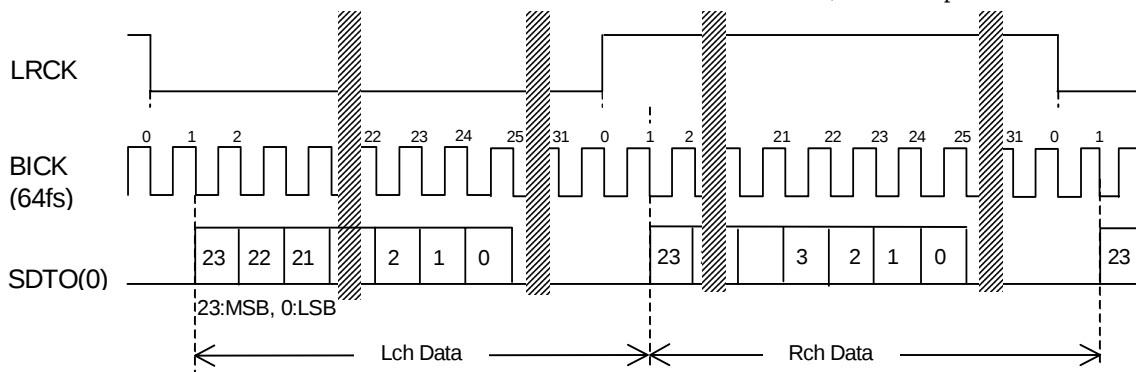


Figure 33. Mode 5, 7 Timing

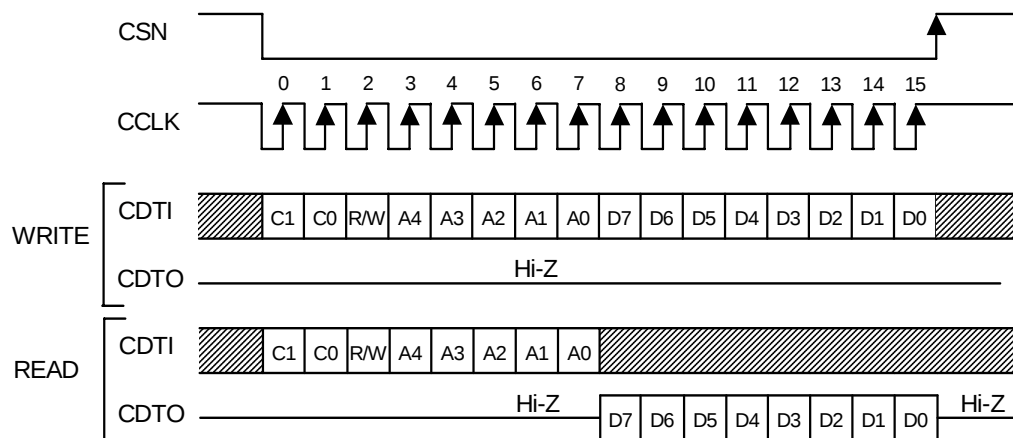
Mode5 : LRCK, BICK : Output

Mode7 : LRCK, BICK : Input

## ■ Serial Control Interface

### (1). 4-wire serial control mode (IIC= "L")

The internal registers may be either written or read by the 4-wire  $\mu$ P interface pins: CSN, CCLK, CDTI & CDTO. The data on this interface consists of Chip address (2bits, C1-0 are fixed to "00"), Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. For read operations, the CDTO output goes high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. PDN= "L" resets the registers to their default values. When the state of P/S pin is changed, the AK4114 should be reset by PDN= "L".



C1-C0: Chip Address (Fixed to "00")  
 R/W: READ/WRITE (0:READ, 1:WRITE)  
 A4-A0: Register Address  
 D7-D0: Control Data

Figure 34. 4-wire Serial Control I/F Timing

(2). I<sup>2</sup>C bus control mode (IIC= "H")

AK4114 supports the standard-mode I<sup>2</sup>C-bus (max : 100kHz). Then AK4114 can not be incorporated in a fast-mode I<sup>2</sup>C-bus system (max : 400kHz).

## (2)-1. Data transfer

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK4114 recognizes the START condition, the device interfaced to the bus waits for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by a STOP condition generated by the master device.

## (2)-1-1. Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW except for the START and the STOP condition.

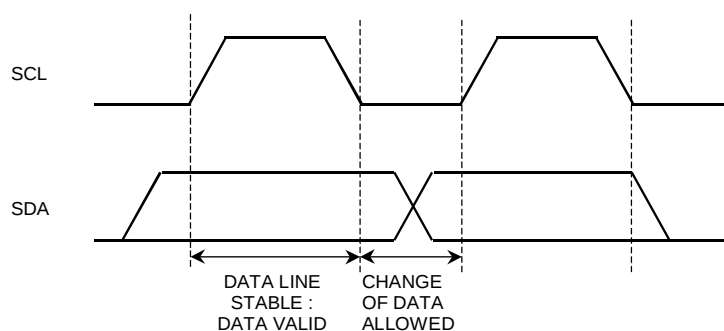


Figure 35. Data transfer

## (2)-1-2. START and STOP condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. All sequences start from the START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All sequences end by the STOP condition.

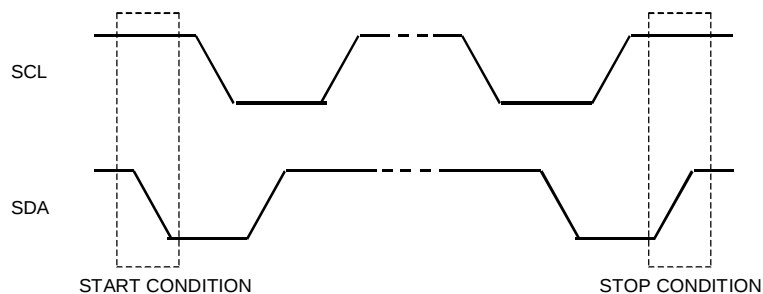
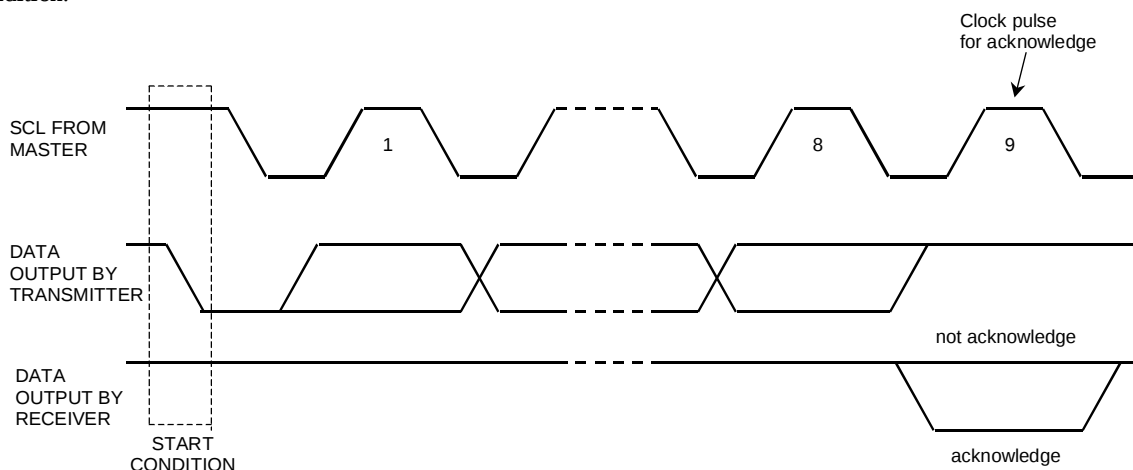


Figure 36. START and STOP conditions

## (2)-1-3. ACKNOWLEDGE

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable “L” during “H” period of this clock pulse. The AK4114 will generate an acknowledge after each byte has been received.

In the read mode, the slave, AK4114 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition.

Figure 37. Acknowledge on the I<sup>2</sup>C-bus

## (2)-1-4. FIRST BYTE

The first byte, which includes seven bits of slave address and one bit of R/W bit, is sent after the START condition. If the transmitted slave address matches an address for one of the device, the receiver who has been addressed pulls down the SDA line.

The most significant five bits of the slave address are fixed as “00100”. The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The hard-wired input pins (CAD1 pin and CAD0 pin) set them. The eighth bit (LSB) of the first byte (R/W bit) defines whether a write or read condition is requested by the master. A “1” indicates that the read operation is to be executed. A “0” indicates that the write operation is to be executed.

|   |   |   |   |   |      |      |     |
|---|---|---|---|---|------|------|-----|
| 0 | 0 | 1 | 0 | 0 | CAD1 | CAD0 | R/W |
|---|---|---|---|---|------|------|-----|

(Those CAD1/0 should match with CAD1/0 pins.)

Figure 38. The First Byte

## (2)-2. WRITE Operations

Set R/W bit = "0" for the WRITE operation of AK4114.

After receipt the start condition and the first byte, the AK4114 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4114. The format is MSB first, and those most significant 3-bits are "Don't care".

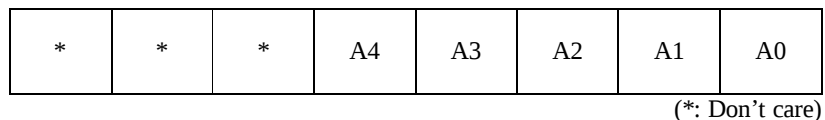


Figure 39. The Second Byte

After receipt the second byte, the AK4114 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8bits.

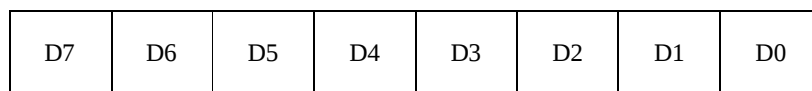


Figure 40. Byte structure after the second byte

The AK4114 is capable of more than one byte write operation by one sequence.

After receipt of the third byte, the AK4114 generates an acknowledge, and awaits the next data again. The master can transmit more than one words instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 1FH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

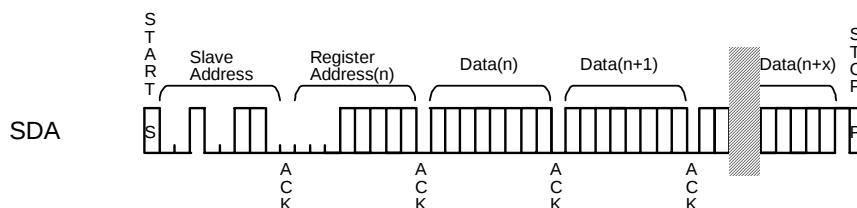


Figure 41. WRITE Operation

## (2)-3. READ Operations

Set R/W bit = "1" for the READ operation of AK4114.

After transmission of a data, the master can read next address's data by generating the acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 1FH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4114 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

## (2)-3-1. CURRENT ADDRESS READ

The AK4114 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1.

After receipt of the slave address with R/W bit set to "1", the AK4114 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4114 discontinues transmission

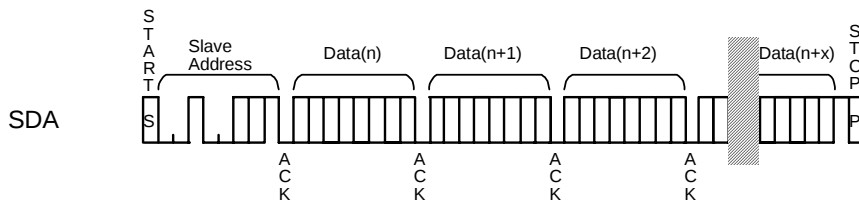


Figure 42. CURRENT ADDRESS READ

## (2)-3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation.

The master issues the start condition, slave address(R/W="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4114 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4114 discontinues transmission.

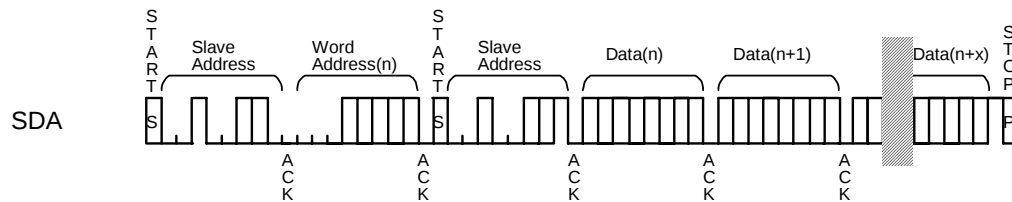


Figure 43. RANDOM READ

## ■ Register Map

| Addr | Register Name               | D7    | D6    | D5    | D4    | D3    | D2    | D1     | D0    |
|------|-----------------------------|-------|-------|-------|-------|-------|-------|--------|-------|
| 00H  | CLK & Power Down Control    | CS12  | BCU   | CM1   | CM0   | OCKS1 | OCKS0 | PWN    | RSTN  |
| 01H  | Format & De-em Control      | MONO  | DIF2  | DIF1  | DIF0  | DEAU  | DEM1  | DEM0   | DFS   |
| 02H  | Input/ Output Control 0     | TX1E  | OPS12 | OPS11 | OPS10 | TX0E  | OPS02 | OPS01  | OPS00 |
| 03H  | Input/ Output Control 1     | EFH1  | EFH0  | UDIT  | TLR   | DIT   | IPS2  | IPS1   | IPS0  |
| 04H  | INT0 MASK                   | MQIT0 | MAUT0 | MCIT0 | MULK0 | MDTS0 | MPE0  | MAUD0  | MPAR0 |
| 05H  | INT1 MASK                   | MQIT1 | MAUT1 | MCIT1 | MULK1 | MDTS1 | MPE1  | MAUD1  | MPAR1 |
| 06H  | Receiver status 0           | QINT  | AUTO  | CINT  | UNLCK | DTSCD | PEM   | AUDION | PAR   |
| 07H  | Receiver status 1           | FS3   | FS2   | FS1   | FS0   | 0     | V     | QCRC   | CCRC  |
| 08H  | RX Channel Status Byte 0    | CR7   | CR6   | CR5   | CR4   | CR3   | CR2   | CR1    | CR0   |
| 09H  | RX Channel Status Byte 1    | CR15  | CR14  | CR13  | CR12  | CR11  | CR10  | CR9    | CR8   |
| 0AH  | RX Channel Status Byte 2    | CR23  | CR22  | CR21  | CR20  | CR19  | CR18  | CR17   | CR16  |
| 0BH  | RX Channel Status Byte 3    | CR31  | CR30  | CR29  | CR28  | CR27  | CR26  | CR25   | CR24  |
| 0CH  | RX Channel Status Byte 4    | CR39  | CR38  | CR37  | CR36  | CR35  | CR34  | CR33   | CR32  |
| 0DH  | TX Channel Status Byte 0    | CT7   | CT6   | CT5   | CT4   | CT3   | CT2   | CT1    | CT0   |
| 0EH  | TX Channel Status Byte 1    | CT15  | CT14  | CT13  | CT12  | CT11  | CT10  | CT9    | CT8   |
| 0FH  | TX Channel Status Byte 2    | CT23  | CT22  | CT21  | CT20  | CT19  | CT18  | CT17   | CT16  |
| 10H  | TX Channel Status Byte 3    | CT31  | CT30  | CT29  | CT28  | CT27  | CT26  | CT25   | CT24  |
| 11H  | TX Channel Status Byte 4    | CT39  | CT39  | CT39  | CT39  | CT39  | CT39  | CT39   | CT32  |
| 12H  | Burst Preamble Pc Byte 0    | PC7   | PC6   | PC5   | PC4   | PC3   | PC2   | PC1    | PC0   |
| 13H  | Burst Preamble Pc Byte 1    | PC15  | PC14  | PC13  | PC12  | PC11  | PC10  | PC9    | PC8   |
| 14H  | Burst Preamble Pd Byte 0    | PD7   | PD6   | PD5   | PD4   | PD3   | PD2   | PD1    | PD0   |
| 15H  | Burst Preamble Pd Byte 1    | PD15  | PD14  | PD13  | PD12  | PD11  | PD10  | PD9    | PD8   |
| 16H  | Q-subcode Address / Control | Q9    | Q8    | Q7    | Q6    | Q5    | Q4    | Q3     | Q2    |
| 17H  | Q-subcode Track             | Q17   | Q16   | Q15   | Q14   | Q13   | Q12   | Q11    | Q10   |
| 18H  | Q-subcode Index             | Q25   | Q24   | Q23   | Q22   | Q21   | Q20   | Q19    | Q18   |
| 19H  | Q-subcode Minute            | Q33   | Q32   | Q31   | Q30   | Q29   | Q28   | Q27    | Q26   |
| 1AH  | Q-subcode Second            | Q41   | Q40   | Q39   | Q38   | Q37   | Q36   | Q35    | Q34   |
| 1BH  | Q-subcode Frame             | Q49   | Q48   | Q47   | Q46   | Q45   | Q44   | Q43    | Q42   |
| 1CH  | Q-subcode Zero              | Q57   | Q56   | Q55   | Q54   | Q53   | Q52   | Q51    | Q50   |
| 1DH  | Q-subcode ABS Minute        | Q65   | Q64   | Q63   | Q62   | Q61   | Q60   | Q59    | Q58   |
| 1EH  | Q-subcode ABS Second        | Q73   | Q72   | Q71   | Q70   | Q69   | Q68   | Q67    | Q66   |
| 1FH  | Q-subcode ABS Frame         | Q81   | Q80   | Q79   | Q78   | Q77   | Q76   | Q75    | Q74   |

When PDN pin goes “L”, the registers are initialized to their default values.

When RSTN bit goes “0”, the internal timing is reset and the registers are initialized to their default values.

All data can be written to the register even if PWN bit is “0”.

## ■ Register Definitions

### Reset & Initialize

| Addr | Register Name            | D7   | D6  | D5  | D4  | D3    | D2    | D1  | D0   |
|------|--------------------------|------|-----|-----|-----|-------|-------|-----|------|
| 00H  | CLK & Power Down Control | CS12 | BCU | CM1 | CM0 | OCKS1 | OCKS0 | PWN | RSTN |
|      | R/W                      | R/W  | R/W | R/W | R/W | R/W   | R/W   | R/W | R/W  |
|      | Default                  | 0    | 1   | 0   | 0   | 0     | 0     | 1   | 1    |

RSTN: Timing Reset & Register Initialize

0: Reset & Initialize

1: Normal Operation

PWN: Power Down

0: Power Down

1: Normal Operation

OCKS1-0: Master Clock Frequency Select

CM1-0: Master Clock Operation Mode Select

BCU: Block start & C/U Output Mode

When BCU=1, the three Output Pins(BOUT, COUT, UOUT) become to be enabled.

The block signal goes high at the start of frame 0 and remains high until the end of frame 31.

CS12: Channel Status Select

0: Channel 1

1: Channel 2

Selects which channel status is used to derive C-bit buffers, AUDION, PEM, FS3, FS2, FS1, FS0, Pc and Pd. The de-emphasis filter is controlled by channel 1 in the Parallel Mode.

### Format & De-emphasis Control

| Addr | Register Name          | D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0  |
|------|------------------------|------|------|------|------|------|------|------|-----|
| 01H  | Format & De-em Control | MONO | DIF2 | DIF1 | DIF0 | DEAU | DEM1 | DEM0 | DFS |
|      | R/W                    | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W |
|      | Default                | 0    | 1    | 1    | 0    | 1    | 0    | 1    | 0   |

DFS: 96kHz De-emphasis Control

DEM1-0: 32, 44.1, 48kHz De-emphasis Control (see Table 8.)

DEAU: De-emphasis Auto Detect Enable

0: Disable

1: Enable

DIF2-0: Audio Data Format Control (see Table 14.)

MONO: Double sampling frequency mode enable

0: Stereo mode

1: Mono mode

**Input/Output Control**

| Addr | Register Name           | D7   | D6    | D5    | D4    | D3   | D2    | D1    | D0    |
|------|-------------------------|------|-------|-------|-------|------|-------|-------|-------|
| 02H  | Input/ Output Control 0 | TX1E | OPS12 | OPS11 | OPS10 | TX0E | OPS02 | OPS01 | OPS00 |
|      | R/W                     | R/W  | R/W   | R/W   | R/W   | R/W  | R/W   | R/W   | R/W   |
|      | Default                 | 1    | 0     | 0     | 0     | 1    | 0     | 0     | 0     |

OPS02-00: Output Through Data Select for TX0 pin

OPS12-10: Output Through Data Select for TX1 pin

TX0E: TX0 Output Enable

0: Disable. TX0 outputs “L”.

1: Enable

TX1E: TX1 Output Enable

0: Disable. TX1 outputs “L”.

1: Enable

| Addr | Register Name           | D7   | D6   | D5   | D4  | D3  | D2   | D1   | D0   |
|------|-------------------------|------|------|------|-----|-----|------|------|------|
| 03H  | Input/ Output Control 1 | EFH1 | EFH0 | UDIT | TLR | DIT | IPS2 | IPS1 | IPS0 |
|      | R/W                     | R/W  | R/W  | R/W  | R/W | R/W | R/W  | R/W  | R/W  |
|      | Default                 | 0    | 1    | 0    | 0   | 1   | 0    | 0    | 0    |

IPS2-0: Input Recovery Data Select

DIT: Through data/Transmit data select for TX1 pin

0: Through data (RX data).

1: Transmit data (DAUX data).

TLR: Double sampling frequency mode channel select for DIT(stereo)

0: L channel

1: R channel

UDIT: U bit control for DIT

0: U bit is fixed to “0”

1: Recovered U bit is used for DIT (loop mode for U bit)

EFH1-0: Interrupt 0 Pin Hold Count Select

00: 512 LRCK

01: 1024 LRCK

10: 2048 LRCK

11: 4096 LRCK

**Mask Control for INT0**

| Addr | Register Name | D7   | D6   | D5   | D4   | D3    | D2   | D1   | D0   |
|------|---------------|------|------|------|------|-------|------|------|------|
| 04H  | INT0 MASK     | MQI0 | MAT0 | MCI0 | MUL0 | MDTS0 | MPE0 | MAN0 | MPR0 |
|      | R/W           | R/W  | R/W  | R/W  | R/W  | R/W   | R/W  | R/W  | R/W  |
|      | Default       | 1    | 1    | 1    | 0    | 1     | 1    | 1    | 0    |

MPR0: Mask Enable for PAR bit  
 MAN0: Mask Enable for AUDN bit  
 MPE0: Mask Enable for PEM bit  
 MDTS0: Mask Enable for DTSCD bit  
 MUL0: Mask Enable for UNLOCK bit  
 MCI0: Mask Enable for CINT bit  
 MAT0: Mask Enable for AUTO bit  
 MQI0: Mask Enable for QINT bit

0: Mask disable  
 1: Mask enable

**Mask Control for INT1**

| Addr | Register Name | D7   | D6   | D5   | D4   | D3    | D2   | D1   | D0   |
|------|---------------|------|------|------|------|-------|------|------|------|
| 05H  | INT1 MASK     | MQI1 | MAT1 | MCI1 | MUL1 | MDTS1 | MPE1 | MAN1 | MPR1 |
|      | R/W           | R/W  | R/W  | R/W  | R/W  | R/W   | R/W  | R/W  | R/W  |
|      | Default       | 1    | 0    | 1    | 1    | 0     | 1    | 0    | 1    |

MPR1: Mask Enable for PAR bit  
 MAN1: Mask Enable for AUDN bit  
 MPE1: Mask Enable for PEM bit  
 MDTS1: Mask Enable for DTSCD bit  
 MUL1: Mask Enable for UNLOCK0 bit  
 MCI1: Mask Enable for CINT bit  
 MAT1: Mask Enable for AUTO bit  
 MQI1: Mask Enable for QINT bit

0: Mask disable  
 1: Mask enable

**Receiver Status 0**

| Addr | Register Name     | D7   | D6   | D5   | D4    | D3    | D2  | D1     | D0  |
|------|-------------------|------|------|------|-------|-------|-----|--------|-----|
| 06H  | Receiver status 0 | QINT | AUTO | CINT | UNLCK | DTSCD | PEM | AUDION | PAR |
|      | R/W               | RD   | RD   | RD   | RD    | RD    | RD  | RD     | RD  |
|      | Default           | 0    | 0    | 0    | 0     | 0     | 0   | 0      | 0   |

PAR: Parity Error or Biphase Error Status

0: No Error

1: Error

It is "1" if Parity Error or Biphase Error is detected in the sub-frame.

AUDION: Audio Bit Output

0: Audio

1: Non Audio

This bit is made by encoding channel status bits.

PEM: Pre-emphasis Detect.

0: OFF

1: ON

This bit is made by encoding channel status bits.

DTSCD: DTS-CD Auto Detect

0: No detect

1: Detect

UNLCK: PLL Lock Status

0: Locked

1: Out of Lock

CINT: Channel Status Buffer Interrupt

0: No change

1: Changed

AUTO: Non-PCM Auto Detect

0: No detect

1: Detect

QINT: Q-subcode Buffer Interrupt

0: No change

1: Changed

QINT, CINT and PAR bits are initialized when 06H is read.

**Receiver Status 1**

| Addr | Register Name     | D7  | D6  | D5  | D4  | D3 | D2 | D1   | D0   |
|------|-------------------|-----|-----|-----|-----|----|----|------|------|
| 07H  | Receiver status 1 | FS3 | FS2 | FS1 | FS0 | 0  | V  | QCRC | CCRC |
|      | R/W               | RD  | RD  | RD  | RD  | RD | RD | RD   | RD   |
|      | Default           | 0   | 0   | 0   | 1   | 0  | 0  | 0    | 0    |

CCRC: Cyclic Redundancy Check for Channel Status

0: No Error

1: Error

QCRC: Cyclic Redundancy Check for Q-subcode

0: No Error

1: Error

V: Validity of channel status

0: Valid

1: Invalid

FS3-0: Sampling Frequency detection (see Table 4.)

**Receiver Channel Status**

| Addr    | Register Name            | D7              | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|---------|--------------------------|-----------------|------|------|------|------|------|------|------|
| 08H     | RX Channel Status Byte 0 | CR7             | CR6  | CR5  | CR4  | CR3  | CR2  | CR1  | CR0  |
| 09H     | RX Channel Status Byte 1 | CR15            | CR14 | CR13 | CR12 | CR11 | CR10 | CR9  | CR8  |
| 0AH     | RX Channel Status Byte 2 | CR23            | CR22 | CR21 | CR20 | CR19 | CR18 | CR17 | CR16 |
| 0BH     | RX Channel Status Byte 3 | CR31            | CR30 | CR29 | CR28 | CR27 | CR26 | CR25 | CR24 |
| 0CH     | RX Channel Status Byte 4 | CR39            | CR38 | CR37 | CR36 | CR35 | CR34 | CR33 | CR32 |
| R/W     |                          | RD              |      |      |      |      |      |      |      |
| Default |                          | Not initialized |      |      |      |      |      |      |      |

CR39-0: Receiver Channel Status Byte 4-0

**Transmitter Channel Status**

| Addr    | Register Name            | D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|---------|--------------------------|------|------|------|------|------|------|------|------|
| 0DH     | TX Channel Status Byte 0 | CT7  | CT6  | CT5  | CT4  | CT3  | CT2  | CT1  | CT0  |
| 0EH     | TX Channel Status Byte 1 | CT15 | CT14 | CT13 | CT12 | CT11 | CT10 | CT9  | CT8  |
| 0FH     | TX Channel Status Byte 2 | CT23 | CT22 | CT21 | CT20 | CT19 | CT18 | CT17 | CT16 |
| 10H     | TX Channel Status Byte 3 | CT31 | CT30 | CT29 | CT28 | CT27 | CT26 | CT25 | CT24 |
| 11H     | TX Channel Status Byte 3 | CT39 | CT38 | CT37 | CT36 | CT35 | CT34 | CT33 | CT32 |
| R/W     |                          | R/W  |      |      |      |      |      |      |      |
| Default |                          | 0    |      |      |      |      |      |      |      |

CT39-0: Transmitter Channel Status Byte 4-0

**Burst Preamble Pc/Pd in non-PCM encoded Audio Bitstreams**

| Addr    | Register Name            | D7              | D6   | D5   | D4   | D3   | D2   | D1  | D0  |
|---------|--------------------------|-----------------|------|------|------|------|------|-----|-----|
| 12H     | Burst Preamble Pc Byte 0 | PC7             | PC6  | PC5  | PC4  | PC3  | PC2  | PC1 | PC0 |
| 13H     | Burst Preamble Pc Byte 1 | PC15            | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 |
| 14H     | Burst Preamble Pd Byte 0 | PD7             | PD6  | PD5  | PD4  | PD3  | PD2  | PD1 | PD0 |
| 15H     | Burst Preamble Pd Byte 1 | PD15            | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| R/W     |                          | RD              |      |      |      |      |      |     |     |
| Default |                          | Not initialized |      |      |      |      |      |     |     |

PC15-0: Burst Preamble Pc Byte 0 and 1

PD15-0: Burst Preamble Pd Byte 0 and 1

**Q-subcode Buffer**

| Addr    | Register Name               | D7              | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|---------|-----------------------------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| 16H     | Q-subcode Address / Control | Q9              | Q8  | Q7  | Q6  | Q5  | Q4  | Q3  | Q2  |
| 17H     | Q-subcode Track             | Q17             | Q16 | Q15 | Q14 | Q13 | Q12 | Q11 | Q10 |
| 18H     | Q-subcode Index             | Q25             | Q24 | Q23 | Q22 | Q21 | Q20 | Q19 | Q18 |
| 19H     | Q-subcode Minute            | Q33             | Q32 | Q31 | Q30 | Q29 | Q28 | Q27 | Q26 |
| 1AH     | Q-subcode Second            | Q41             | Q40 | Q39 | Q38 | Q37 | Q36 | Q35 | Q34 |
| 1BH     | Q-subcode Frame             | Q49             | Q48 | Q47 | Q46 | Q45 | Q44 | Q43 | Q42 |
| 1CH     | Q-subcode Zero              | Q57             | Q56 | Q55 | Q54 | Q53 | Q52 | Q51 | Q50 |
| 1DH     | Q-subcode ABS Minute        | Q65             | Q64 | Q63 | Q62 | Q61 | Q60 | Q59 | Q58 |
| 1EH     | Q-subcode ABS Second        | Q73             | Q72 | Q71 | Q70 | Q69 | Q68 | Q67 | Q66 |
| 1FH     | Q-subcode ABS Frame         | Q81             | Q80 | Q79 | Q78 | Q77 | Q76 | Q75 | Q74 |
| R/W     |                             | RD              |     |     |     |     |     |     |     |
| Default |                             | Not initialized |     |     |     |     |     |     |     |

■ Burst Preambles in non-PCM Bitstreams

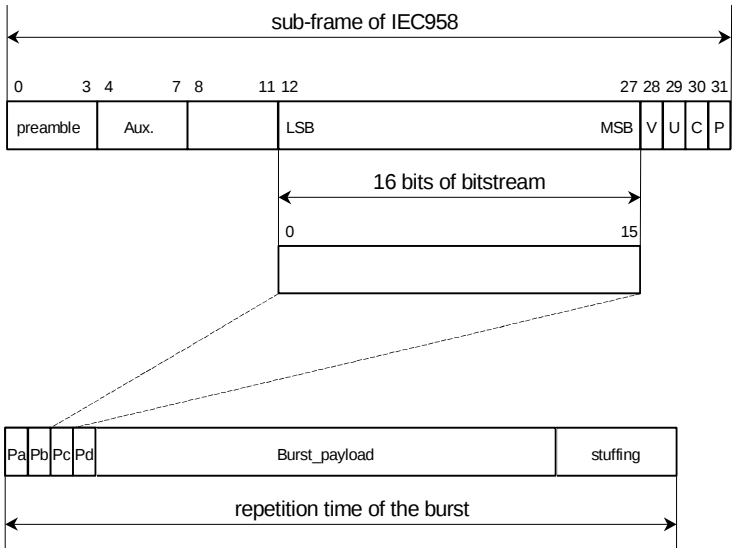


Figure 44. Data structure in IEC60958

| Preamble word | Length of field | Contents    | Value           |
|---------------|-----------------|-------------|-----------------|
| Pa            | 16 bits         | sync word 1 | 0xF872          |
| Pb            | 16 bits         | sync word 2 | 0x4E1F          |
| Pc            | 16 bits         | Burst info  | See Table 16    |
| Pd            | 16 bits         | Length code | Numbers of bits |

Table 15. Burst preamble words

| Bits of Pc | Value | Contents                                                        | Repetition time of burst<br>in IEC60958 frames |
|------------|-------|-----------------------------------------------------------------|------------------------------------------------|
| 0-4        | 0     | data type<br>NULL data                                          | ≤4096                                          |
|            | 1     | Dolby AC-3 data                                                 | 1536                                           |
|            | 2     | reserved                                                        |                                                |
|            | 3     | PAUSE                                                           |                                                |
|            | 4     | MPEG-1 Layer1 data                                              | 384                                            |
|            | 5     | MPEG-1 Layer2 or 3 data or MPEG-2 without extension             | 1152                                           |
|            | 6     | MPEG-2 data with extension                                      | 1152                                           |
|            | 7     | MPEG-2 AAC ADTS                                                 | 1024                                           |
|            | 8     | MPEG-2, Layer1 Low sample rate                                  | 384                                            |
|            | 9     | MPEG-2, Layer2 or 3 Low sample rate                             | 1152                                           |
|            | 10    | reserved                                                        |                                                |
|            | 11    | DTS type I                                                      | 512                                            |
|            | 12    | DTS type II                                                     | 1024                                           |
|            | 13    | DTS type III                                                    | 2048                                           |
|            | 14    | ATRAC                                                           | 512                                            |
|            | 15    | ATRAC2/3                                                        | 1024                                           |
|            | 16-31 | reserved                                                        |                                                |
| 5, 6       | 0     | reserved, shall be set to "0"                                   |                                                |
| 7          | 0     | error-flag indicating a valid burst_payload                     |                                                |
|            | 1     | error-flag indicating that the burst_payload may contain errors |                                                |
| 8-12       |       | data type dependent info                                        |                                                |
| 13-15      | 0     | bit stream number, shall be set to "0"                          |                                                |

Table 16. Fields of burst info Pc

## ■ Non-PCM Bitstream timing

1) When Non-PCM preamble is not coming within 4096 frames,

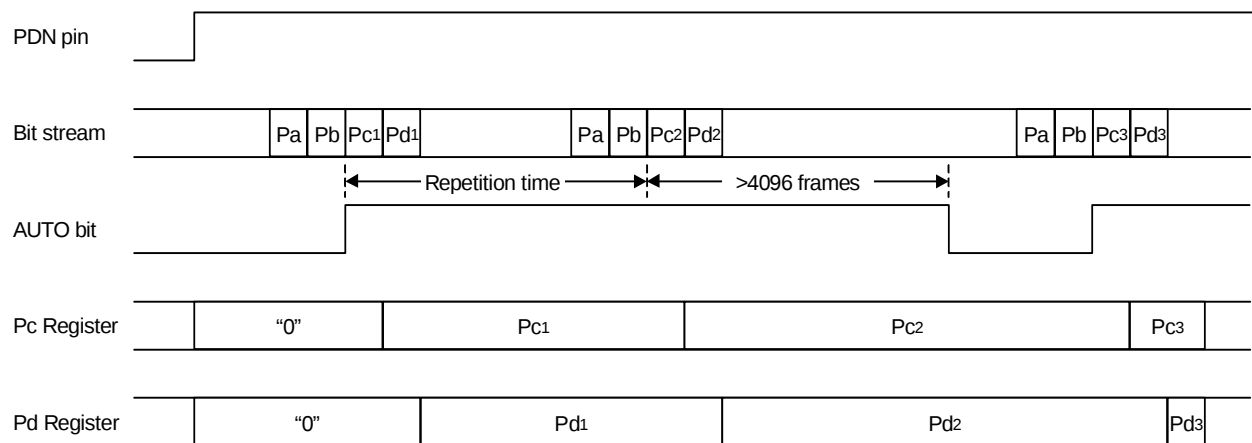


Figure 45. Timing example 1

2) When Non-PCM bitstream stops (when MULK0=0),

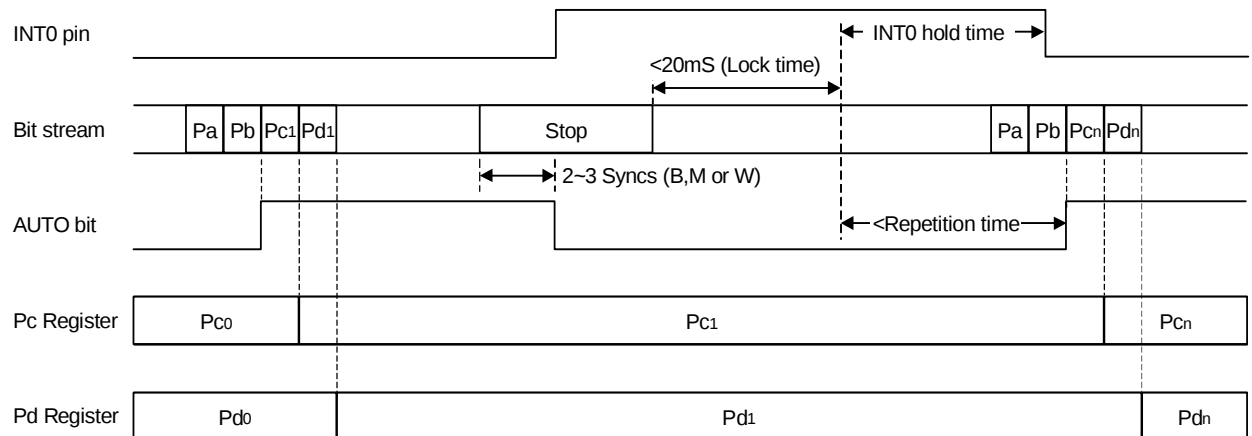


Figure 46. Timing example 2

# SYSTEM DESIGN

Figure 47 shows the example of system connection diagram for Serial Mode.

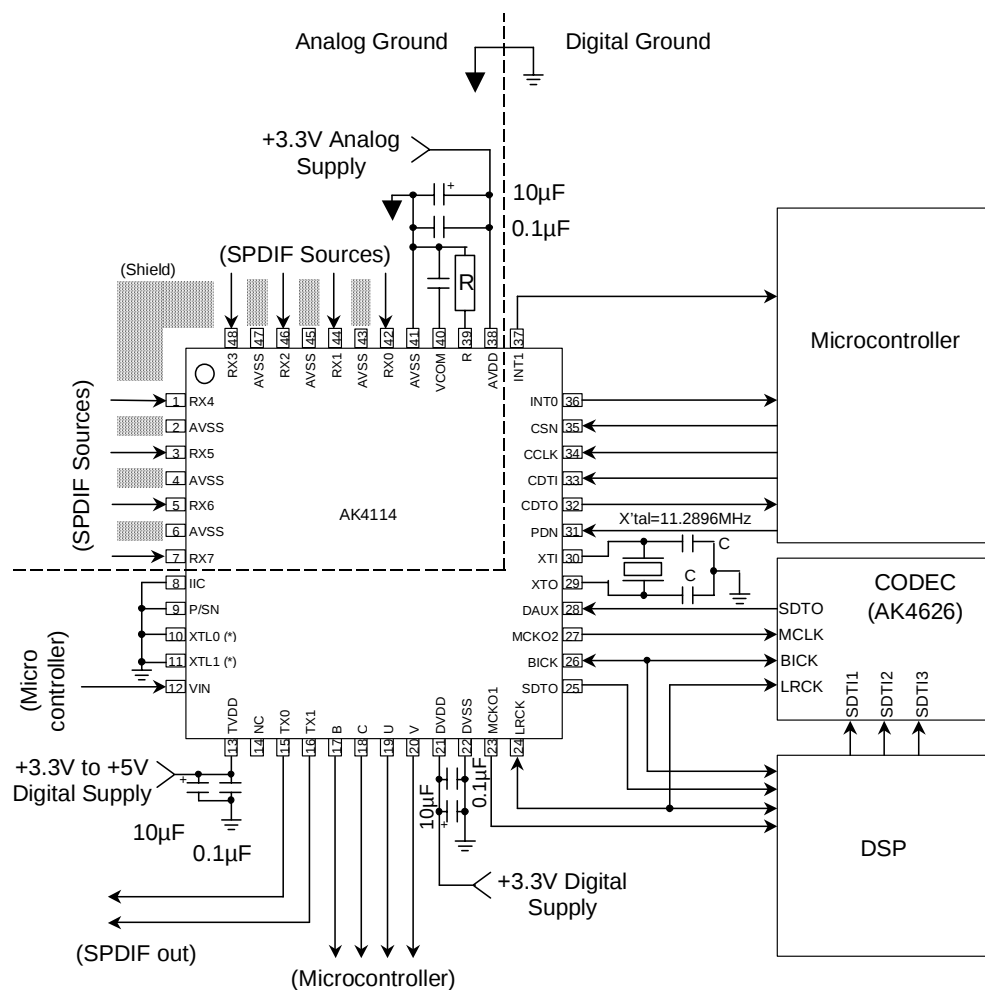


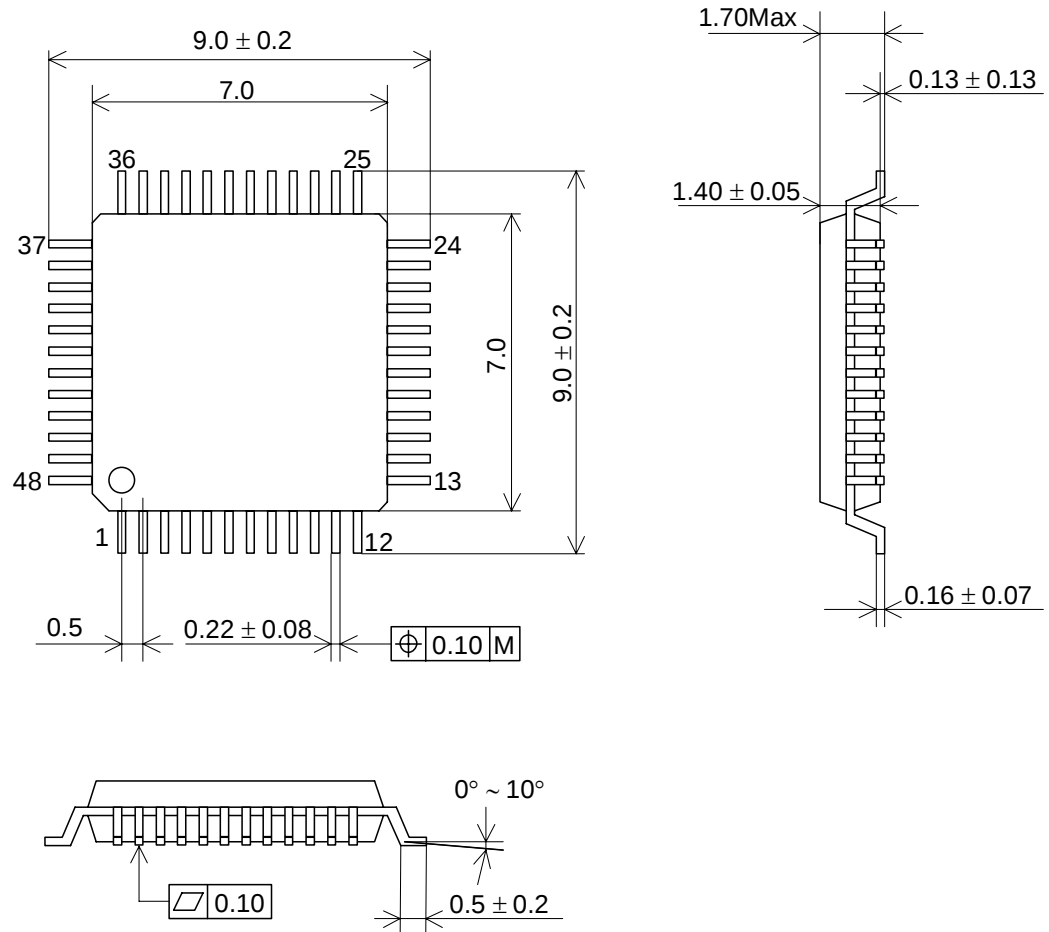
Figure 47. Typical Connection Diagram (Serial Mode)

## Notes:

- For setting of XTL0 and XTL1, refer the Table 3.
- "C" depends on the crystal.
- AVSS and DVSS must be connected the same ground plane.
- Digital signals, especially clocks, should be kept away from the R pin in order to avoid an effect to the clock jitter performance.

## PACKAGE

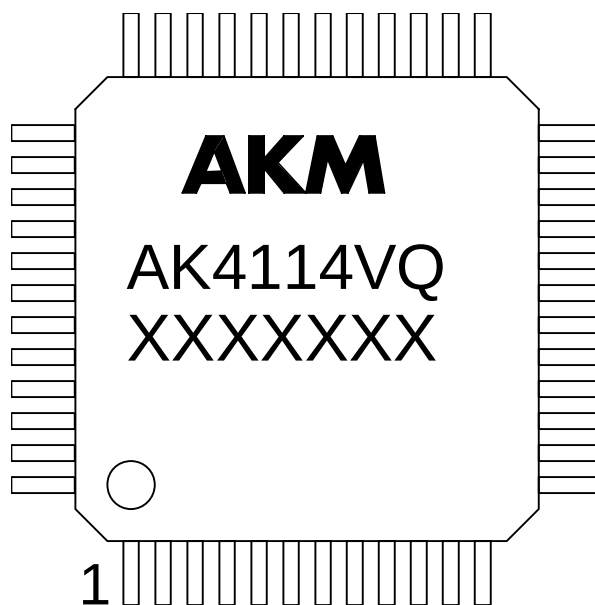
## 48pin LQFP(Unit:mm)



### Material & Lead finish

Package molding compound: Epoxy  
 Lead frame material: Cu  
 Lead frame surface treatment: Solder (Pb free) plate

|                |
|----------------|
| <b>MARKING</b> |
|----------------|



XXXXXXXX: Date code identifier

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