# AK2345

## FRS CTCSS Encoder/Decoder

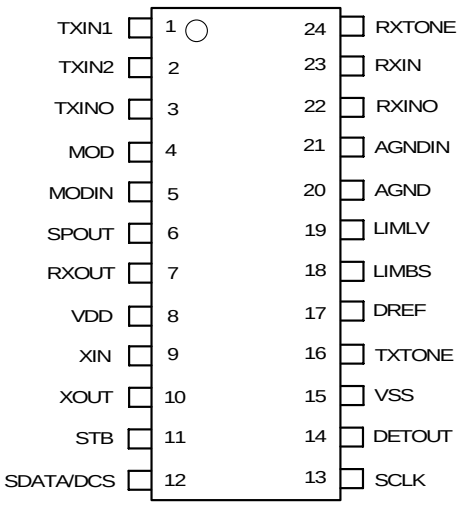
## Features

1. CTCSS (Continuous Tone Controlled Squelch System) Encoder/Decoder.
2. Programmable for up to 50 CTCSS frequencies.
3. Integrated CTCSS signal elimination filter.
4. Built-in Adder TX CTCSS/CDCSS and voice signal.
5. Built-in high speed CTCSS Decoder.
6. Conform to CDCSS. (Continuous Digital Controlled Squelch System)
7. Integrated voice signal circuits such as a limiter, splatter filter, etc.
8. Built-in (3.6864 MHz or 4.194304 MHz) oscillator circuit with crystal oscillator. (Page 25)
9. Control register controlled via serial interface.
10. CMOS Process low voltage operation. (1.8V…5.5V)
11. Compact plastic package is used. (24 pin VSOP)

## Description

The AK2345 is an IC which supports CTCSS (Continuous Tone Controlled Squelch System), compatible with the TIA/EIA-603 standard.
A single CTCSS may be selected from among 50 different frequencies within a range of from 67 to 254.1 Hz. By sending that CTCSS simultaneously with the voice signal during transmission, and by setting the audio circuit so that it operates only when a CTCSS of that frequency is detected, it is possible to have multiple communications on the same radio frequency.
TX has a built-in Adder CTCSS and voice signal, and RX has a built-in high-speed CTCSS Decoder respectively.
Voice signal filters, a limiter, op-amp, and other circuits are integrated, making it possible to configure a radio base band unit, especially FRS from a single chip.

■ Pin assignment



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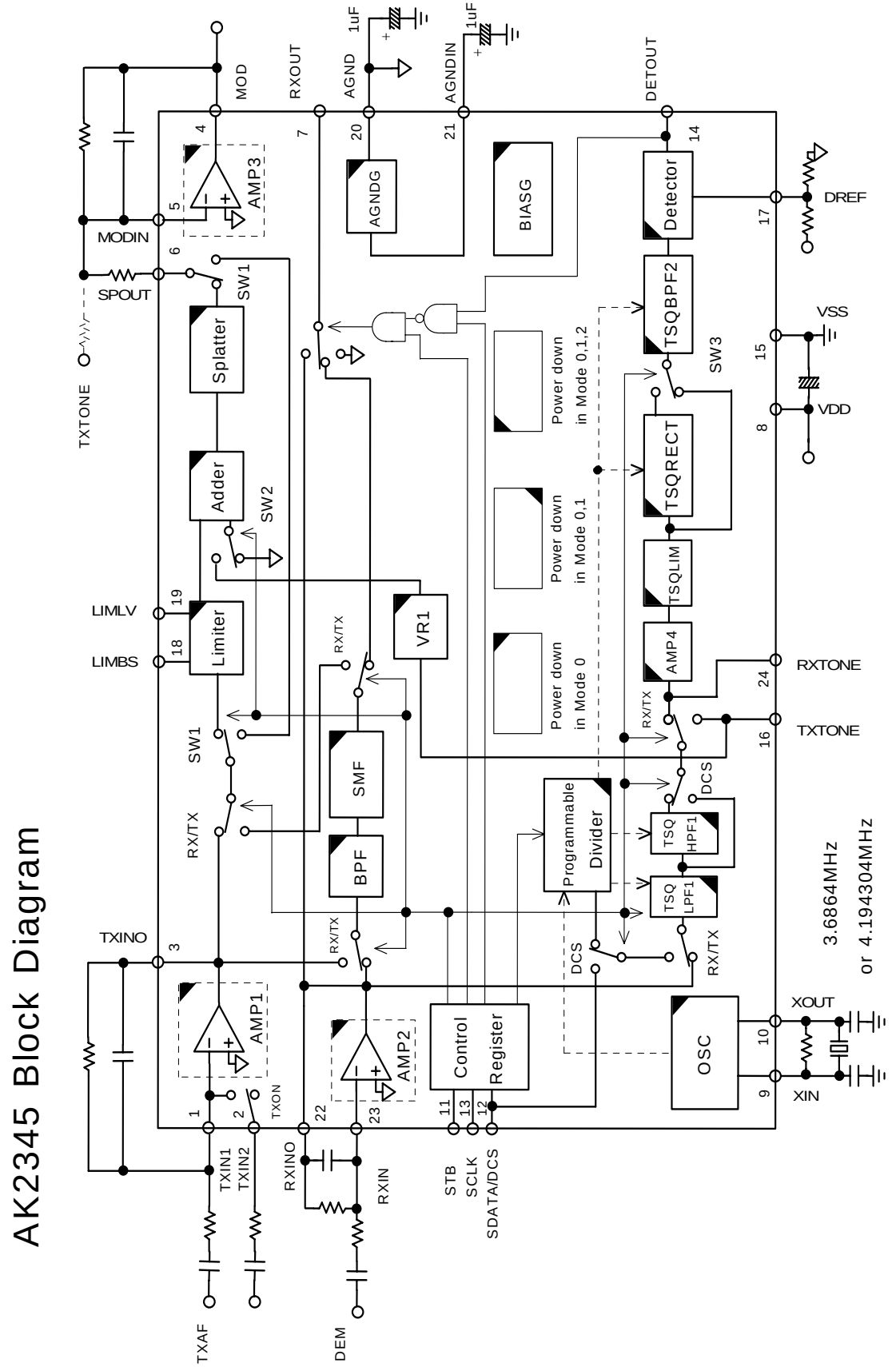
# Block Diagram



# Circuit Configuration

| Block | Function |
|---|---|
| AMP1 | Operational amplifier for adjusting the transmitting voices signal gain and preventing SCF aliasing in subsequent stages. Set the gain at 30 dB or lower and the cut-off frequency at about 10 kHz by connecting external resistors and capacitors. |
| AMP2 | Operational amplifier for adjusting the receiving voice signals and CTCSS/CDCSS signal gain, and preventing SCF aliasing in subsequent stages. Set the gain at 20 dB or lower and the cut-off frequency at about 10 kHz by connecting external resistors and capacitors. |
| BPF | SCF circuit, which limits the band of input voice signals. This prevents voice signals below 300 Hz from having an adverse effect on CTCSS/CDCSS signals during transmitting. The CTCSS/CDCSS signal is remove during receiving and only the voice signal is output. |
| SMF | This eliminates the high frequency component and clock component generated by BPF. |
| Limiter | An amplitude limiting circuit for the purpose of inhibiting frequency deviation of the modulation signals. The DC voltage applied to the LIMLV pin can adjust the limit level. If the LIMLV pin is made open, the limit level is a predetermined level. |
| Adder | Circuit which is adding TX CTCSS signal to voice signal internally. |
| VR1 | The volume to control the amplitude of the TX CTCSS signal level which add to the voice signal internally with “Adder”. The adjustment coarse range is -10dB or -20dB, fine range is -8.5dB to +7.0dB by 0.5dB step. |
| Splatter | A SCF circuit which removes the component above 3 kHz included in the limiter output signal. |
| AMP3 | An operational amplifier for the purpose of configuring a smoothing filter for the transmitting SCF circuit. Set the gain at 0 dB and the cut-off frequency at about 10 kHz by connecting external resistors and capacitors. |
| Control Register | Circuit which is used to input and store control signals for switching the CTCSS/CDCSS frequency, transmit/receive, etc. |
| Programmable Divider | Circuit which generates the clock signals required for generating and detecting the 50 CTCSS signal frequencies |
| OSC | Circuit which generates the reference clock with external resistors and capacitors. |
| TSQHPF1<br>TSQLPF1 | Programmable filter which changes rectangular waves to sine wave. During receiving, it extracts CTCSS/CDCSS from the received signals. |
| AMP4 | Operational amplifier which amplifies CTCSS signal from TSQHPF1 and supplies it to TSQLIM. The gain can be set by serial control register. |
| TSQLIM | Circuit which performs amplitude limiting of CTCSS signal. |
| TSQRECT | Circuit which performs for high-speed CTCSS decoder. |
| TSQBPF2 | Narrow band-pass filter for differentiating the 50 CTCSS signal frequencies. The center frequency is changed by a clock from a programmable frequency divider. |

| Block | Function |
|---|---|
| Detector | Circuit which judges if CTCSS is present or not from the TSQBPF2 output signal. |
| AGNDG | Circuit for generating a reference voltage for internal analog circuits. |
| BIASG | Circuit which determines the operating current of the operational amplifiers used internally. |

## Pin / Function

| Pin No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | TXIN1 | I | Transmit signal input pin 1. This is the inverted input of AMP1. A mic amp is configured by connecting resistors and capacitors externally. |
| 2 | TXIN2 | I | Transmit signal input pin 2. This is the inverted input of AMP1. The input signal of TXIN1 and TXIN2 are added and output to the TXINO pin. This input is muted with setting “TXON” data of control register. |
| 3 | TXINO | O | AMP1 output pin. This pin can drive a 30kohm ( AC resistance) or greater load. |
| 4 | MOD | O | Transmit modulation signal input pin. This pin can drive a 10kohm (AC resistance) or greater load. |
| 5 | MODIN | I | Transmit modulation signal input pin. This is the inverting input for AMP3. Connecting external resistors and capacitors configures a smoothing filter. |
| 6 | SPOUT | O | Splatter filter output pin.<br>It can drive a 10kohm (AC resistance) or higher load.<br>“SW1” data can bypass the Limiter to Splatter. |
| 7 | RXOUT | O | Receiving voice signal output pin. It can drive a 10kohm (AC resistance) or higher load. When in the standby state, the impedance at this pin becomes high. |
| 8 | VDD | - | Positive power supply pin.<br>A 1.8V…5.5V voltage is applied. |
| 9 | XIN | I/O | Crystal oscillator connection pins. By connecting a 3.6864MHz or 4.194304MHz oscillator between these 2 pins, a reference clock used internally by the IC is created. The frequency of crystal oscillator is set by CKSL data of control register. When a clock is supplied externally, please refer to external application circuits. (Refer to Page 25 Fig.2 or 3) |
| 10 | XOUT | I | Crystal oscillator connection pins. |
| 11 | STB | I | Serial data strobe signal input pin. |
| 12 | SDATA/DCS | I | Serial data input pin. 8 bit serial data are input for setting operating modes or CTCSS/CDCSS frequencies, etc. After setting “DCS” with serial data, CDCSS code is available and output from TXTONE pin through TSQLPF1 filter. (Refer to Page 8) |
| 13 | SCLK | I | Clock input pin for serial data. |

| Pin No. | Pin Name | I/O | Function |
|---|---|---|---|
| 14 | DETOUT | O | CTCSS detects signal output pin. (Open drain output)<br>When in the receive mode, if a CTCSS at the frequency set by serial data is detected; this signal goes “Low”.<br>In the transmit mode, it is high impedance at all times. |
| 15 | VSS | - | Negative power supply pin.<br>A voltage of 0V is applied. |
| 16 | TXTONE | O | Transmit CTCSS/CDCSS monitor pin.<br>When in the transmit mode, CTCSS of the frequency set by serial data is output from this pin. CDCSS codes from CPU input into SDATA/DCS pin, which is limited by TSQLPF1, is also output from this pin.<br>When in the receive mode, the AGND level is output.<br>When in the standby state, the impedance at this terminal becomes high.<br>It can drive a 10kohm (AC resistance) or higher load. |
| 17 | DREF | I | CTCSS detect level adjust pin. The CTCSS decoder's threshold level is determined by applying a DC voltage greater than the AGND level to this pin.<br>It is computed by Vth=0.575VDD formula.<br>( Refer to Page 21 and 24) |
| 18 | LIMBS | I | Limiter level fine adjustment pin.<br>By applying a DC voltage to this pin, fine adjustment of the lower limit limiter level can be done and the limiter's symmetry can be adjusted. |
| 19 | LIMLV | I | Limiter level adjustment pin.<br>The limit level can be adjusted by applying the DC voltage to this pin. If no connections are made, the pre-determined limiter level is set. |
| 20 | AGND | O | Analog ground pin. A 1/2VDD voltage, which becomes the reference for the analog circuit, is output.<br>Connect a capacitor to stabilize the analog ground. |
| 21 | AGNDIN | I | Analog ground input pin. Connect a capacitor to stabilize the analog ground. |
| 22 | RXINO | O | AMP2 output pin. This pin can drive a 30kΩ (AC resistance) or greater load. |
| 23 | RXIN | I | Receive demodulation signal input pin. This is the inverted input of AMP2. A pre filter is configured by connecting resistors and capacitors externally. |
| 24 | RXTONE | O | Receiving CTCSS/CDCSS monitor pin.<br>In the Receive mode, the designated CTCSS/CDCSS is selected from the receiving signal. This pin can drive a 10kΩ (AC resistance) or greater load. |

## Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Power Supply Voltage : (VDD) | VDD | -0.3 | 6.5 | V |
| Ground Level | VSS | 0 | 0 | V |
| Input Current(except power supply pin) | $I_{IN}$ | -10 | +10 | mA |
| Analog Input Voltage | $V_{AIN}$ | -0.3 | VDD+0.3 | V |
| Digital Input Voltage | $V_{DIN}$<br>$V_{DINO}$<br>Note 1) | -0.3<br>-0.3 | VDD+0.3<br>6.5 | V |
| Storage Temperature | Tstg | -55 | 130 | C |

Note: All voltage values are with respect to the VSS pin.
Note 1) Applicable to DETOUT.

Caution: If used under conditions that exceed these values, the device may be destroyed.
And normal operation cannot be guaranteed under this extreme.

## Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Operating temperature | Ta | -30 | | 70 | C |
| Power supply voltage : (VDD) | VDD | 1.8 | 3.0 | 5.5 | V |
| Analog reference voltage | AGND | | 1/2VDD | | V |
| Current consumption | | | | | |
| RXOFF=1,STBY=1 (Mode 0) | Idd0 | | 0.01 | 0.1 | |
| RXOFF=0,STBY=1 (Mode 1) | Idd1 | | 3.2 | 5.0 | mA |
| RX/TX=1,STBY=0 (Mode 3) | Idd2 | | 4.3 | 8.5 | |

Note: All voltages are with respect to the VSS pin.

# Digital Characteristics

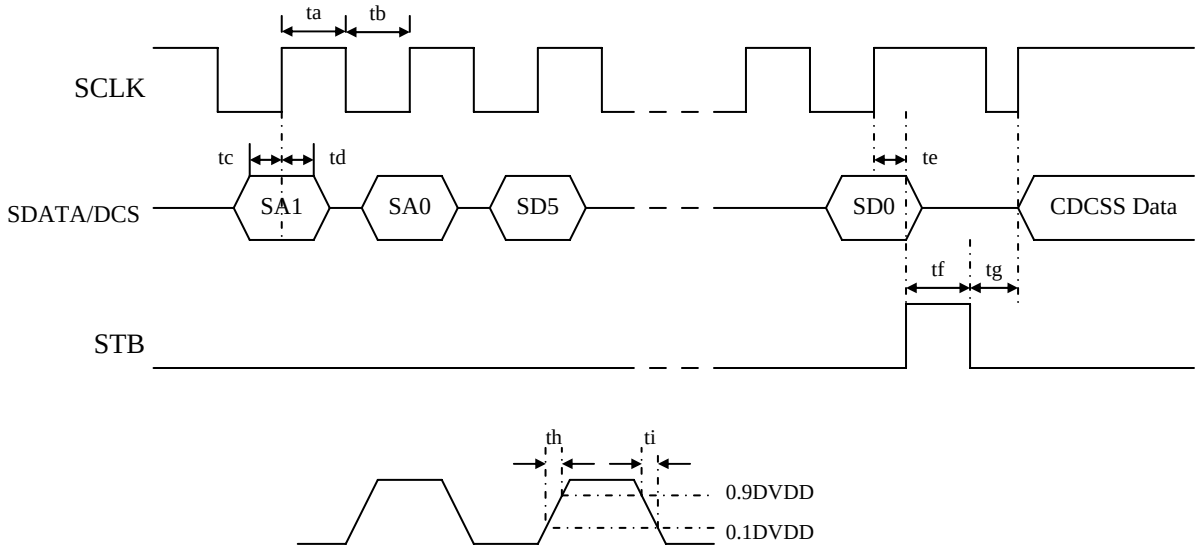
## 1) DC Characteristics

| Parameter | Pin | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| High level input voltage | (1) | $V_{IH}$ | 70%VD+ | | | V |
| Low level input voltage | (1) | $V_{IL}$ | | | 30%VD+ | V |
| High level input current $V_{IH}$=VD+ | (1) | $I_{IH}$ | | | 10 | uA |
| Low level input current $V_{IL}$=0V | (1) | $I_{IL}$ | -10 | | | uA |
| Low level output voltage $I_{OL}$=0.8mA | (2) | $V_{OL}$ | | | 0.3 | V |

(1) SDATA/DCS, SCLK, STB
(2) DETOUT

## 2) AC Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Master Clock Frequency CKSL="1"<br>CKSL="0" | fclk | | 3.6864<br>4.194304 | | MHz |
| Serial data input timing | | | | | |
| Clock pulse width 1 | ta | 500 | | | ns |
| Clock pulse width 2 | tb | 500 | | | ns |
| SDATA set up time | tc | 100 | | | ns |
| SDATA hold time | td | 100 | | | ns |
| STROBE Set up time | te | 100 | | | ns |
| STROBE pulse width | tf | 100 | | | ns |
| STROBE dehold time | tg | 100 | | | ns |
| digital input rising time | th | | | 250 | ns |
| digital input falling time | ti | | | 250 | ns |




Serial Data Input

Note) CDCSS code is acceptable after STB has fallen. Specified period of time is Tg.
While CDCSS is transmitting, please set SCLK pin is fixed to high level and STB pin to low.

# Analog Characteristics

0dBm=0.775Vrms
0dBx=-5dBm at VDD=2V Note 6)

1) TX System

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Standard Input Level @TXINO | | -10 | | dBx |
| Absolute Gain TXINO…MOD 1kHz Note 1) | -1.5 | 0 | 1.5 | dB |
| Maximum Output Level @MOD | | | 0 | dBx |
| Limiter Level @MOD 1kHz Note 1)<br>No external R<br>Adjustment range when external R connected | -9 | -8 | -7<br>-7 | dBx |
| Noise Level TXIN…MOD Note 1,2) | | | -62 | dBm |
| TX CTCSS Output Level @TXTONE | -12 | -10 | -8 | dBx |
| TX CTCSS Frequency Deviation @TXTONE | -0.3 | | +0.3 | % |
| TX CTCSS Distortion @TXTONE | | -35 | -26 | dB |
| CDCSS Signal Gain @TXTONE<br>SDATA/DCS : 134Hz rectangle, Duty ratio 50%<br>TSQLPF1 cut-off freq. : 136.5Hz | -12 | -10 | -8 | dBx |

2) RX System

| Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Standard Input Level @RXINO | | | -10 | | dBx |
| Absolute Gain RXINO…RXOUT 1kHz Note 1) | | -1.5 | 0 | 1.5 | dB |
| Maximum Output Level @RXOUT | | | | 0 | dBx |
| Noise Level RXIN…RXOUT Note 1,2) | | | | -62 | dBm |
| RX CTCSS Detection Level in normal and high speed mode RXINO…DETOUT Note 3) | | -38 | | | dBx |
| RX CTCSS Non-detection Level in normal and high speed mode RXINO…DETOUT Note 4) | | | | -18 | dBx |
| RX CTCSS Response Time in normal mode RXINO…DETOUT Note 5) | @100Hz | | 160 | 250 | ms |
| | @67Hz | | 240 | 370 | ms |
| RX CTCSS Response Time in high speed mode RXINO…DETOUT Note 5) | @100Hz | | 95 | 150 | ms |
| | @67Hz | | 150 | 210 | ms |
| CDCSS Signal Gain RXINO…RXTONE(DCS=1) | | -2 | 0 | 2 | dB |
| Maximum CDCSS Signal Level @RXTONE(DCS=1) | | | | -10 | dBx |

3) Operational Amplifiers

| Parameter | | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Gain Error | AMP1,2,3 | f = 60Hz…3.4kHz<br>Gain = 0…30dB | -1 | 0 | 1 | dB |

4) Filter Characteristics

| Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| TX Overall Characteristic Note 7) | 250Hz | | -43 | -38 | |
| TXINO…SPOUT | 300Hz | -3 | | 0.5 | |
| | 350Hz | -1 | | 1 | dB |
| Relative Gain | 2.0kHz | -1 | | 1 | |
| 0dB @ 1kHz | 3.0kHz | -3 | | 0 | |
| (Refer to Fig.1) | 3.6kHz | | -50 | -40 | |
| RX Overall Characteristic | 250Hz | | -43 | -38 | |
| RXINO…RXOUT | 300Hz | -3 | | 0.5 | |
| | 350Hz | -1 | | 1 | dB |
| Relative Gain | 2.5kHz | -1 | | 1 | |
| 0dB @ 1kHz | 3.0kHz | -1 | | 1 | |
| (Refer to Fig.2) | 3.6kHz | | -45 | -40 | |

Note 1) Refer to the external circuit example. Refer to Page 23.

Note 2) After 3rd order low-pass filter (fc=30kHz)

Note 3) Frequency deviation within ±0.5%. Refer to the external circuit example.
AMP4 Gain: 21dB

Note 4) Frequency deviation ±3.0% or greater. (When the TSQBPF2 Q value is “H”)
AMP4 Gain: 21dB

Note 5) when -20 dBx Refer to the external circuit example. Page 24, Fig.1
AMP4 Gain: 21dB

Note 6) dBx is standardized so that it can correspond to all voltages between 1.8…5.5 V.
When the voltage is 2 V, 0 dBx = -5 dBm. If we let the voltage be X [V], then

$$0\ \text{dBx} = -5 + 20\log(X/2) \quad [\text{dBm}].$$

Note 7) Passing through Limiter, Adder and Splatter by setting “SW1”=0.

□

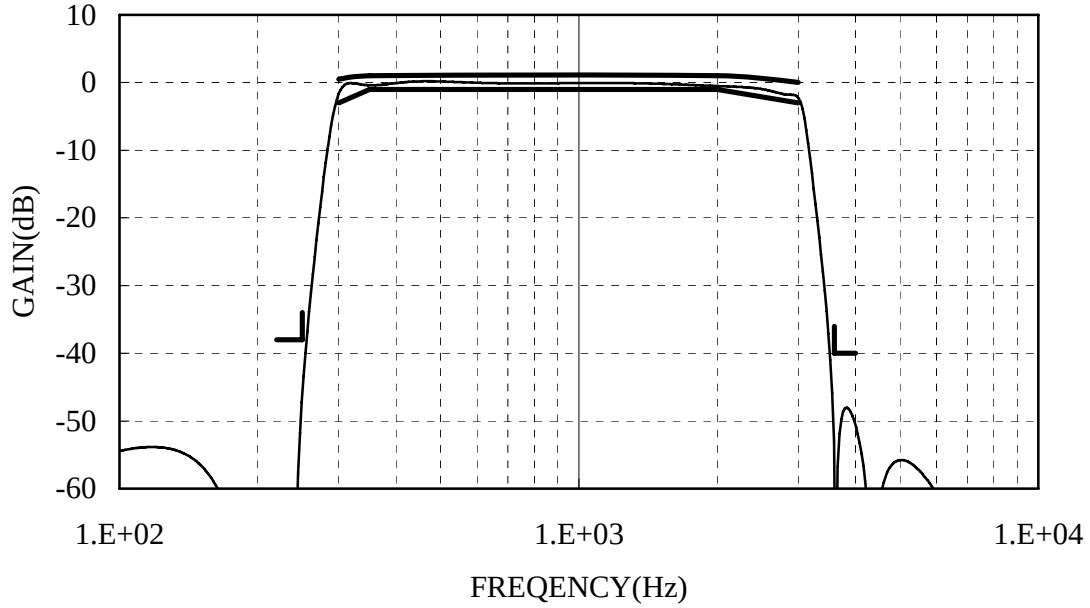



Fig. 1 TX Overall Characteristic

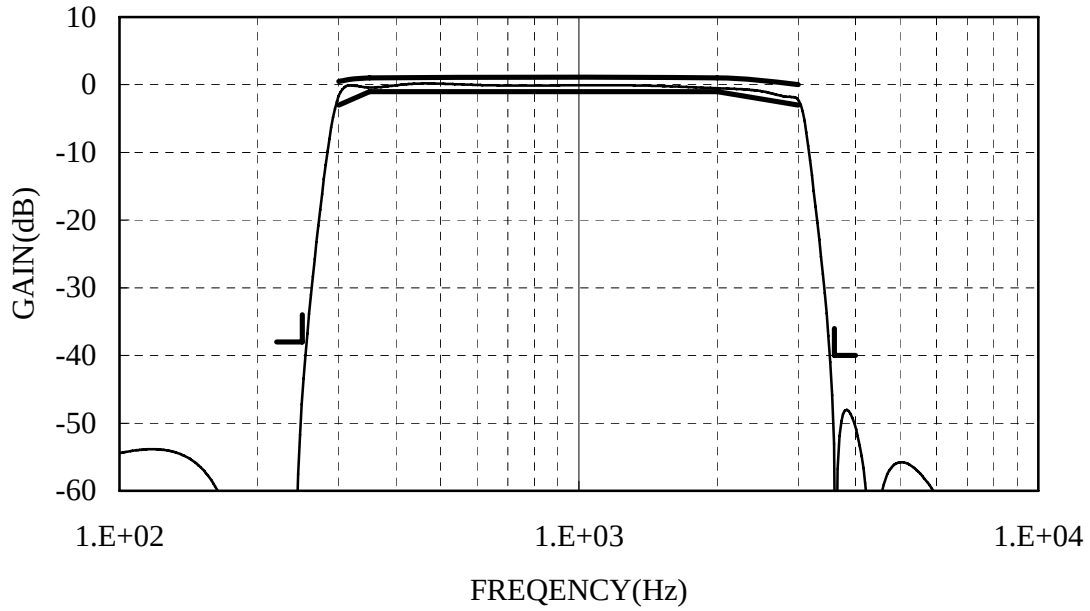
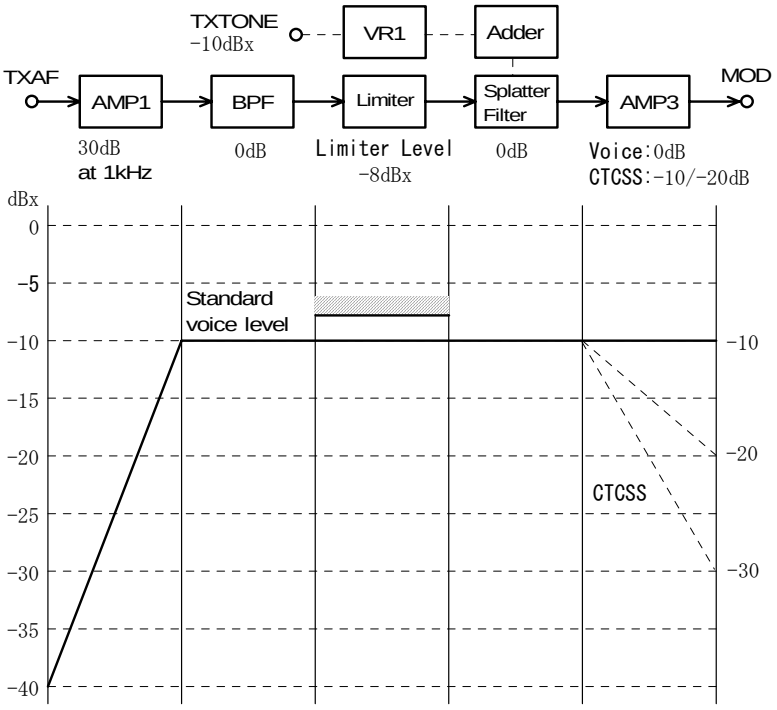


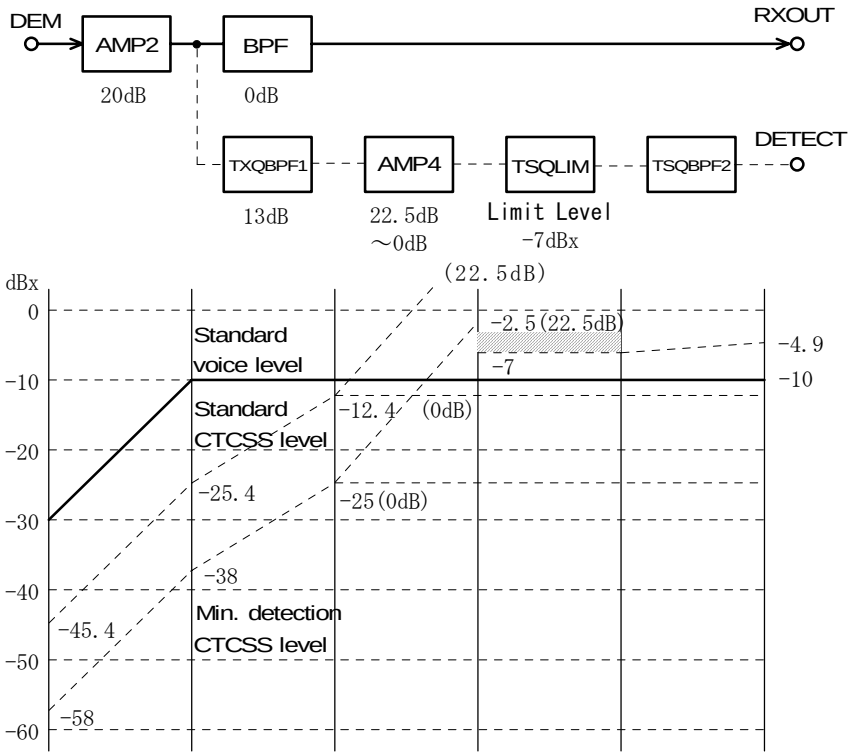

Fig. 2 RX Overall Characteristic

# Level Diagram

1) TX System




2) RX System




Note) when AMP2 is used as De-emphasis, the level diagram of CTCSS is changed.

# Serial Interface Configuration

Writing data to the control register from the serial interface pints (SDATA/DCS, SCLK, and STB) sets the various modes and the CTCSS/CDCSS frequency of the AK2345. Serial data are configured from two address bits and 6 data bits, for a total of 8 bits.

■Register Configuration

| Address | | Function | Data | | | | | |
|---|---|---|---|---|---|---|---|---|
| SA1 | SA0 | | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 |
| 0 | 0 | Mode 1 and Internal switch 1 | TST | RXOFF | RVTN | RXON | RX/TX | STBY |
| 0 | 1 | Mode 2 and Internal switch 2 | 0 | 0 | DCS | SW3 | SW2 | SW1 |
| | | | 0 | 1 | 0/1 | VR15 | VR14 | VR13 |
| | | | 1 | 0 | 0 | VR12 | VR11 | VR10 |
| | | | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | Master clock AMP4 Gain | GA3 | CKSL | TXON | GA2 | GA1 | GA0 |
| 1 | 1 | Frequency | CTCSS/CDCSS frequency register | | | | | |

Note: SA[1:0]_SD[5:0] =01_100001 of SD3 and 01_110000 of SD[3:0] are assigned to test registers. These registers should be set to “0”.

■Register Map

1) Setting of Mode1 and Internal Switch1

| Address | | Data | | | | | |
|---|---|---|---|---|---|---|---|
| SA1 | SA0 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 |
| 0 | 0 | TST | RXOFF | RVTN | RXON | RX/TX | STBY |

| Data name | Function | | | |
|---|---|---|---|---|
| TST | Test mode control “1”: Normal Operation “0”: Test Mode | | | |
| RXOFF | RXOUT pin control | | | |
| RVTN | TX CTCSS phase control “1”: Positive Phase (0 degree) “0”: Negative Phase (180 degree) | | | |
| RXON | RXOUT pin control | RXOFF | RXON | RXOUT pin |
| | | 1 | 1 | Goes ON/OFF according to the presence of the receive CTCSS. |
| | | 1 | 0 | Normally ON |
| | | 0 | 0/1 | Normally OFF (AGND level) |
| RX/TX | Selects the Transmit or Receive mode. “1”: RX Mode “0”: TX Mode | | | |
| STBY | Standby mode control “1”: Standby Mode “0”: Normal Operation | | | |

2-1) Setting of Mode2 and Internal Switch2

| Address | | Sub Address | | Data | | | |
|---|---|---|---|---|---|---|---|
| SA1 | SA0 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 |
| 0 | 1 | 0 | 0 | DCS | SW3 | SW2 | SW1 |
| 0 | 1 | 0 | 1 | Note 4) | VR15 | VR14 | VR13 |
| 0 | 1 | 1 | 0 | 0 | VR12 | VR11 | VR10 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

| Data name | Function | | | | |
|---|---|---|---|---|---|
| DCS | CDCSS/CTCSS mode control | Data name | | Circuit block condition | |
| | | DCS | RX/TX | TSQLPF1 | TSQHPF1 |
| | | "1" (CDCSS mode) | "1" (RX mode) | Through (Gain:0dB) | Bypass |
| | | | "0" (TX mode) | Through (Gain:0dB) | Bypass |
| | | "0" (CTCSS mode) | "1" (RX mode) | Through (Gain:13dB) | Through (Gain:0dB) |
| | | | "0" (TX mode) | Through (Gain:0dB) | Bypass |
| SW3 | RX CTCSS response time mode control | "1": High speed mode detection<br>"0": Normal mode detection | | | Note 1) |
| SW2 | TX CTCSS/DCSS control | "1": ON (adding TX tone to voice internally )<br>"0": OFF( AGND level ) (adding TX tone to voice externally ) | | | Note 2,3) |
| SW1 | TX voice control | "1": Limiter and Splatter are bypassed<br>"0": Limiter and Splatter are through | | | |
| VR15 | Coarse adjustment of TX CTCSS/CDCSS signal level | "1": -10dB<br>"0": -20dB | | | Note 2) |
| VR14…10 | Fine adjustment of TX CTCSS/CDCSS signal level. Refer to the next page | | | | |

Note 1) Even if AK2345 receives the reverse tone (negative phase signal) in high-speed detection mode, the shortening detection is not effective in de-response time. Use of high-speed detection mode is not recommendatory in the reverse tone system.

Note 2) SW2 can configure to add TX CTCSS/CDCSS signal to voice signal internally. TX CTCSS/CDCSS signal level is adjusted by VR15 in coarse range and VR14 to VR10 in fine one listed in following page.

Note 3) CTCSS/CDCSS signal is normally output from TXTONE pin according to setting the data of address "11" in both SW2=0 and SW2=1.

Note 4) Setting of "0" and "1" does not change the circuits operation.

Note 5) Address: "01", sub-address: "10", data: SD3 and address: "01", sub-address: "11", data: SD3, SD2, SD1 and SD0 have a test function. Normally set to "0" to protect a malfunction.

2-2) Fine adjustment of TX CTCSS/CDCSS signal level in internal addition to voice signal

| Data | | | | | Gain |
|---|---|---|---|---|---|
| VR14 | VR13 | VR12 | VR11 | VR10 | (dB) |
| 0 | 0 | 0 | 0 | 0 | -8.5 |
| 0 | 0 | 0 | 0 | 1 | -8.0 |
| 0 | 0 | 0 | 1 | 0 | -7.5 |
| 0 | 0 | 0 | 1 | 1 | -7.0 |
| 0 | 0 | 1 | 0 | 0 | -6.5 |
| 0 | 0 | 1 | 0 | 1 | -6.0 |
| 0 | 0 | 1 | 1 | 0 | -5.5 |
| 0 | 0 | 1 | 1 | 1 | -5.0 |
| 0 | 1 | 0 | 0 | 0 | -4.5 |
| 0 | 1 | 0 | 0 | 1 | -4.0 |
| 0 | 1 | 0 | 1 | 0 | -3.5 |
| 0 | 1 | 0 | 1 | 1 | -3.0 |
| 0 | 1 | 1 | 0 | 0 | -2.5 |
| 0 | 1 | 1 | 0 | 1 | -2.0 |
| 0 | 1 | 1 | 1 | 0 | -1.5 |
| 0 | 1 | 1 | 1 | 1 | -1.0 |
| 1 | 0 | 0 | 0 | 0 | -0.5 |
| 1 | 0 | 0 | 0 | 1 | 0.0 |
| 1 | 0 | 0 | 1 | 0 | 0.5 |
| 1 | 0 | 0 | 1 | 1 | 1.0 |
| 1 | 0 | 1 | 0 | 0 | 1.5 |
| 1 | 0 | 1 | 0 | 1 | 2.0 |
| 1 | 0 | 1 | 1 | 0 | 2.5 |
| 1 | 0 | 1 | 1 | 1 | 3.0 |
| 1 | 1 | 0 | 0 | 0 | 3.5 |
| 1 | 1 | 0 | 0 | 1 | 4.0 |
| 1 | 1 | 0 | 1 | 0 | 4.5 |
| 1 | 1 | 0 | 1 | 1 | 5.0 |
| 1 | 1 | 1 | 0 | 0 | 5.5 |
| 1 | 1 | 1 | 0 | 1 | 6.0 |
| 1 | 1 | 1 | 1 | 0 | 6.5 |
| 1 | 1 | 1 | 1 | 1 | 7.0 |

3) Setting of the master clock frequency and AMP4 Gain

| Address | | Data | | | | | |
|---|---|---|---|---|---|---|---|
| SA1 | SA0 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 |
| 1 | 0 | GA3 | CKSL | TXON | GA2 | GA1 | GA0 |

| Data name | Function | |
|---|---|---|
| CKSL | Master clock frequency | ”1”: 3.6864MHz<br>“0”: 4.194304MHz |
| TXON | TXIN2 pin control | “1”: OFF (Mute)<br>“0”: ON |

| Data name | | | | Function |
|---|---|---|---|---|
| GA3 | GA2 | GA1 | GA0 | AMP4 Gain (dB) |
| 1 | 0 | 0 | 0 | 0.0 |
| 0 | 0 | 0 | 0 | 1.5 |
| 1 | 0 | 0 | 1 | 3.0 |
| 0 | 0 | 0 | 1 | 4.5 |
| 1 | 0 | 1 | 0 | 6.0 |
| 0 | 0 | 1 | 0 | 7.5 |
| 1 | 0 | 1 | 1 | 9.0 |
| 0 | 0 | 1 | 1 | 10.5 |
| 1 | 1 | 0 | 0 | 12.0 |
| 0 | 1 | 0 | 0 | 13.5 |
| 1 | 1 | 0 | 1 | 15.0 |
| 0 | 1 | 0 | 1 | 16.5 |
| 1 | 1 | 1 | 0 | 18.0 |
| 0 | 1 | 1 | 0 | 19.5 |
| 1 | 1 | 1 | 1 | 21.0 |
| 0 | 1 | 1 | 1 | 22.5 |

4) Setting of the CTCSS/CDCSS Frequency S: standard CTCSS frequency

| Address | | Data | | | | | | Frequency | TSQBPF2 |
|---|---|---|---|---|---|---|---|---|---|
| SA1 | SA0 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | (Hz) | Q Value |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 67.0 | L |
| | | 0 | 0 | 0 | 0 | 1 | 0 | 71.9 | L |
| | | 0 | 0 | 0 | 0 | 1 | 1 | 77.0 | L |
| | | 0 | 0 | 0 | 1 | 0 | 0 | 82.5 | L |
| | | 0 | 0 | 0 | 1 | 0 | 1 | 88.5 | L |
| | | 0 | 0 | 0 | 1 | 1 | 0 | S 94.8 | H |
| | | 0 | 0 | 0 | 1 | 1 | 1 | S 100.0 | H |
| | | 0 | 0 | 1 | 0 | 0 | 0 | S 103.5 | H |
| | | 0 | 0 | 1 | 0 | 0 | 1 | S 107.2 | H |
| | | 0 | 0 | 1 | 0 | 1 | 0 | S 110.9 | H |
| | | 0 | 0 | 1 | 0 | 1 | 1 | S 114.8 | H |
| | | 0 | 0 | 1 | 1 | 0 | 0 | S 118.8 | H |
| | | 0 | 0 | 1 | 1 | 0 | 1 | S 123.0 | H |
| | | 0 | 0 | 1 | 1 | 1 | 0 | S 127.3 | H |
| | | 0 | 0 | 1 | 1 | 1 | 1 | S 131.8 | H |
| | | 0 | 1 | 0 | 0 | 0 | 0 | S 136.5 | H |
| | | 0 | 1 | 0 | 0 | 0 | 1 | S 141.3 | H |
| | | 0 | 1 | 0 | 0 | 1 | 0 | S 146.2 | H |
| | | 0 | 1 | 0 | 0 | 1 | 1 | S 151.4 | H |
| | | 0 | 1 | 0 | 1 | 0 | 0 | S 156.7 | H |
| | | 0 | 1 | 0 | 1 | 0 | 1 | S 162.2 | H |
| | | 0 | 1 | 0 | 1 | 1 | 0 | S 167.9 | H |
| | | 0 | 1 | 0 | 1 | 1 | 1 | S 173.8 | H |
| | | 0 | 1 | 1 | 0 | 0 | 0 | S 179.9 | H |
| | | 0 | 1 | 1 | 0 | 0 | 1 | S 186.2 | H |
| | | 0 | 1 | 1 | 0 | 1 | 0 | S 192.8 | H |
| | | 0 | 1 | 1 | 0 | 1 | 1 | S 203.5 | H |
| | | 0 | 1 | 1 | 1 | 0 | 0 | S 210.7 | H |
| | | 0 | 1 | 1 | 1 | 0 | 1 | S 218.1 | H |
| | | 0 | 1 | 1 | 1 | 1 | 0 | S 225.7 | H |
| | | 0 | 1 | 1 | 1 | 1 | 1 | S 233.6 | H |
| | | 1 | 0 | 0 | 0 | 0 | 0 | S 241.8 | H |
| | | 1 | 0 | 0 | 0 | 0 | 1 | S 250.3 | H |
| | | 1 | 0 | 0 | 0 | 1 | 0 | S 67.0 | H |
| | | 1 | 0 | 0 | 0 | 1 | 1 | S 71.9 | H |
| | | 1 | 0 | 0 | 1 | 0 | 0 | S 74.4 | H |
| | | 1 | 0 | 0 | 1 | 0 | 1 | S 77.0 | H |
| | | 1 | 0 | 0 | 1 | 1 | 0 | S 79.7 | H |
| | | 1 | 0 | 0 | 1 | 1 | 1 | S 82.5 | H |
| | | 1 | 0 | 1 | 0 | 0 | 0 | S 85.4 | H |
| | | 1 | 0 | 1 | 0 | 0 | 1 | S 88.5 | H |
| | | 1 | 0 | 1 | 0 | 1 | 0 | S 91.5 | H |
| | | 1 | 0 | 1 | 0 | 1 | 1 | S 97.4 | H |
| | | 1 | 0 | 1 | 1 | 0 | 0 | S 69.4 | H |
| | | 1 | 0 | 1 | 1 | 0 | 1 | 159.8 | H |
| | | 1 | 0 | 1 | 1 | 1 | 0 | 165.5 | H |
| | | 1 | 0 | 1 | 1 | 1 | 1 | 171.3 | H |
| | | 1 | 1 | 0 | 0 | 0 | 0 | 177.3 | H |

| Address | | Data | | | | | | Frequency | TSQBPF2 |
|---|---|---|---|---|---|---|---|---|---|
| SA1 | SA0 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | (Hz) | Q Value |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 183.5 | H |
| | | 1 | 1 | 0 | 0 | 1 | 0 | 189.9 | H |
| | | 1 | 1 | 0 | 0 | 1 | 1 | 196.6 | H |
| | | 1 | 1 | 0 | 1 | 0 | 0 | 199.5 | H |
| | | 1 | 1 | 0 | 1 | 0 | 1 | 206.5 | H |
| | | 1 | 1 | 0 | 1 | 1 | 0 | 229.1 | H |
| | | 1 | 1 | 0 | 1 | 1 | 1 | 254.1 | H |
| | | 1 | 1 | 1 | 0 | 0 | 0 | Note 1) | - |
| | | 1 | 1 | 1 | 0 | 0 | 1 | 74.0 | H |

Note 1) Available for setting TX mode (“RX/TX”=0) and CDCSS mode (“DCS”=1).
TSQLPF1’s cut-off frequency is 3.24kHz at “CKSL”=1 and 3.69kHz at “CKSL”=0.

Note 2) If a code other than the above is set, the level at TXTONE pin changes to AGND level in TX mode and DETOUT pin goes “Low” in RX mode.

Note 3) because the 74.4zHz and 74.0Hz are very closely, it is difficult for AK2345 to distinguish them each other. Please pay attention to set these tone frequencies in the same system.

# Operating Explanation

1) Mode of operation (Address: “00”)

The AK2345 operation mode is determined by 4 bits logic of TST, RXOFF, RX/TX and STBY from 6 bits serial data selected according to address “00” (See Table 1)
In addition, regarding the transmit mode and receive mode, voice signal output and CTCSS/CDCSS output can be controlled by the 4 bits RXOFF, RVTN, RXON and RX/TX. (See Table 2,3,4)

| TST | RXOFF | RVTN | RXON | RX/TX | STBY | Operation Mode | Description |
|---|---|---|---|---|---|---|---|
| 0 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | Test Mode | This mode is used to test when the IC is shipped. |
| 1 | 1 | 0/1 | 0/1 | 0/1 | 1 | Standby Mode (Mode 0) | In this mode, the oscillator circuit stops, analog outputs set the high impedance and reducing the power consumption. |
| 1 | 0 | 0/1 | 0/1 | 0/1 | 1 | Voice Operation Mode (Mode 1) | Only voice signal section is in operation. CTCSS circuit operation is stopped and power consumption drops. |
| 1 | 0/1 | 0/1 | 0/1 | 0 | 0 | Transmit Mode (Mode 2) | Voice signals from TXIN1, 2 pass through BPF, Limiter and Splatter are output to MOD. CTCSS is output from TXTONE according to “CTCSS Frequency Setting” table. DETOUT pin goes to “Low”. CDCSS is from SDATA/DCS pin to TXTONE pin also. |
| 1 | 0/1 | 0/1 | 0/1 | 1 | 0 | Receive Mode (Mode 3) | When detecting the CTCSS frequency as same as the setting frequency according to “CTCSS Frequency setting table”, DETOUT pin goes to “Low”. The CTCSS signal is eliminated by BPF, then only the voice signal is output from RXOUT. |

Table.1

Signal Control in Voice Operation Mode

| Data name | Function | | | |
|---|---|---|---|---|
| RX/TX SW1 | RX/TX Switching | SW1 | RX/TX | RXOUT pin |
| | | 0 | 0 | AMP1 output is connected to BPF.<br>AMP2 output is connected to RXOUT. |
| | | 0 | 1 | AMP1 output is connected to SPOUT through Limiter and Splatter.<br>AMP2 output is connected to BPF. |
| | | 1 | 0/1 | AMP1 output is connected to SPOUT.<br>AMP2 output is connected to RXOUT. |
| RXON | RXOUT pin control | "1": OFF(AGND level)<br>"0": ON | | |

Table.2

Signal Control in Transmit Mode

| Data name | Function | | | |
|---|---|---|---|---|
| RXOFF RXON | RXOUT pin control | RXOFF | RXON | RXOUT pin |
| | | 1 | 1 | OFF (AGND level) |
| | | 1 | 0 | ON |
| | | 0 | 0/1 | OFF (AGND level) |
| RVTN | TXTONE phase control | "1": Positive Phase (0 degree)<br>"0": Negative Phase (180 degree) | | |

Table.3

Signal Control in Receive Mode

| Data name | Function | | | |
|---|---|---|---|---|
| RXOFF RXON | RXOUT pin control | RXOFF | RXON | RXOUT pin |
| | | 1 | 1 | Goes ON/OFF according to the presence of the receive tone. |
| | | 1 | 0 | Normally ON |
| | | 0 | 0/1 | Normally OFF (AGND level) |

Table.4

2) CTCSS Mode(Address: 01, "DCS"=0)

2.1) Transmitter Mode (Address: 00, "RX/TX"=0)

AK2345 has not only CTCSS of 39 frequencies compatible with the TIA/EIA-603 standard but also 11 new frequencies that are higher than 156.7Hz, total 50 frequencies of CTCSS are available in TX mode.

These signals are generated by "Programmable Divider" according to the frequency setting table of address: 11, output to TXTONE (16) pin through TSQLPF1 which eliminate the high harmonics.

SW2 can select to add TX CTCSS to voice signal internally or externally, CTCSS level is adjusted by VR15 and VR14 to VR10.

To stop TX CTCSS select a code other than the values shown in the CTCSS frequency setting table. (Example: set "0" in each bit of SD0 to SD5)

### 2.2) Receiver Mode (Address: 00, “RX/TX”=1)

Voice and CTCSS/CDCSS signals from RXIN (23) pin are band-limited and amplified 13dB by TSQLPF1, rejected DC offset by TSQHPF1 and output to RXTONE (24) pin according to the frequency setting table of address: 11.

Received CTCSS is waveformed by gain-amplifier: AMP4, limiter: TSQLIM, high Q-value filter: TSQBPF and judged to be detecting or non-detecting at Detector in the last sequence. When the circuits detect it, DETOUT (14) pin goes to “Low” level.

CTCSS Detector works properly with supplying DC voltage higher than AGND level to DREF (17) pin. The level is computed by the following formula. (Refer to Page 24 Fig.1)
Vth = AGND+3.9k/(22k+3.9k)*AGND = 1/2VDD+0.1506*1/2VDD = 0.575*VDD
For example: Vth=1.73V @VDD=3.0V

DETOUT pin goes to “High” in non-detecting operation at this mode (Mode 2), Standby mode (Mode 0), Voice operation mode (Mode 1) and TX mode (Mode 2). However, it goes to “Low” if a code is set other than the frequency in the setting table. (Refer to Page 18 Note2)

The high Q-value CTCSS filter: TSQBPF2 has ±3.0% frequency deviation that discriminates clearly 39 CTCSS standard frequency. Also additional 11 CTCSS can be discriminates due to ±3.0% frequency deviation each other. However, standard 39 frequencies are from 67.0Hz to 250.3Hz and additional 11 frequencies are from 159.8Hz to 254.1Hz. So CTCSS from 156.7Hz to 254.1Hz frequencies show ±1.5% deviation, there is a possibility that mis-detection will happen in neighboring CTCSS.
Please select the CTCSS frequency to keep ±3.0% frequency deviation, especially from 156.7Hz to 254.1Hz ranges.

### 2.3) Receiver (Decode) mode, Response time

AK2345 response time can be speeded up by the selection of TSQBPF2 Q-value and the use of TSQRECT circuit block.
The TSQBPF2 Q-value for 5 frequencies, 67.0, 71.9, 77.0, 82.5 and 88.5Hz.have both “L” and “H” Q-value. If “L” is selected, response time can be shortened, but distinguishing between neighboring frequencies (when 88.5Hz, between that and 84.5Hz and 91.5Hz) becomes more difficult. The Q-value becomes “H” for the other frequencies.

TSQRECT has high-speed detection mode for 50 CTCSS by full wave rectifier type frequency multiply circuit, which shorted response time to 70 % by setting data “SW3”=1 compared with normal mode.

### 2.4) Receiver Mode, from detection to non-detection

Response time is the interval between receiving the desired tone at RXIN pin and changing DETOUT pin level to “Low” due to detection.
If CTCSS is stopped or changes to other tone, DETOUT pin goes to “High” again because of non-detection, which is called de-response time.

De-response time which is from detection status to non-detection can be minimized by setting the following program sequence.

a. Set tone frequency to “11/111000”
b. Set to receiver mode by “RX/TX”=1
c. Set 10mS waiting time.
d. Set the desired tone frequency again.

3) CDCSS Mode(Address: 01, “DCS”=1)

3.1) Transmitter mode (Address: 00, “RX/TX”=0)

CDCSS code from CPU connected to SDATA/DCS (12) pin automatically passes through TSQLPF1 filter, and signal is output to TXTONE (16) pin. This CDCSS signal pass is programmed by “DCS” data listed in Page 14.

Please refer to Page 8 about timing chart and also TSQLPF1’s cutoff frequency is set by frequency setting table Page 17 and 18.

The TX level of CDCSS is -10±2dBx at 134Hz (CDCSS data rate: 134.4bps) equal to the standard voice one.

(Refer to Analog characteristics Page 9)

3.2) Receiver mode (Address: 00, “RX/TX”=1)

Voice and CDCSS code from RXIN pin automatically pass through TSQLPF1 filter and CDCSS signal is output to RXTONE (24) pin. TSQLPF1’s cutoff frequency is set by frequency setting table Page 17 and 18.

CDCSS RX gain is 0dB from RXINO pin to RXTONE pin specified in Page 9, and maximum signal level is –10dBx.

If RXTONE pin is connected to CPU input pin, please put some waveform-processing device between them such as comparator.

4) Voice Filter (BPF) Power Down

The test mode can be used and the voice filter can be powered down. In the power down mode, the impedance of the SPOUT and RXOUT pins become Hi-Impedance in all operation modes.

| Address | | Data | | | | | | Voice filter |
|---|---|---|---|---|---|---|---|---|
| SA1 | SA0 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Power down |
| | | 0 | 0 | 0 | 0 | 0 | 0 | Power down release |

5) Initializing at the power on.

The AK2345 does not have a rest pin, so the status of the internal registers is not fixed when the power is switched on.

Following registers should be initialized sequentially after the power is on.

SA[1:0]_SD[5:0]

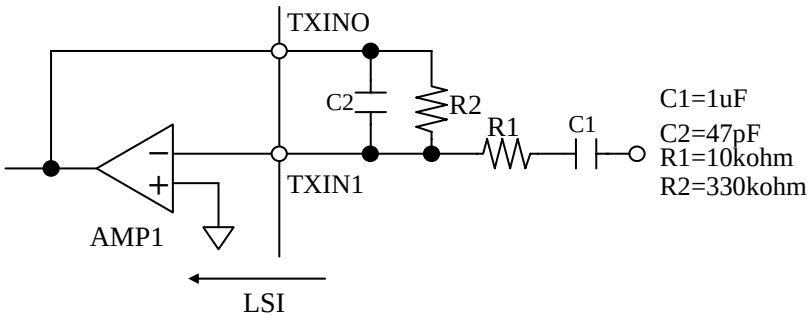
(1) 00_111111 (standby mode)
(2) 00_000000 (voice filter power down release)
(3) 01_100001 (SD3=0 for test register release)
(4) 01_110000 (SD[3:0]=0 for test register release)

Rest of the registers will be set sequentially after these four registers setting.

# Examples of External Circuit

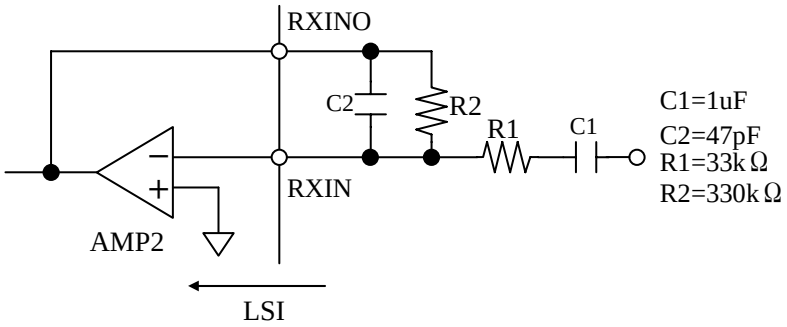
(1) AMP1

This is an op-amp which can be used to configure a filter to adjust the gain of the transmit signal and prevent aliasing so as to cut noise at or above 80kHz. Set the gain at 30dB or lower. The following diagram shows an example of a gain 30dB and cut-off frequency 10kHz. An example of a pre-emphasis filter with a gain of 0dB at 1kHz is C1=1000pF, C2=15pF,R1=15kohm,R2=160kohm.



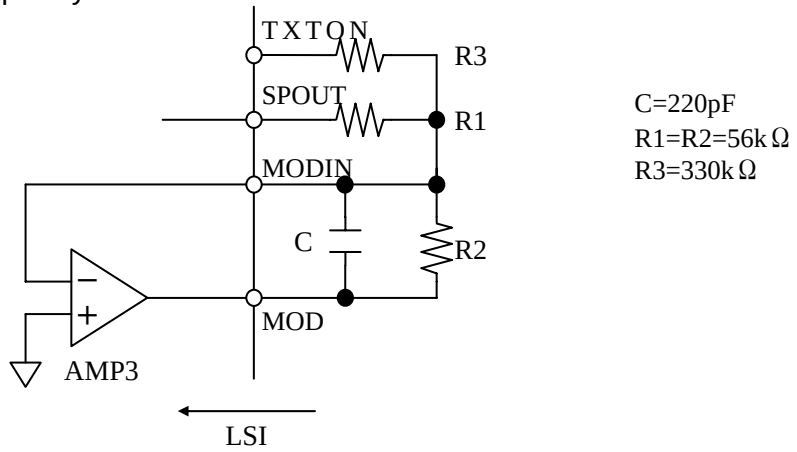

(2) AMP2

This is an op-amp which can be used to configure a filter to adjust the gain of the receive signal and prevent aliasing so as to cut noise at or above 80kHz. Set the gain at 20dB or lower. The following diagram shows an example of a gain 20dB and cut-off frequency 10kHz. An example of a de-emphasis with a gain of 0dB at 1kHz is C1=0.47uF, C2=0.01uF,R1=16kohm,R2=56kohm.




(3) AMP3

This amplifier is used to adjust the transmitting signal gain and configure a smoothing filter. The smoothing filter is used to cut the 80 kHz clock component included in signals at SPOUT. This amp can also be used to add the voice signal and tone signal. The following diagram shows an example of a first-order low pass filter configuration with a gain of 0 dB and a cut-off frequency of 13 kHz.



(4) Threshold level of RX tone detector

The receiving tone detector works under inputting a DC level to the DREF pin, which is higher than the AGND level. The threshold level is computed by the following formula. (Refer to Fig.1)

Vth = AGND+3.9k/(22k+3.9k)*AGND = 1/2VDD+0.1506*1/2VDD = 0.575*VDD

For example: Vth=1.73V @VDD=3.0V

If the threshold level is changed, the response time also changes. For example, the threshold level is made higher; the response time becomes longer. If it is made lower, the response time becomes shorter.

If the hysteresis is desired between detection and non-detection, please feed back the signal to DETOUT. Fig.2 shows an example of receiving tone detection circuit with an approximately 3dB hysteresis.

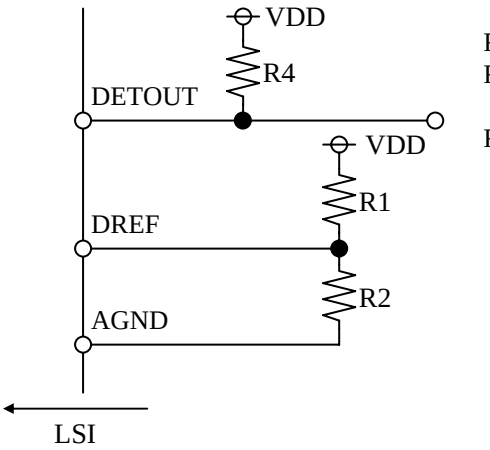



Fig.1 Without hysteresis

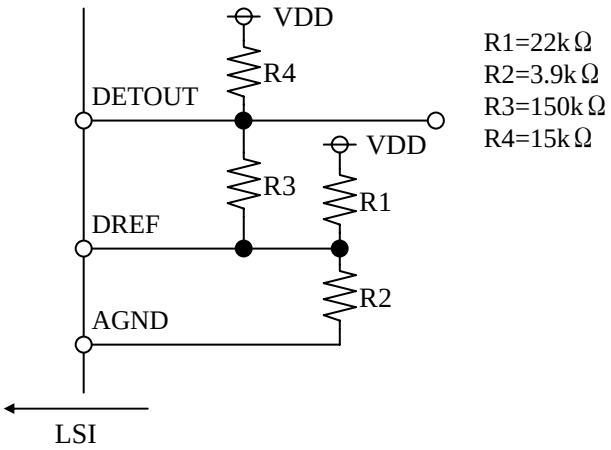
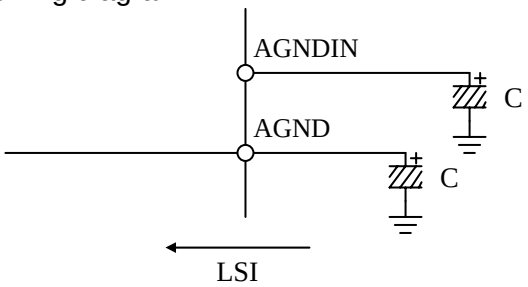



Fig.2 With hysteresis

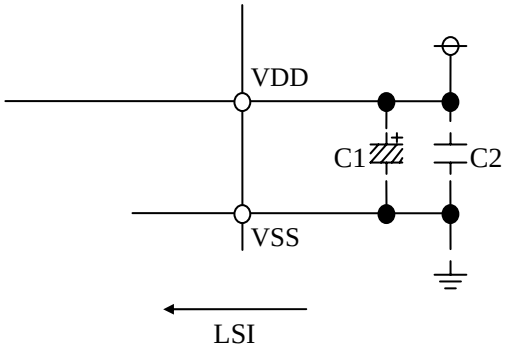
(5) AGND stabilization capacitor

Connect a 0.3uF or larger capacitor between AGND and VSS to stabilize the AGND level. Also in order to eliminate the effect of the ripple in the power supply; please connect a capacitor of the appropriate value between AGNDIN and VSS. A connection example is shown in the following diagram.




(6) Power supply stabilization capacitor

Connecting a capacitor between VDD and VSS reduces the influence of power supply noise. Position of the capacitor is as close as possible to the power supply pin.



(7) Oscillation circuit

Quartz crystal, resistor(1Mohm) and capacitors(22pF) should be connected as shown Fig.1 for on-chip oscillator operation. AK2345 is designed to get a stable oscillation for the electrical equivalent circuit of quartz crystal unit : resonance resistance≦150Ω, shunt capacitance≦5pF. Recommended external capacitance is 22pF due not to exceed the load capacitance≦16pF. (5pF+22pF//22pF)

The first gate of XIN pin uses non-voltage-tracking type inverter. The threshold level is 0.8V. For external clock operation, if the high (H) level of the input clock signal amplitude equals to or is greater than 1.5V, and the low (L) level equals to or is smaller than 0.5V, then connection should be made as shown in Fig.2.

If the input clock signal amplitude (peak-to-peak) equals to or is smaller than 1V, and equals to or is greater than 200mV, then AC coupling should be as illustrated in Fig.3. Please be careful not to let the clock's amplitude exceed the absolute maximum ratings.

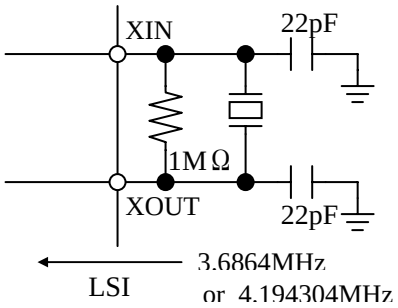



Fig.1

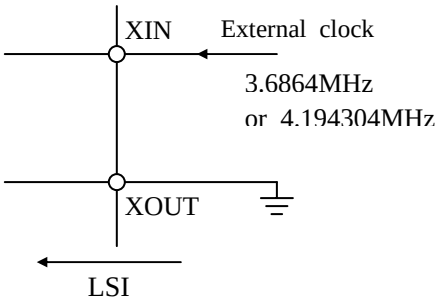



Fig.2

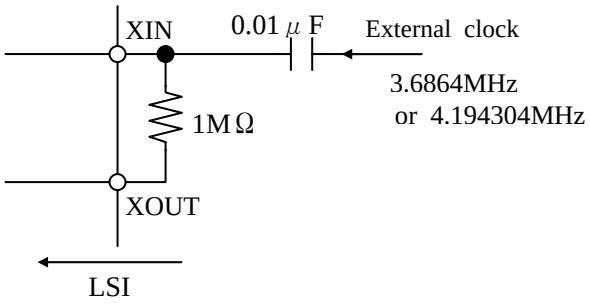
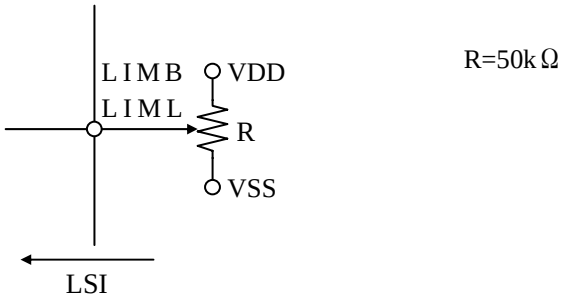



Fig.3

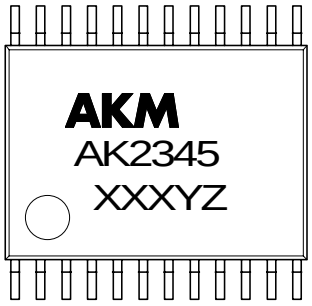
(8) Limiter level setting resistor

If the limiter level is to be adjusted externally, apply DC voltage to the LIMLV pin as shown in the following diagram. The DC voltage applied should be greater than the AGND voltage and if we let the voltage between LIMLV and AGND be a V, the limit level becomes AGND ± a V. If LIMLV is left open, the limit level becomes the pre-determined limit level. The lower limiter level can be fine adjust and the limiter's non-symmetry corrected by applying DC voltage to the LIMBS pin.



# Package

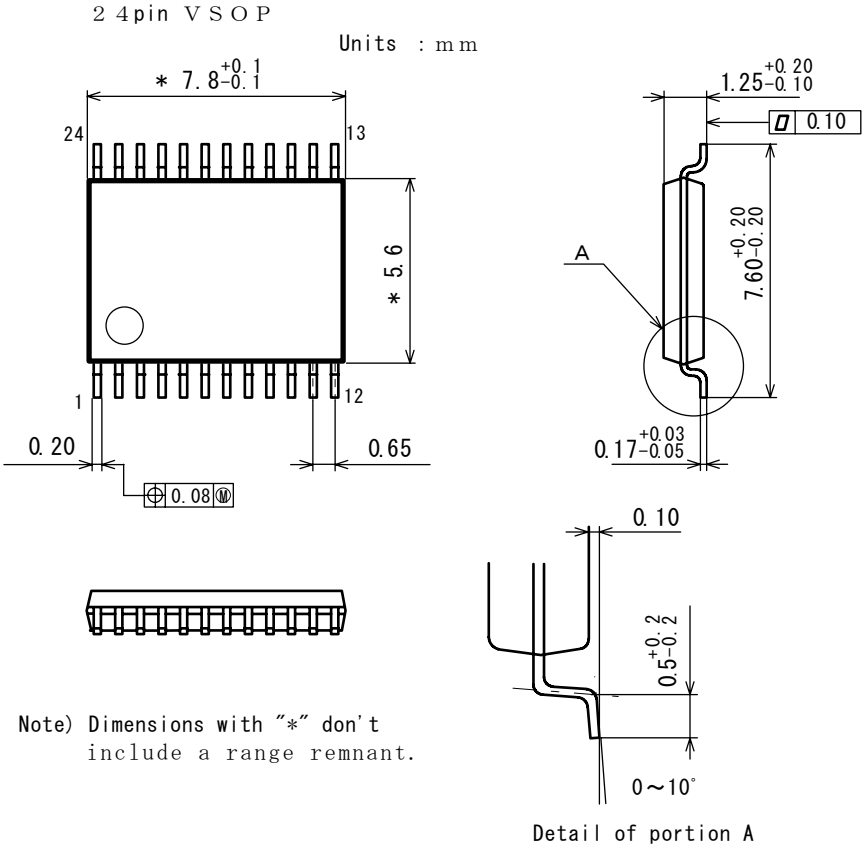
■Marking




［XXXYZ Content］

XXX：Manufacturing Data
Last digit of AD year, 2 digits of week number
Y：Production lot number
Z：Assembly Plant Code

■Package External Dimensions




[Material] Resin: Low stress type Epoxy resin
Lead frame: Cu

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