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AIC1221

Ultra LDO 2A Linear Regulator With Adjustable & Bypass Pin

A low noise, high PSRR and ultra low dropout

linear regulator AIC1221 is optimized for low ESR

ceramic capacitors operation with 2A continuous

current. The AIC1221 is designed for portable and wireless devices with demanding performance

The AIC1221 offers high precision output voltage

of ±2% tolerance. Output voltage can also be

A noise bypass pin is available for further

reduction of output noise. The bypass pin could

be floating if it's unnecessary. At 2A load current

and 5V output voltage, a 480mV dropout is

performed. The quality of low quiescent current

and low dropout voltage makes this device ideal

for battery power applications. The high ripple

rejection and low noise of the AIC1221 provide enhanced performances for critical applications

In addition, a logic-level shutdown input is

included, which reduce supply current to 0.01µA

(typ.) in shutdown mode with fast turn-on time

less than 100µs. The AIC1221's current limit and

thermal protection provide protection against any

overload condition that would create excessive

adjusted for those other than the preset values.

DESCRIPTION

and space requirements.

junction temperatures.

FEATURES

- Guaranteed 2A Output Current.
- Fast Response in Line/Load Transient.
- Wide Operating Voltage Ranges: 1.8V to 6V.
- 0.01µA Shutdown Standby Current.
- Low Quiescent Current: 30µA.
- Fixed: 1.8V, 2.5V, 3.3V, 5V Output Voltage.
- Adjustable Output Voltage are available from 0.8~5.5V.
- Low Dropout : 550mV at 2A and 3.3V output voltage, 480mV at 2A and 5V output voltage.
- High PSRR : 70dB at 1kHz.
- Active Low or High Shutdown Control. Current Limit and Thermal Protection.
- Available in $\pm 2\%$ Output Tolerance.
- Available in SOT-223 & TO-252 (3 & 5 pin) and SOP-8 Package.

APPLICATIONS

- LCD TV, LCD Monitor, DPF
- Networking
- STB
- DVD, HDD Driver
- Portable AV Equipment
- PC Peripherals

TYPICAL APPLICATION CIRCUIT



Fixed Linear Regulator

Adjustable Linear Regulator

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TYPICAL APPLICATION CIRCUIT (Continued)



Adjustable Linear Regulator in SOP-8 Package

ORDERING INFORMATION

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Package & Tape & Reel Packing Type

→ 1.8V Version, in TO-252 Green Package & Tape & Reel Packing Type

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ORDERING INFORMATION (Continued)



Packing Type



ORDERING INFORMATION (Continued)



Example: AIC 1221 H-18GR8TR

→ Chip Enable High, 1.8V Version, in SOP-8 Exposed Pad (Heat Sink) Green Package & Tape & Reel Packing Type



ABSOLUTE MAXIMUM RATINGS

Input Voltage		7V
EN Pin Voltage		7V
Noise Bypass Terminal Voltage		7V
Operating Temperature Range		40°C~85°C
Maximum Junction Temperature		150°C
Storage Temperature Range		65°C~150°C
Lead Temperature (Soldering, 10 sec)		
Thermal Resistance (Junction to Case)	SOT-223	
	TO-252	
	SOP-8 (Exposed Pad)	15°C /W
Thermal Resistance (Junction to Ambient)	SOT-223	
(Assume no ambient airflow, no heat sink)	TO-252	
	SOP-8 (Exposed Pad)	

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.



ELECTRICAL CHARACTERISTICS

($C_{IN} = C_{out} = 4.7 \mu F$ (Note 1), $C_{BP} = 22nF$, $V_{IN} = V_{OUT} + 1V$, $T_J = 25^{\circ}C$, unless otherwise specified) (Note 2)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Voltage (Note 3)		V _{IN}	1.8		6	V
Output Voltage Tolerance	I _{OUT} =1mA	V _{OUT}	-2		2	%
Continuous Output Current	$V_{IN} \ge 2.3V$	I _{OUT}	2			А
Quiescent Current	$\begin{array}{l} \mbox{Chip Enable Low, } V_{EN} \leqq 0.4V, \\ I_{OUT} = 0 \mbox{ mA} \\ \mbox{Chip Enable High, } V_{EN} \geqq 1.6V, \\ I_{OUT} = 0 \mbox{ mA} \end{array}$	ΙQ		30	50	μA
GND Pin Current	$\begin{array}{l} \mbox{Chip Enable Low, } V_{EN} \leqq 0.4V, \\ I_{OUT} = 2A \\ \mbox{Chip Enable High, } V_{EN} \geqq 1.6V, \\ I_{OUT} = 2A \end{array}$	I _{GND}		30	50	μA
Standby Current	Chip Enable Low, $V_{EN} = V_{IN}$ Chip Enable High, $V_{EN} = 0$	I _{STBY}		0.01	0.5	μA
Output Current Limit	R _{LOAD} = 0.1 Ω	IIL	2.2	3.0	3.9	А
Current Fold Back	R _{LOAD} = 0.1 Ω	I _{CFB}		1.0		А
	I _{OUT} = 2A, V _{OUT} =1.8V	V _{DROP}		700	900	
Dropout Voltage	I _{OUT} = 2A, V _{OUT} =3.3V			550	700	mV
	I _{OUT} = 2A, V _{OUT} =5.0V			480	600	
Line Regulation	V _{IN} = V _{OUT} + 1V to 6V, I _{OUT} =1mA	ΔV_{LIR}		3	15	mV
Load Regulation	I _{OUT} =1mA to 2A	ΔV_{LOR}		5	15	mV
Ripple Rejection	f=1KHz, Ripple=0.5Vp-p,	PSRR		70		dB
Output Noise Voltage	C _{BP} = 22nF, f=10Hz ~100KHz			24		μVrms
Temperature Coefficient		тс		50		ppm/°C
Thermal Shutdown Temperature	$V_{IN} = V_{OUT} + 1V$	T _{SD}		150		°C
Thermal Shutdown Hysteresis		ΔT_{SD}		20		°C
ADJ Pin Specifications						
ADJ Pin Current	$V_{ADJ} = V_{REF}$	I _{ADJ}		10	100	nA
ADJ Pin Threshold		VTH(_{ADJ)}	0.05	0.1	0.2	V
Reference Voltage Tolerance		V _{REF}	0.686	0.7	0.714	V

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ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Shutdown Pin Specifications						
Shutdown Pin Current	V _{EN} = V _{IN} or GND	I _{EN}		0	0.5	μA
Shutdown Exit Delay Time	I _{OUT} = 30mA	Δt		100		μS
Max Output Discharge Resistance to GND during Shutdown		RDSON_ CLMP		20	100	Ω
Shutdown Input Threshold	Chip Enable Low, Output OFF, $V_{IN} = 1.6V$ to $6V$ Chip Enable High, Output ON, $V_{IN} = 1.6V$ to $6V$	V _{ENH}	1.6			
	Chip Enable Low, Output ON, V_{IN} = 1.6V to 6V Chip Enable High, Output OFF, V_{IN} = 1.6V to 6V	V _{ENL}			0.4	V
Power Good Specifications						
PGOOD Rise Threshold				90	93	%
PGOOD Hysteresis			3	10		%
PGOOD Sink Capability	I _{PGOOD} =10mA			0.2	0.4	V
PGOOD Delay			0.5		5	ms

Note 1: In the case of V_{out} <1.8V, 10µF C_{out} is recommended.

Note 2: Specifications are production tested at T_=25°C.pecifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 3: V_{in}(min) is the higher value of Vout + Dropout Voltage or 1.8V.

TYPICAL PERFORMANCE CHARACTERISTICS



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Fig. 3 Quiescent Current vs. Temperature at V_{OUT} =1.8V



Fig. 5 Ground Current vs. Input Voltage at V_{OUT} =1.8V





Fig. 4 Quiescent Current vs. Temperature at V_{OUT} =3.3V



Fig.6 Ground Current vs. Input Voltage at V_{OUT}=3.3V

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



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Fig. 15 Line Transient Response at V_{OUT} =5.0V



Fig.17 Load Transient Response at $V_{\text{OUT}}\text{=}3.3V$



Fig.16 Load Transient Response at V_{OUT}=1.8V





TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

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Fig. 23 Current Fold Back at V_{OUT} =3.3V

Fig.24 PSRR Curve



BLOCK DIAGRAM



PIN DESCRIPTION

VIN
GND
VOUT
EN (5 Pin and 8 Pin)
EN (5 Pin and 8 Pin)
BP (5 Pin and 8 Pin)

- Power supply input pin. Bypass with a $4.7\mu F$ capacitor to GND.
- Ground.
- Regulator Output pin. Sources up to 2A.
- Chip Enable (Active Low). This pin isn't allowed to float.
- Chip Enable (Active High). This pin isn't allowed to float.
 - Bypass pin. It should be connected to external 22nF capacitor to GND to reduce output noise. The bypass pin could be floating if it's unnecessary.
 - Power Good open Drain output.

ADJ (5 Pin and 8 Pin)

PGOOD (8 Pin)

 The output voltage can either be set by the internal feedback resistors when this pin is grounded, or be set by the external feedback resistors when using a resistive divider.

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APPLICATION INFORMATION

The AIC1221 is a high performance linear regulator that provides low-dropout voltage and low quiescentcurrent. The device is available in an adjustable version and fixed output voltages ranging from 0.8V to 5.5V, and the device can supply loads up to 2A.

SHUTDOWN

By connecting $\overline{\text{EN}}$ (EN) pin to V_{IN} (ground), the AIC1221 can be shutdown to reduce the supply current to 0.01µA(typ.). At this operation mode, the output voltage of AIC1221 is equal to 0V.

CURRENT LIMIT

The AIC1221 includes a current limiter, which monitors and controls the maximum output current. If the output is overloaded or shorted to ground, this can protect the device from being damaged.

THERMAL PROTECTION

The AIC1221 includes a thermal-limiting circuit, which is designed to protect the device against overload condition. When the junction temperature exceeds T_J =150°C, the thermal-limiting circuit turns off the pass transistor and allows the IC to cool. For continuous load condition, maximum rating of junction temperature must not be exceeded.

INPUT-OUTPUT CAPACITORS

Linear regulators require input and output capacitors to maintain stability. Input capacitor with a 4.7 μ F, Output capacitor with a 4.7 μ F or 10 μ F (V_{out} <1.8V, 10 μ F C_{out} is recommended) ceramic output capacitor is recommended. When choosing the input and output ceramic capacitors, X5R and X7R types are recommended because they retain their capacitance over wider ranges of voltage and temperature than other types.

NOISE BYPASS CAPACITOR

A 22nF bypass capacitor at BP pin can reduce output voltage noise. The bypass pin can be floating if it's unnecessary.

OUTPUT VOLTAGE PROGRAMMING

Its internal feedback resistors can set the output voltage of AIC1221 linear regulator when the ADJ pin is grounded. In addition, the external feedback resistors when connecting a resistive divider R1 and R2 can set the output voltage of AIC1221 linear regulator. While connecting a resistive divider, V_{OUT} can be calculated as:

$$V_{\text{OUT}} = 0.7 \times \left(1 + \frac{R_1}{R_2}\right)$$

The resistive divider should sit as close to ADJ pin as possible.

POWER DISSIPATION

The maximum power dissipation of AIC1221 depends on the thermal resistance of its case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The rate of temperature rise is greatly affected by the mounting pad configuration on the PCB, the board material, and the ambient temperature. When the IC mounting with good thermal conductivity is used, the junction temperature will be low even when large power dissipation applies.

The power dissipation across the device is

 $P = I_{OUT} (V_{IN} - V_{OUT})$

The maximum power dissipation is:

$$\mathsf{P}_{\mathsf{MAX}} = \frac{(\mathsf{T}_{\mathsf{J}\text{-max}} - \mathsf{T}_{\mathsf{A}})}{\mathsf{R}\boldsymbol{\theta}_{\mathsf{JA}}}$$

Where T_{J-max} is the maximum allowable junction temperature (150°C), and T_A is the ambient temperature suitable in application.

As a general rule, the lower temperature is, the better reliability of the device is. So the PCB mounting pad should provide maximum thermal conductivity to maintain low device temperature.

LAYOUT CONSIDERATION

Connect the bottom-side pad to a large ground plane. Use as much copper as possible to decrease the thermal resistance of the device.





PHYSICAL DIMENSIONS

• SOT-223 PACKAGE OUTLINE DRAWING



s Y	SOT-223			
M B	MILLIMETERS			
0 L	MIN.	MAX.		
А		1.80		
A1	0.02	0.10		
A2	1.55	1.65		
b	0.66	0.84		
b2	2.90	3.10		
с	0.23	0.33		
D	6.30	6.70		
E	6.70	7.30		
E1	3.30	3.70		
е	2.30 BSC			
e1	4.60 BSC			
L	0.90			
θ	0°	8°		

Note: 1. Refer to JEDEC TO-261AA.

- 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
- 3. Dimension "E1" does not include inter-lead flash or protrusions.
- 4. Controlling dimension is millimeter, converted inch
- dimensions are not necessarily exact.



TO-252-3L PACKAGE OUTLINE DRAWING

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S	TO-2	52-3L	
M B	MILLIMETERS		
0 L	MIN.	MAX.	
А	2.19	2.38	
A1	0.00	0.13	
b	0.64	0.89	
b3	4.95	5.46	
С	0.46	0.61	
c2	0.46	0.89	
D	5.33	6.22	
E	6.35	6.73	
е	2.28 BSC		
Н	9.40	10.41	
L	1.40	1.78	
L1	2.67 REF		
L2	0.51 BSC		
L3	0.89	2.03	
L4		1.02	
θ	0°	8°	

- Note: 1. Refer to JEDEC TO-252AA and AB.
 - 2. Dimension "E" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 - 3. Dimension "D" does not include inter-lead flash or protrusions.
 - 4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.



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TO-252-5L PACKAGE OUTLINE DRAWING

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SEE VIEW B

b

SECTION A-A



S V	TO-252-5L MILLIMETERS			
M B				
O L	MIN.	MAX.		
А	2.19	2.38		
A1	0.00	0.13		
b	0.51	0.71		
b3	4.32	5.46		
С	0.46	0.61		
c2	0.46	0.89		
D	5.33	6.22		
Е	6.35	6.73		
е	1.27 BSC			
Н	9.40	10.41		
L	1.40	1.78		
L1	2.67 REF			
L2	0.51 BSC			
L3	0.89	2.03		
q	0°	8°		



- Note: 1. Refer to JEDEC TO-252AD and AB.
 - 2. Dimension "E" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .3. Dimension "D" does not include inter-lead flash or protrusions.

 - 4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

• SOP-8 Exposed Pad (Heat Sink) PACKAGE OUTLINE DRAWING



Note : 1. Refer to JEDEC MS-012E.

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- 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
- 3. Dimension "E" does not include inter-lead flash or protrusions.
- 4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

S	SOP-8 Exposed Pad(Heat Sink)		
M B	MILLIMETERS		
0 L	MIN.	MAX.	
А	1.35	1.75	
A1	0.00	0.15	
В	0.31	0.51	
С	0.17	0.25	
D	4.80	5.00	
E	3.80	4.00	
е	1.27 BSC		
Н	5.80	6.20	
h	0.25	0.50	
L	0.40	1.27	
q	0°	8°	
D1	1.5	3.5	
E1	1.0	2.55	

Note:

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